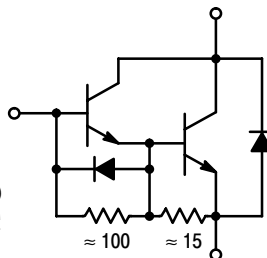


SWITCHMODE™ Series NPN Silicon Power Darlington Transistor with Base-Emitter Speedup Diode

The MJ10005 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

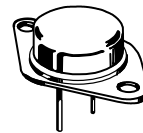
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits
- Fast Turn-Off Times
 - 40 ns Inductive Fall Time — 25°C (Typ)
 - 650 ns Inductive Storage Time — 25°C (Typ)
 - Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
 - Reversed Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents



MJ10005*

*ON Semiconductor Preferred Device

**20 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
400 VOLTS
175 WATTS**



**CASE 1-07
TO-204AA
(TO-3)**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	400	Vdc
Collector-Emitter Voltage	V_{CEX}	450	Vdc
Collector-Emitter Voltage	V_{CEV}	500	Vdc
Emitter Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous	I_C	20	Adc
— Peak (1)	I_{CM}	30	
Base Current — Continuous	I_B	2.5	Adc
— Peak (1)	I_{BM}	5.0	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	175	Watts
@ $T_C = 100^\circ\text{C}$		100	
Derate above 25°C		1.0	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle \leq 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

MJ10005

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 1) (I _C = 250 mA, I _B = 0, V _{clamp} = Rated V _{CEO})	V _{CEO(sus)}	400	—	—	Vdc
Collector Emitter Sustaining Voltage (Table 1, Figure 12) (I _C = 2.0 A, V _{clamp} = Rated V _{CEX} , T _C = 100°C) (I _C = 10 A, V _{clamp} = Rated V _{CEX} , T _C = 100°C)	V _{CEX(sus)}	450 325	— —	— —	Vdc
Collector Cutoff Current (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc) (V _{CEV} = Rated Value, V _{BE(off)} = 1.5 Vdc, T _C = 150°C)	I _{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current (V _{CE} = Rated V _{CEV} , R _{BE} = 50 Ω, T _C = 100°C)	I _{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V _{EB} = 2.0 Vdc, I _C = 0)	I _{EBO}	—	—	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	I _{S/b}	See Figure 11			
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ON CHARACTERISTICS (2)

DC Current Gain (I _C = 5.0 Adc, V _{CE} = 5.0 Vdc) (I _C = 10 Adc, V _{CE} = 5.0 Vdc)	h _{FE}	50 40	— —	600 400	—
Collector Emitter Saturation Voltage (I _C = 10 Adc, I _B = 400 mAdc) (I _C = 20 Adc, I _B = 2.0 Adc) (I _C = 10 Adc, I _B = 400 mAdc, T _C = 100°C)	V _{CE(sat)}	— — —	— — —	1.9 3.0 2.0	Vdc
Base Emitter Saturation Voltage (I _C = 10 Adc, I _B = 400 mAdc) (I _C = 10 Adc, I _B = 400 mAdc, T _C = 100°C)	V _{BE(sat)}	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage (1) (I _F = 10 Adc)	V _f	—	3.0	5.0	Vdc

DYNAMIC CHARACTERISTICS

Small–Signal Current Gain (I _C = 1.0 Adc, V _{CE} = 10 Vdc, f _{test} = 1.0 MHz)	h _{fe}	10	—	—	—
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f _{test} = 100 kHz)	C _{ob}	100	—	325	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 250 Vdc, I _C = 10 A, I _{B1} = 400 mA, V _{BE(off)} = 5.0 Vdc, t _p = 50 μs, Duty Cycle ≤ 2%).	t _d	—	0.12	0.2	μs
Rise Time		t _r	—	0.2	0.6	μs
Storage Time		t _s	—	0.6	1.5	μs
Fall Time		t _f	—	0.15	0.5	μs
Inductive Load Clamped (Table 1)						
Storage Time	(I _C = 10 A(pk), V _{clamp} = Rated V _{CEX} , I _{B1} = 400 mA, V _{BE(off)} = 5.0 Vdc, T _C = 100°C)	t _{sv}	—	1.0	2.5	μs
Crossover Time		t _c	—	0.4	1.5	μs
Storage Time	(I _C = 10 A(pk), V _{clamp} = Rated V _{CEX} , I _{B1} = 400 mA, V _{BE(off)} = 5.0 Vdc, T _C = 25°C)	t _{sv}	—	0.65	—	μs
Crossover Time		t _c	—	0.2	—	μs

- (1) The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.
- (2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

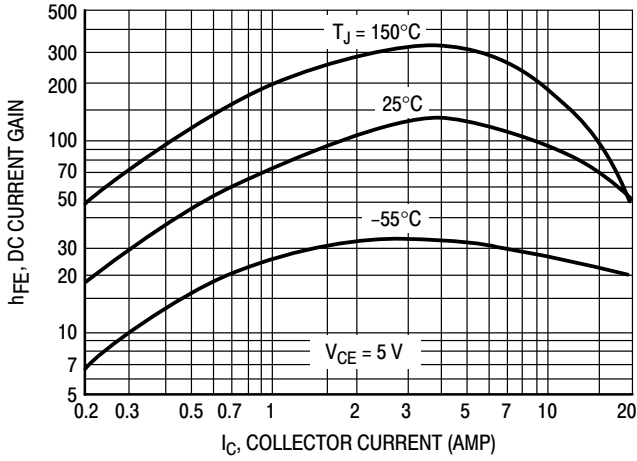


Figure 1. DC Current Gain

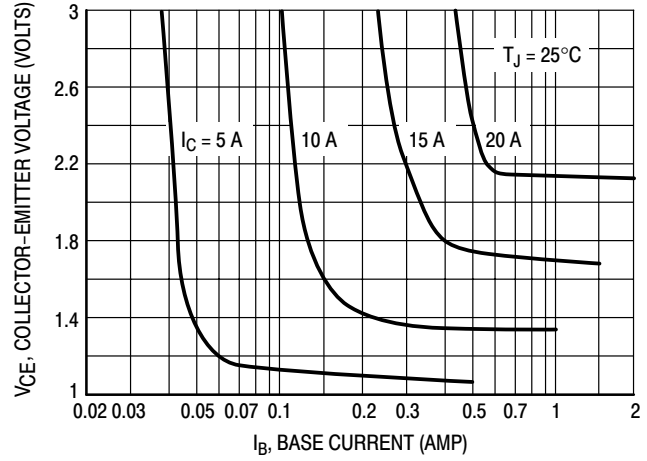


Figure 2. Collector Saturation Region

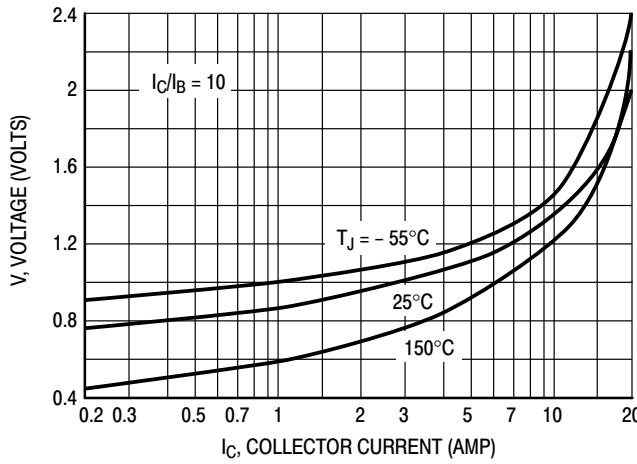


Figure 3. Collector-Emitter Saturation Voltage

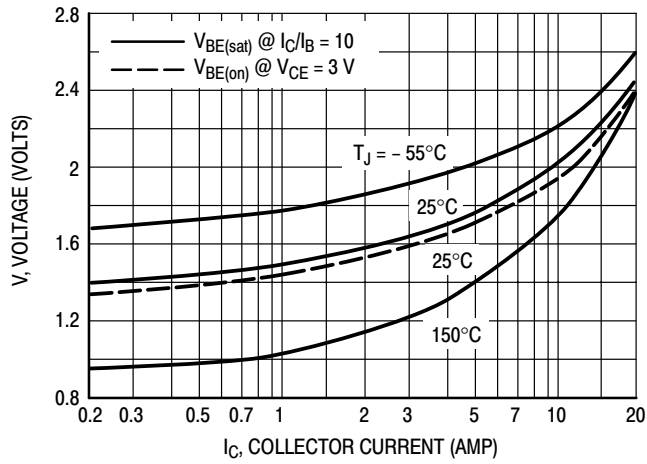


Figure 4. Base-Emitter Voltage

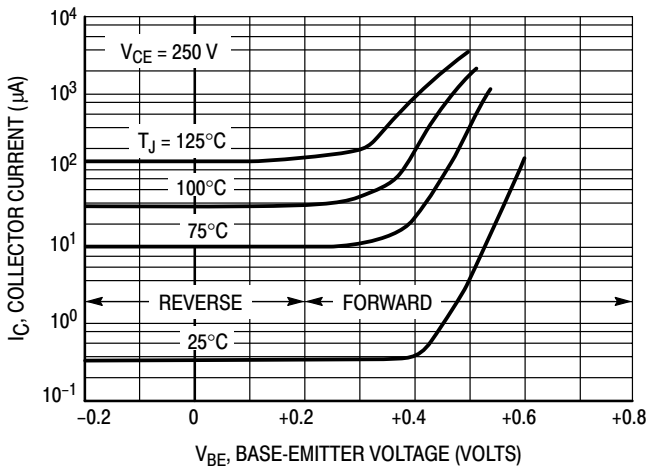


Figure 5. Collector Cutoff Region

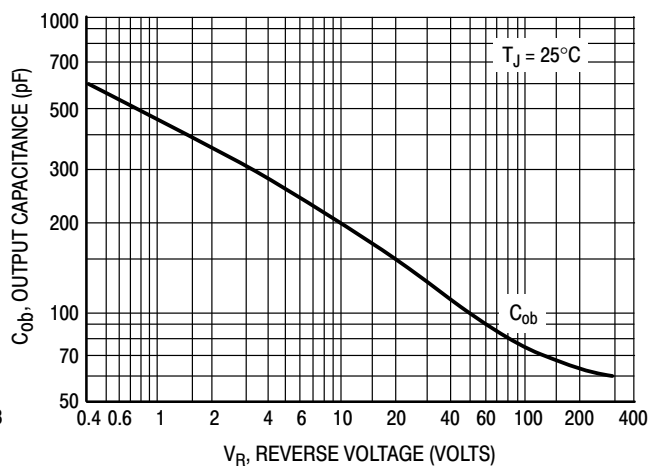


Figure 6. Output Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CE0(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	<p>PW Varied to Attain $I_C = 250 \text{ mA}$</p>	<p>INDUCTIVE TEST CIRCUIT</p> <p>SEE ABOVE FOR DETAILED CONDITIONS</p>	
CIRCUIT VALUES	$L_{coil} = 10 \text{ mH}$, $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CE0(sus)}$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$ $V_{clamp} = \text{Rated } V_{CEX} \text{ Value}$	$V_{CC} = 250 \text{ V}$ $R_L = 25 \Omega$ Pulse Width = $50 \mu\text{s}$
TEST CIRCUITS	<p>INDUCTIVE TEST CIRCUIT</p> <p>SEE ABOVE FOR DETAILED CONDITIONS</p>	<p>OUTPUT WAVEFORMS</p> <p>t_1 Adjusted to Obtain I_C</p> $t_1 \approx \frac{L_{coil} (I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{Cpk})}{V_{Clamp}}$ <p>Test Equipment Scope — Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p>

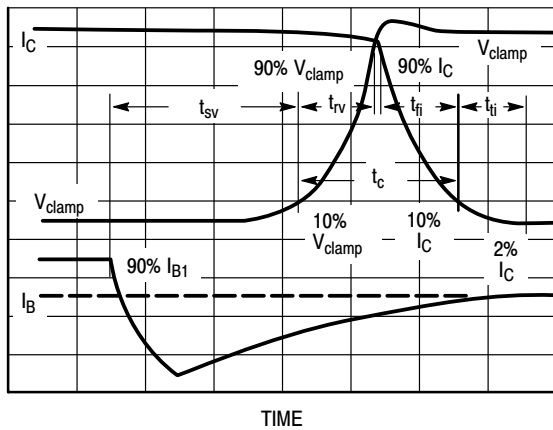


Figure 7. Inductive Switching Measurements

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate

measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
- t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
- t_{fi} = Current Fall Time, 90–10% I_C
- t_{ti} = Current Tail, 10–2% I_C
- t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222.

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \approx t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

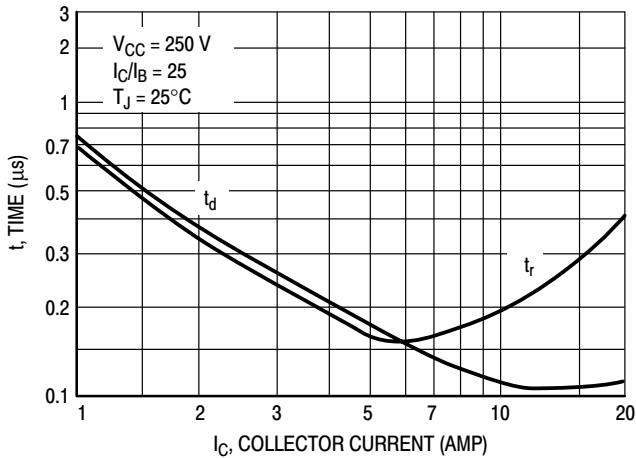


Figure 8. Turn-On Time

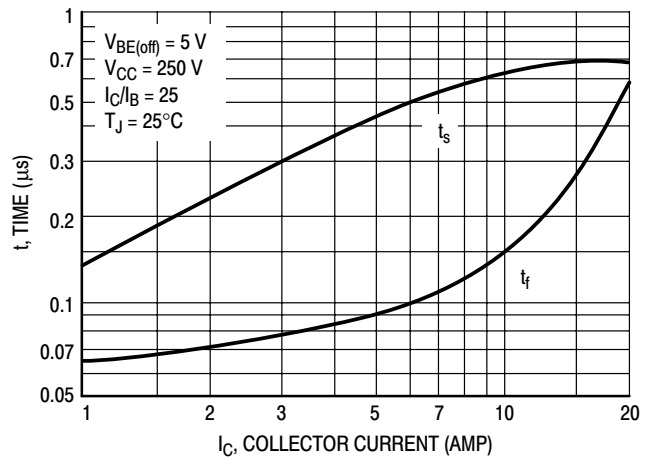


Figure 9. Turn-Off Time

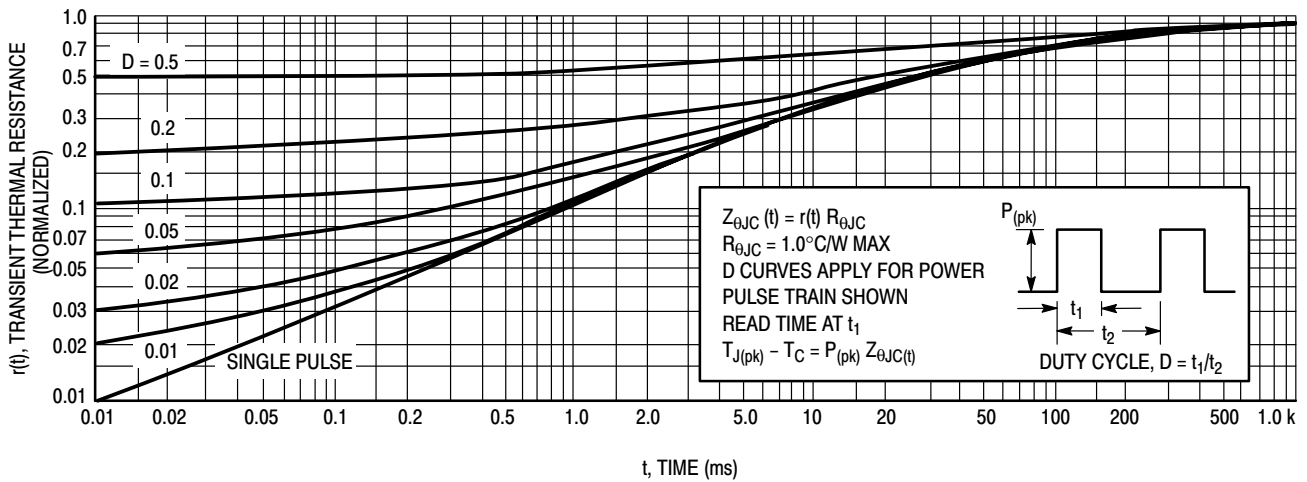


Figure 10. Thermal Response

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

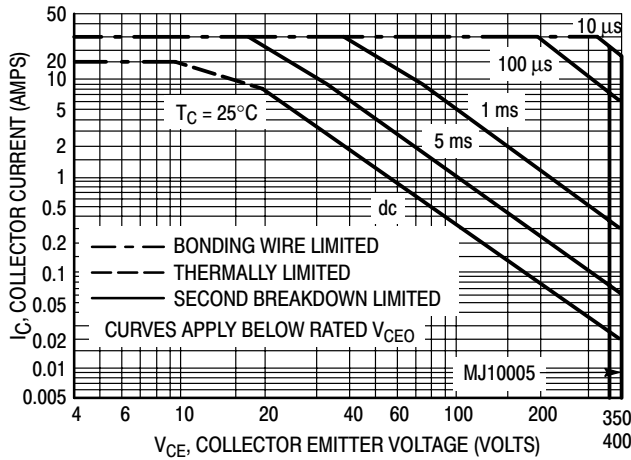


Figure 11. Forward Bias Safe Operating Area

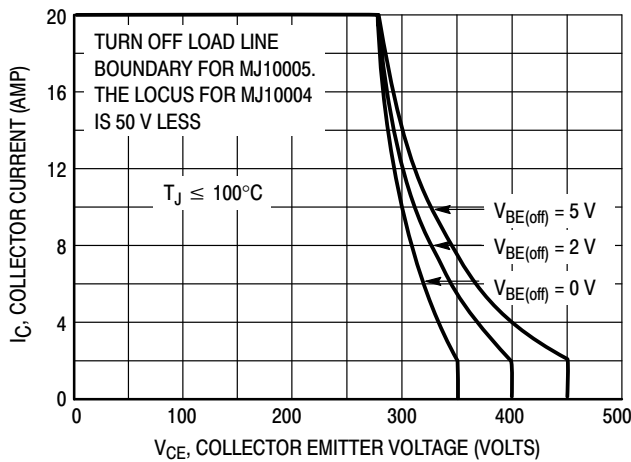


Figure 12. Reverse Bias Switching Safe Operating Area

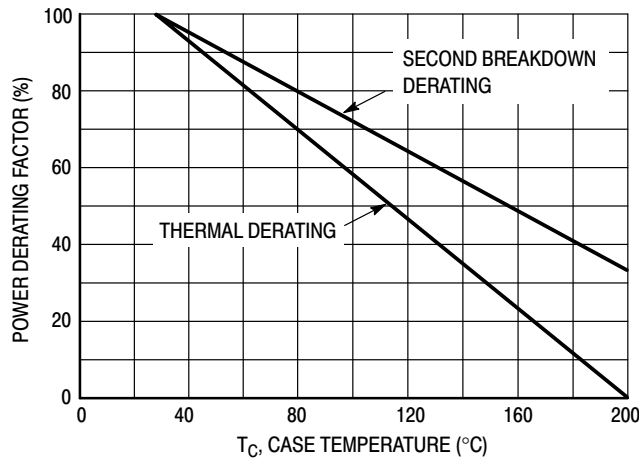


Figure 13. Power Derating

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

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