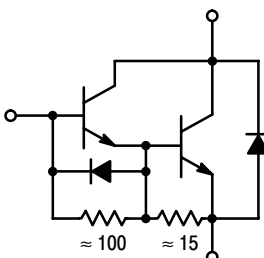


SWITCHMODE™ Series

NPN Silicon Power Darlington Transistor with Base-Emitter Speedup Diode

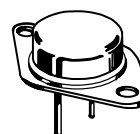
The MJ10023 Darlington transistor is designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line-operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
 - 150 ns Inductive Fall Time @ 25°C (Typ)
 - 300 ns Inductive Storage Time @ 25°C (Typ)
- Operating Temperature Range – 65 to + 200°C
- 100°C Performance Specified for:
 - Reversed Biased SOA with Inductive Loads
 - Switching Times with Inductive Loads
 - Saturation Voltages
 - Leakage Currents



MJ10023

40 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTOR
400 VOLTS
250 WATTS



CASE 197A-05
TO-204AE (TO-3)

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	Vdc
Emitter Base Voltage	V_{EB}	80	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	40 80	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	20 40	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$ Derate above 25°C	P_D	250 143 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (Table 1) ($I_C = 100\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$)	I_{CEV}	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEV}$, $R_{BE} = 50\ \Omega$, $T_C = 100^\circ\text{C}$)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current ($V_{EB} = 2.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	175	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$		See Figure 13	
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 14	

ON CHARACTERISTICS (1)

DC Current Gain ($I_C = 10\text{ Adc}$, $V_{CE} = 5.0\text{ V}$)	h_{FE}	50	—	600	—
Collector–Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 1.0\text{ Adc}$) ($I_C = 40\text{ Adc}$, $I_B = 5.0\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 10\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	— — —	— — —	2.2 5.0 2.5	Vdc
Base–Emitter Saturation Voltage ($I_C = 20\text{ Adc}$, $I_B = 1.2\text{ Adc}$) ($I_C = 20\text{ Adc}$, $I_B = 1.2\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	— —	— —	2.5 2.5	Vdc
Diode Forward Voltage ($I_F = 20\text{ Adc}$)	V_f	—	2.5	5.0	Vdc

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{test} = 1.0\text{ kHz}$)	C_{ob}	150	—	600	pF
--	----------	-----	---	-----	----

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V _{CC} = 250 Vdc, I _C = 20 A, I _{B1} = 1.0 Adc, V _{BE(off)} = 5.0 V, t _p = 50 μs, Duty Cycle ≤ 2.0%)	t _d	—	0.03	0.2	μs
Rise Time		t _r	—	0.4	1.2	μs
Storage Time		t _s	—	0.9	2.5	μs
Fall Time		t _f	—	0.3	0.9	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I _{CM} = 20 A, V _{CEM} = 250 V, I _{B1} = 1.0 A, V _{BE(off)} = 5 V, T _C = 100°C)	t _{sv}	—	1.9	4.4	μs
Crossover Time		t _c	—	0.6	2.0	μs
Fall Time		t _{fi}	—	0.3	—	μs
Storage Time	(I _{CM} = 20 A, V _{CEM} = 250 V, I _{B1} = 1.0 A, V _{BE(off)} = 5 V, T _C = 25°C)	t _{sv}	—	1.0	—	μs
Crossover Time		t _c	—	0.3	—	μs
Fall Time		t _{fi}	—	0.15	—	μs

(1) Pulse Test: $PW = 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

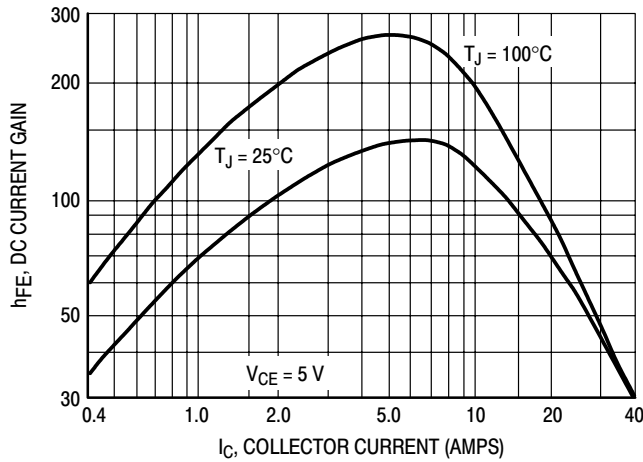


Figure 1. DC Current Gain

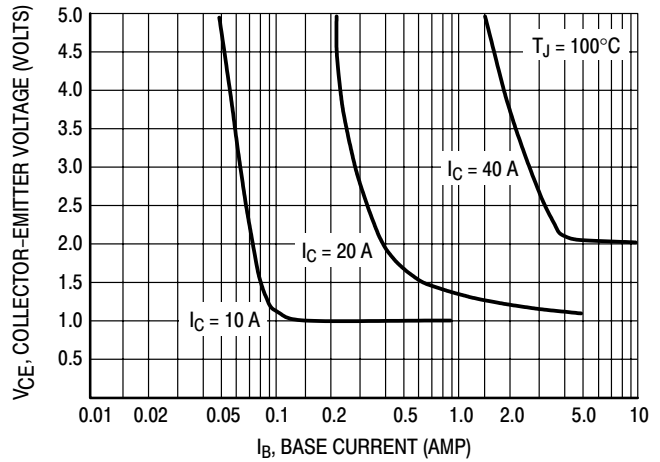


Figure 2. Collector Saturation Region

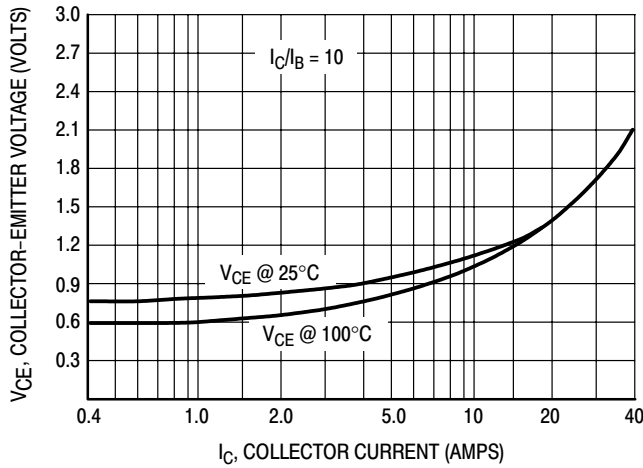


Figure 3. Collector-Emitter Saturation Voltage

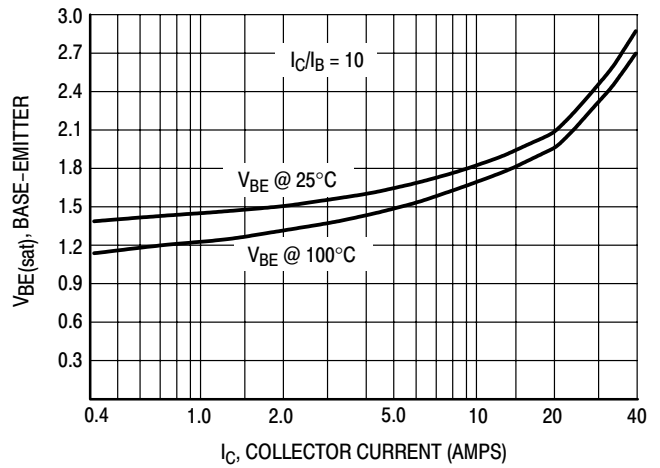


Figure 4. Base-Emitter Saturation Voltage

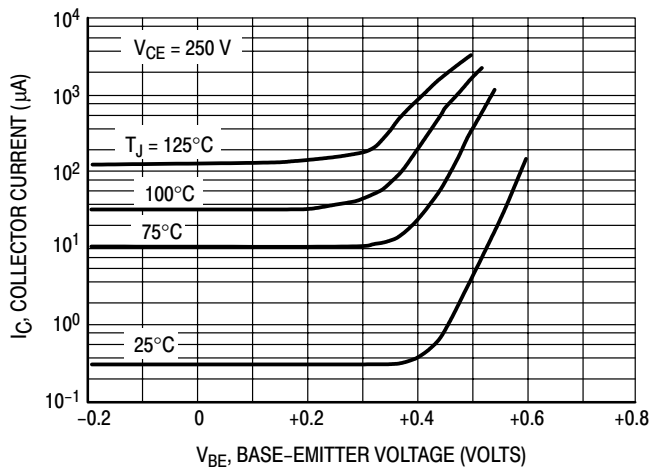


Figure 5. Collector Cutoff Region

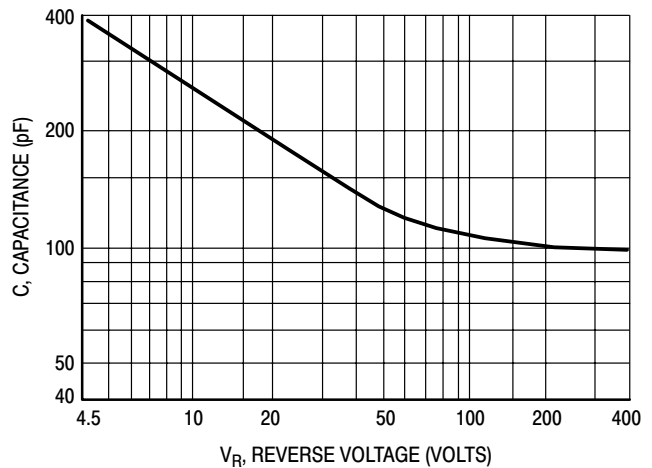
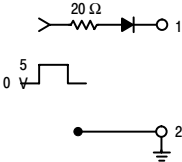
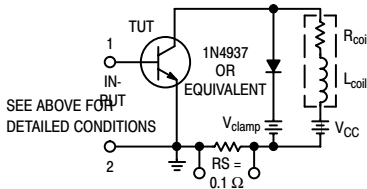
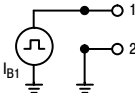
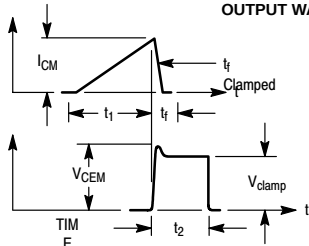
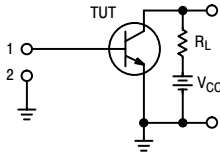


Figure 6. C_{Ob} , Output Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain $I_C = 100 \text{ mA}$	INDUCTIVE TEST CIRCUIT  SEE ABOVE FOR DETAILED CONDITIONS	TURN-ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	$L_{coil} = 10 \text{ mH}$, $V_{CC} = 10 \text{ V}$ $R_{coil} = 0.7 \Omega$ $V_{clamp} = V_{CEO(sus)}$	$L_{coil} = 180 \mu\text{H}$ $R_{coil} = 0.05 \Omega$ $V_{CC} = 20 \text{ V}$	$V_{CC} = 250 \text{ V}$ $R_L = 12.5 \Omega$ Pulse Width = $25 \mu\text{s}$
TEST CIRCUITS	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil} (I_{CM})}{V_{CC}}$$t_2 \approx \frac{L_{coil} (I_{CM})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 	

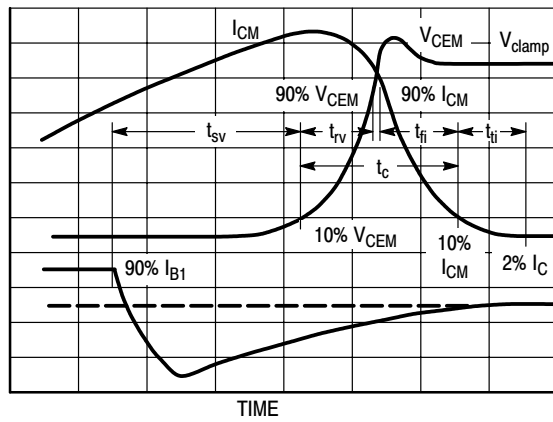


Figure 7. Inductive Switching Measurements

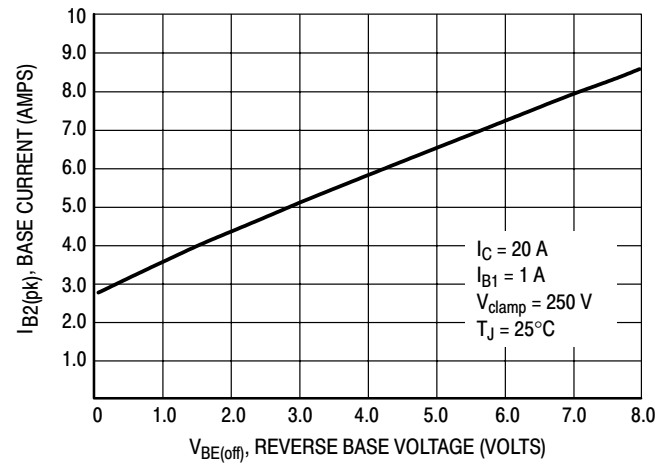


Figure 8. Typical Peak Reverse Base Current

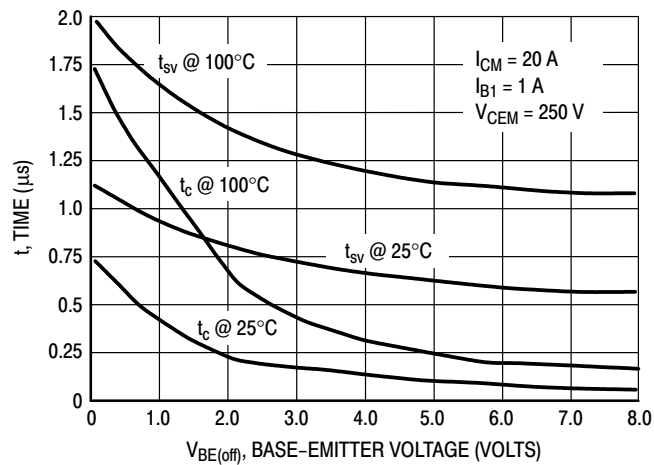


Figure 9. Typical Inductive Switching Times

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{SV} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}

t_{RV} = Voltage Rise Time, 10–90% V_{CEM}

t_{fi} = Current Fall Time, 90–10% I_{CM}

t_{ti} = Current Tail, 10–2% I_{CM}

t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_c) f$$

In general, $t_{RV} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user orientated specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{SV}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

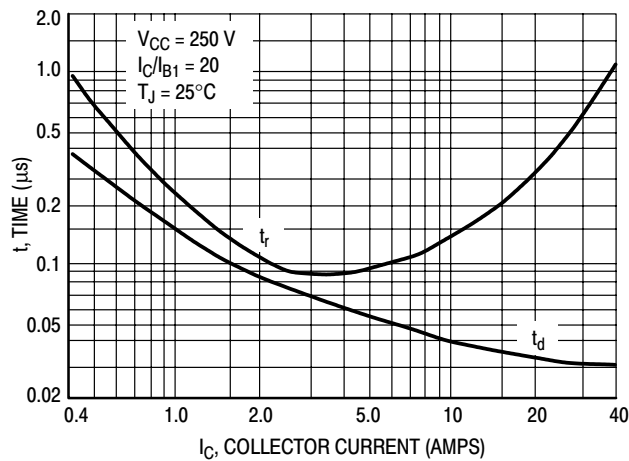


Figure 10. Typical Turn-On Switching Times

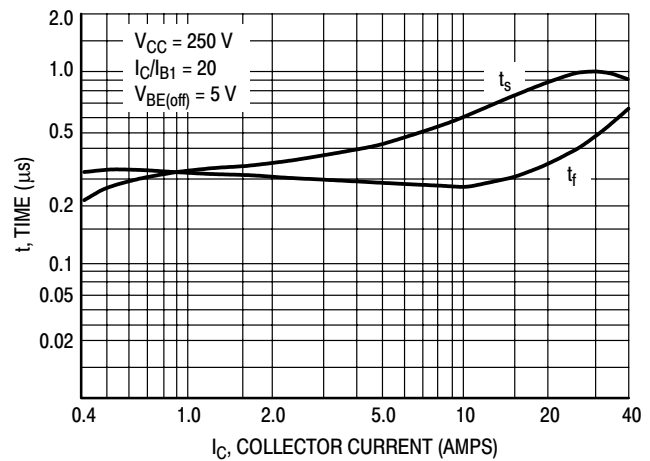


Figure 11. Typical Turn-Off Switching Times

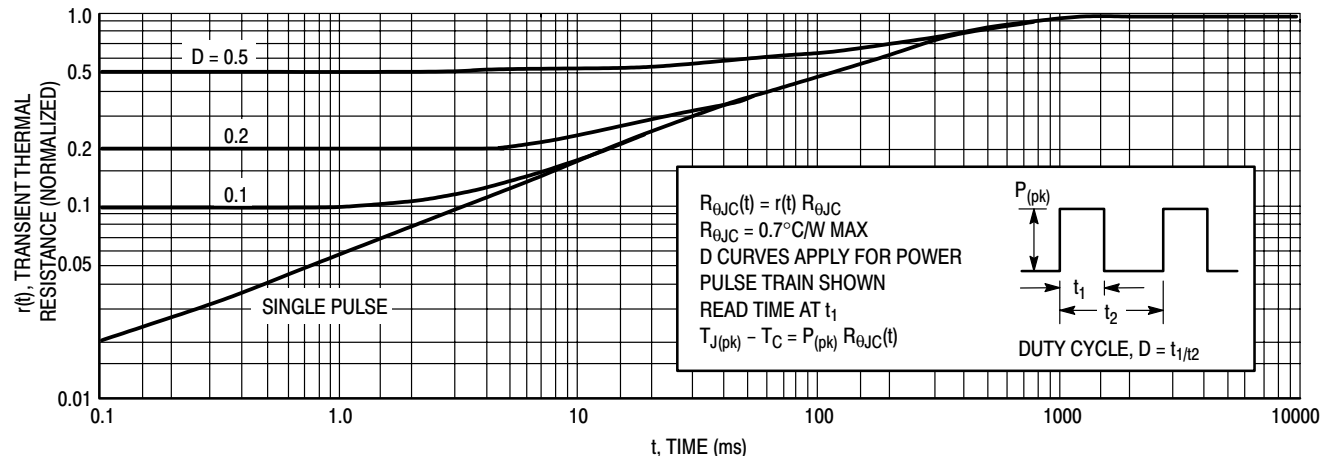


Figure 12. Thermal Response

The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

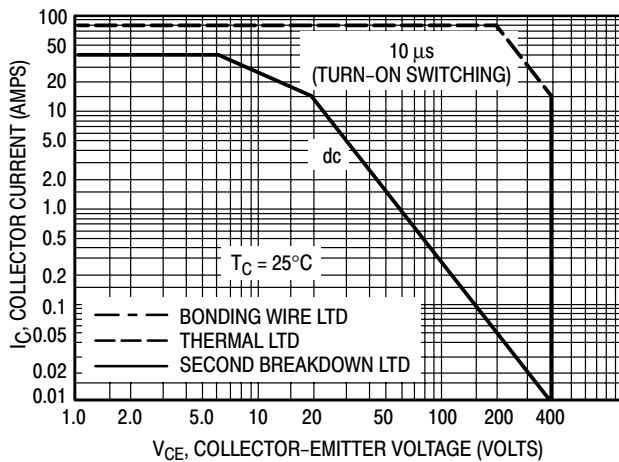


Figure 13. Maximum Forward Bias Safe Operating Area

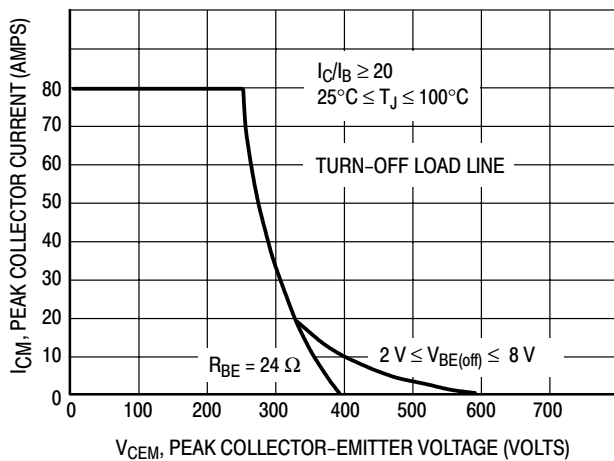


Figure 14. Maximum RBSOA, Reverse Bias Safe Operating Area

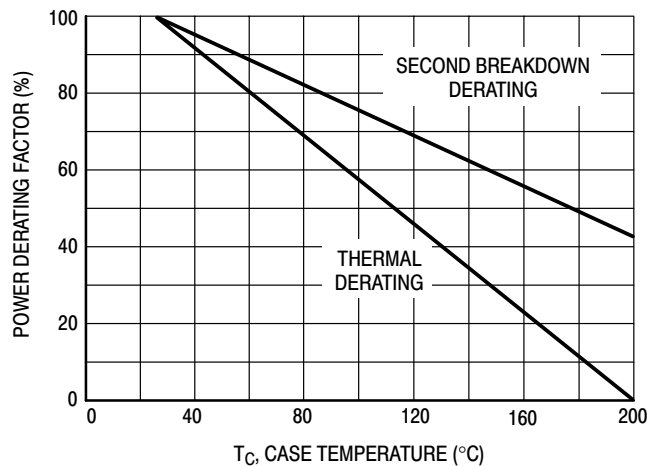


Figure 15. Power Derating

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

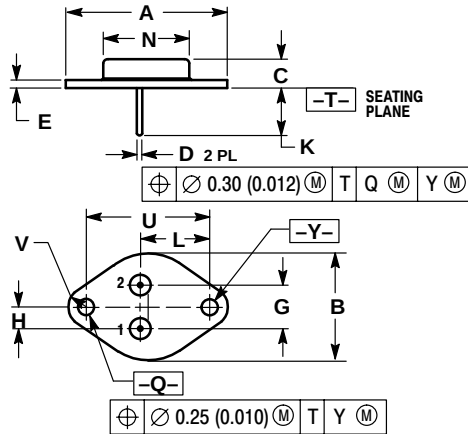
The data of Figure 13 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

PACKAGE DIMENSIONS

CASE 197A-05
TO-204AE (TO-3)
ISSUE J

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:

- PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

SWITCHMODE is a trademark of Semiconductor Components Industries, LLC.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, UK, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com
Toll-Free from Mexico: Dial 01-800-288-2872 for Access –
then Dial 866-297-9322

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 1-303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center

4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.