MMBT4403WT1

Switching Transistor

PNP Silicon

Moisture Sensitivity Level: 1
ESD Rating: Human Body Model – 4 kV
Machine Model – 400 V

MAXIMUM RATINGS

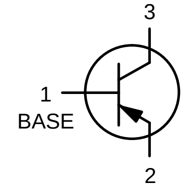
Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	–40	Vdc
Collector–Base Voltage	V_{CBO}	–40	Vdc
Emitter–Base Voltage	V_{EBO}	–5.0	Vdc
Collector Current – Continuous	I_C	–600	mAdc

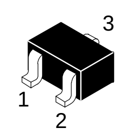
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board T_A = 25°C	P_D	150	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	833	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

ON Semiconductor®

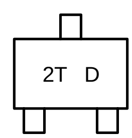
http://onsemi.com





SC–70
CASE 419
STYLE 3

MARKING DIAGRAM



2T = Specific Device Code
D = Date Code

ORDERING INFORMATION

Device	Package	Shipping
MMBT4403WT1	SC–70	3000/Tape & Reel

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

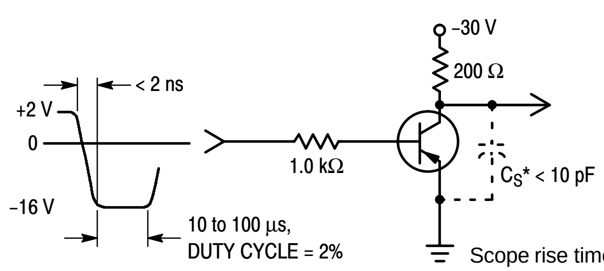
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (Note 1) (I_C = –1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	–40	–	Vdc
Collector–Base Breakdown Voltage (I_C = –0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	–40	–	Vdc
Emitter–Base Breakdown Voltage (I_E = –0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	–5.0	–	Vdc
Base Cutoff Current (V_{CE} = –35 Vdc, V_{EB} = –0.4 Vdc)	I_{BEV}	–	–0.1	µAdc
Collector Cutoff Current (V_{CE} = –35 Vdc, V_{EB} = –0.4 Vdc)	I_{CEX}	–	–0.1	µAdc
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			–
(I_C = –0.1 mAdc, V_{CE} = –1.0 Vdc)		30	–	
(I_C = –1.0 mAdc, V_{CE} = –1.0 Vdc)		60	–	
(I_C = –10 mAdc, V_{CE} = –1.0 Vdc)		100	–	
(I_C = –150 mAdc, V_{CE} = –2.0 Vdc) (Note 1)		100	300	
(I_C = –500 mAdc, V_{CE} = –2.0 Vdc) (Note 1)		20	–	
Collector–Emitter Saturation Voltage (Note 1)	$V_{CE(sat)}$			Vdc
(I_C = –150 mAdc, I_B = –15 mAdc)		–	–0.4	
(I_C = –500 mAdc, I_B = –50 mAdc)		–	–0.75	
Base–Emitter Saturation Voltage (Note 1)	$V_{BE(sat)}$			Vdc
(I_C = –150 mAdc, I_B = –15 mAdc)		–0.75	–0.95	
(I_C = –500 mAdc, I_B = –50 mAdc)		–	–1.3	
SMALL–SIGNAL CHARACTERISTICS				
Current–Gain – Bandwidth Product (I_C = –20 mAdc, V_{CE} = –10 Vdc, f = 100 MHz)	f_T	200	–	MHz
Collector–Base Capacitance (V_{CB} = –10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	–	8.5	pF
Emitter–Base Capacitance (V_{BE} = –0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{eb}	–	30	pF
Input Impedance (I_C = –1.0 mAdc, V_{CE} = –10 Vdc, f = 1.0 kHz)	h_{ie}	1.5	15	kΩ
Voltage Feedback Ratio (I_C = –1.0 mAdc, V_{CE} = –10 Vdc, f = 1.0 kHz)	h_{re}	0.1	8.0	X 10^{-4}
Small–Signal Current Gain (I_C = –1.0 mAdc, V_{CE} = –10 Vdc, f = 1.0 kHz)	h_{fe}	60	500	–
Output Admittance (I_C = –1.0 mAdc, V_{CE} = –10 Vdc, f = 1.0 kHz)	h_{oe}	1.0	100	µmhos

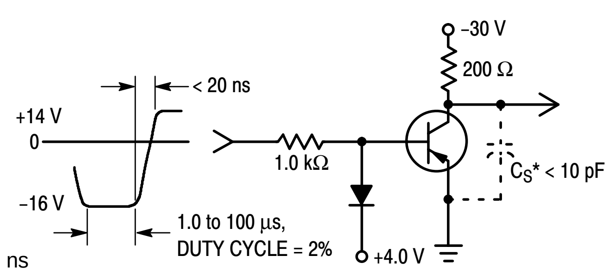
SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Delay Time	(V_{CC} = –30 Vdc, V_{EB} = –2.0 Vdc, I_C = –150 mAdc, I_{B1} = –15 mAdc)	t_d	–	15	ns
Rise Time		t_r	–	20	
Storage Time	(V_{CC} = –30 Vdc, I_C = –150 mAdc, I_{B1} = I_{B2} = –15 mAdc)	t_s	–	225	ns
Fall Time		t_f	–	30	

1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

SWITCHING TIME EQUIVALENT TEST CIRCUIT





Scope rise time < 4.0 ns
*Total shunt capacitance of test jig connectors, and oscilloscope

Figure 1. Turn–On Time **Figure 2. Turn–Off Time**

TRANSIENT CHARACTERISTICS

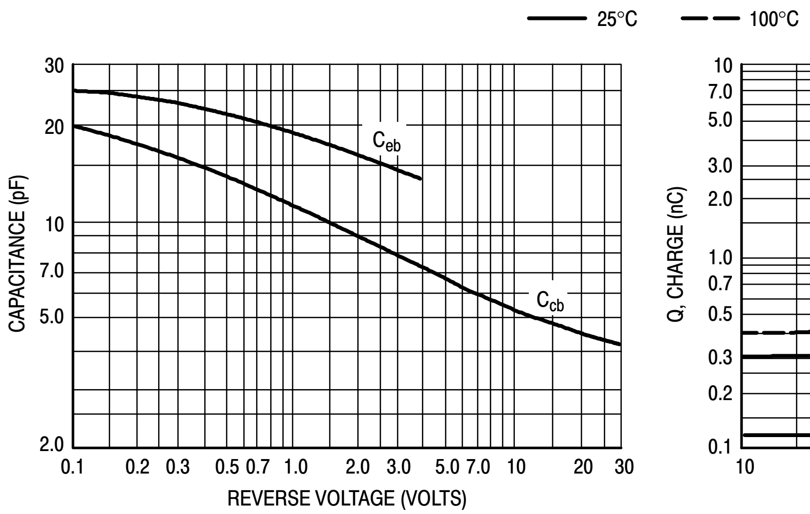


Figure 3. Capacitances

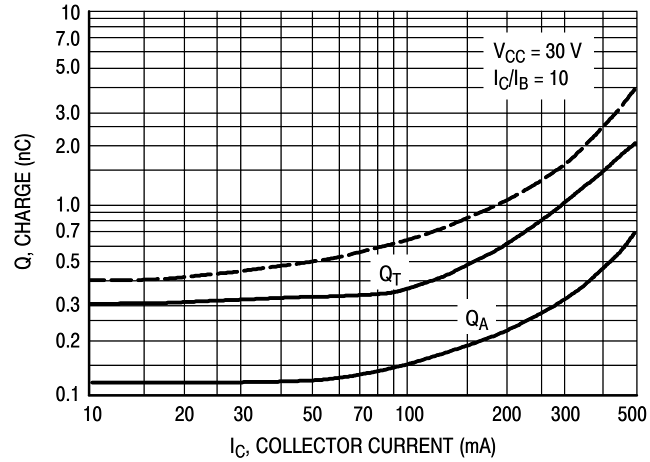


Figure 4. Charge Data

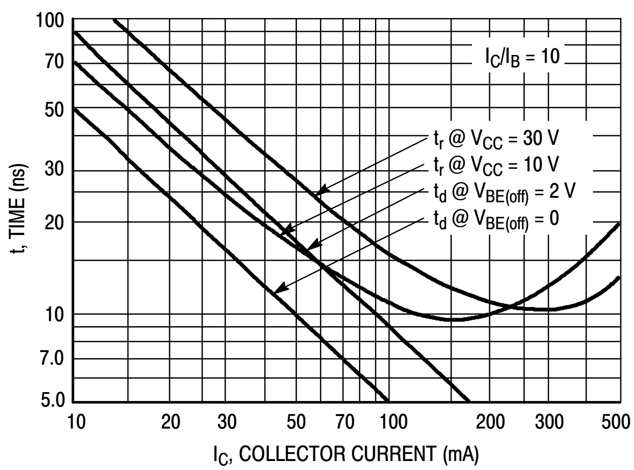


Figure 5. Turn–On Time

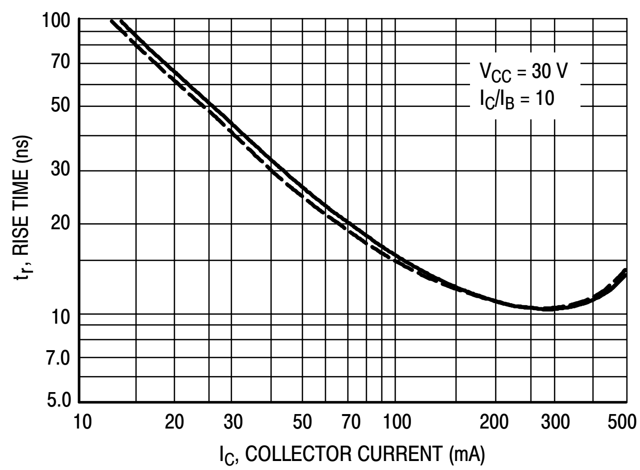


Figure 6. Rise Time

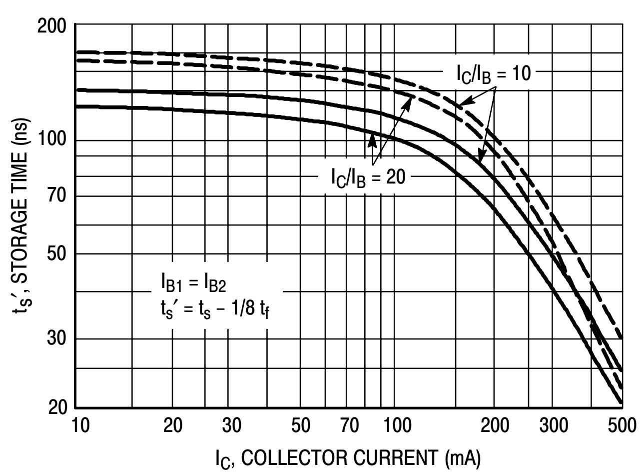


Figure 7. Storage Time

SMALL–SIGNAL CHARACTERISTICS

NOISE FIGURE

V_{CE} = –10 Vdc, T_A = 25°C; Bandwidth = 1.0 Hz

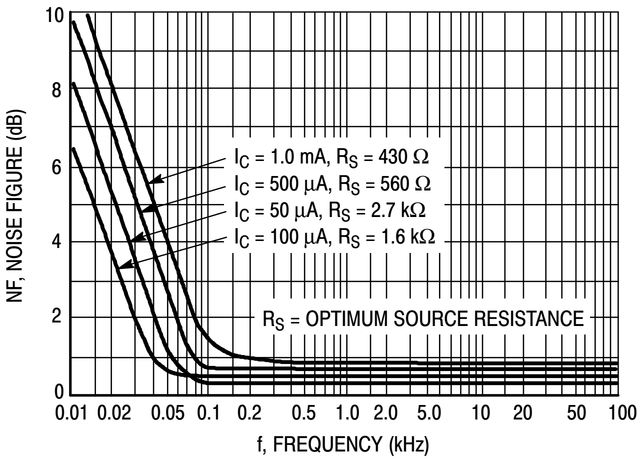


Figure 8. Frequency Effects

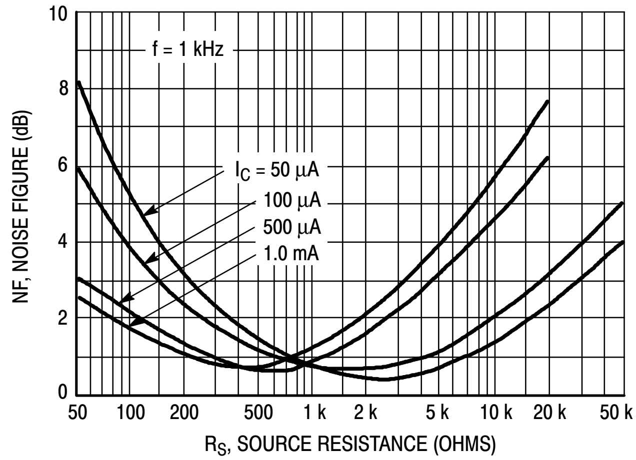


Figure 9. Source Resistance Effects

h PARAMETERS

V_{CE} = –10 Vdc, f = 1.0 kHz, T_A = 25°C

This group of graphs illustrates the relationship between h_{fe} and other "h" parameters for this series of transistors. To obtain these curves, a high–gain and a low–gain unit were selected from the MMBT4403LT1 lines, and the same units were used to develop the correspondingly–numbered curves on each graph.

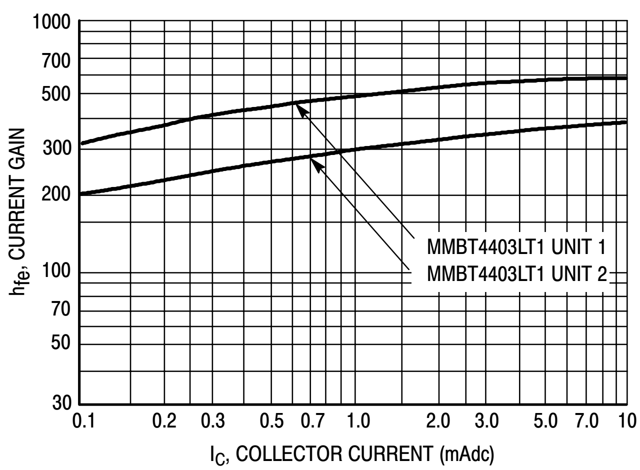


Figure 10. Current Gain

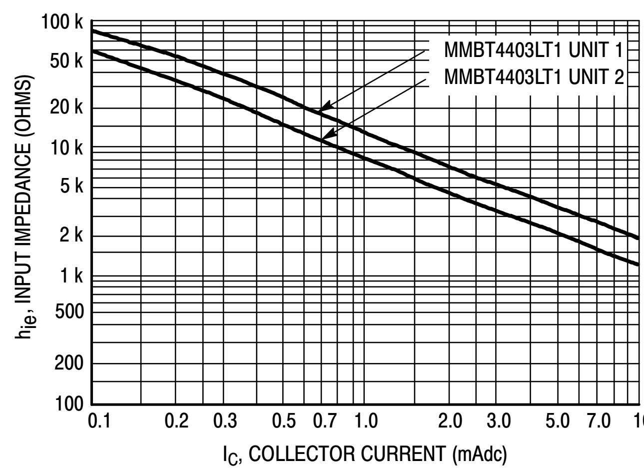


Figure 11. Input Impedance

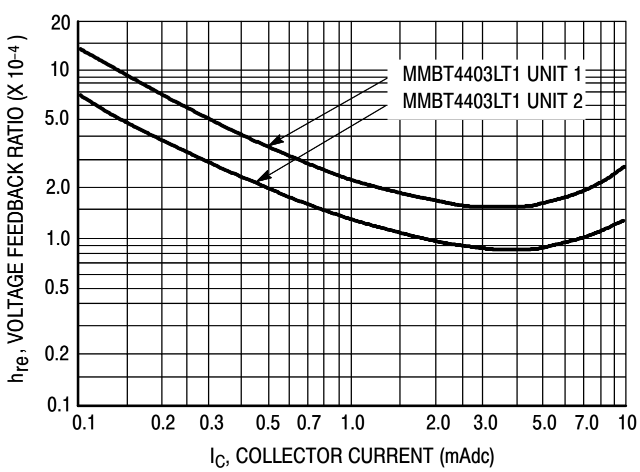


Figure 12. Voltage Feedback Ratio

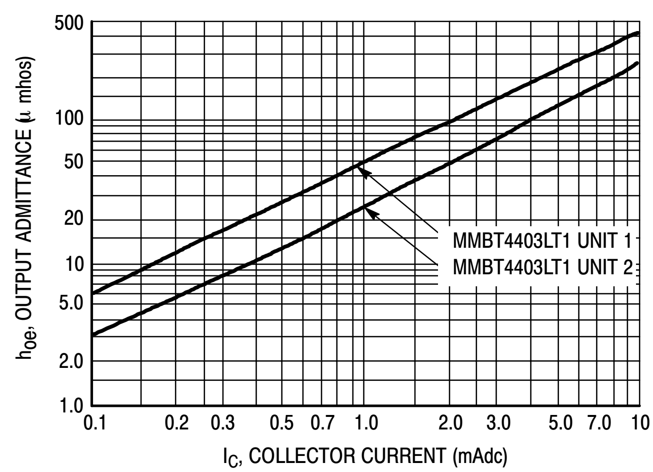


Figure 13. Output Admittance

STATIC CHARACTERISTICS

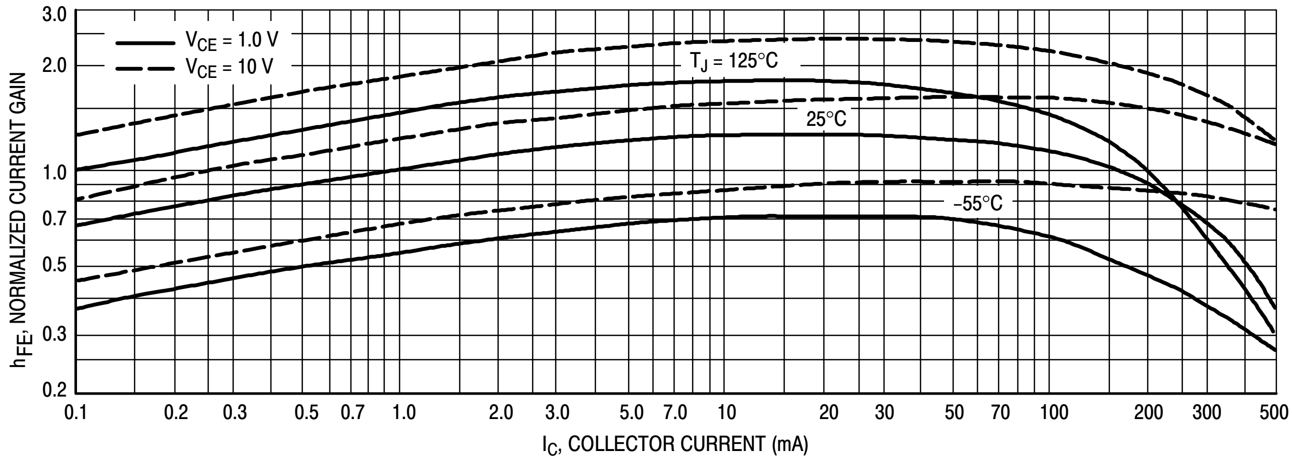


Figure 14. DC Current Gain

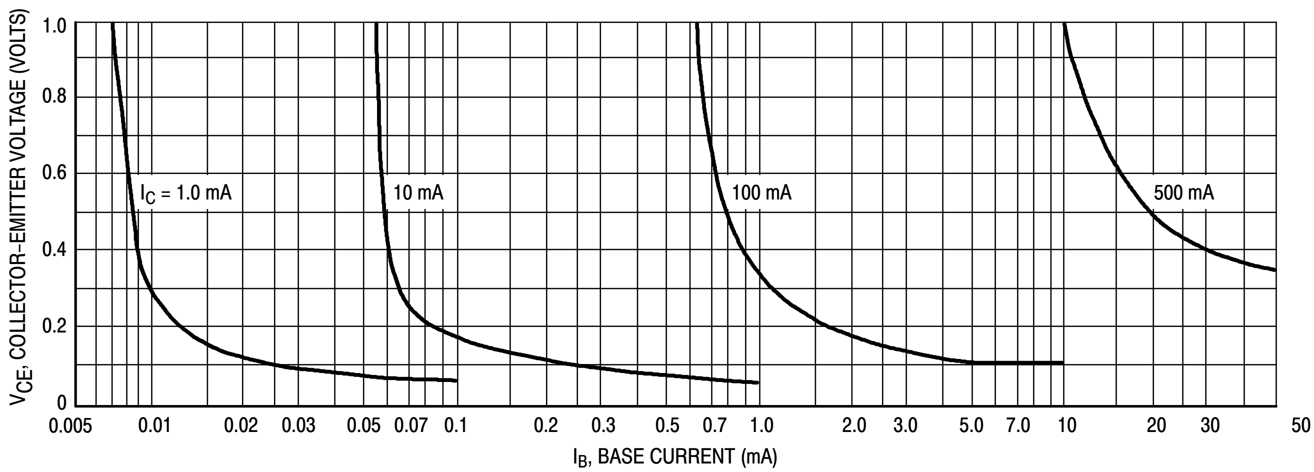


Figure 15. Collector Saturation Region

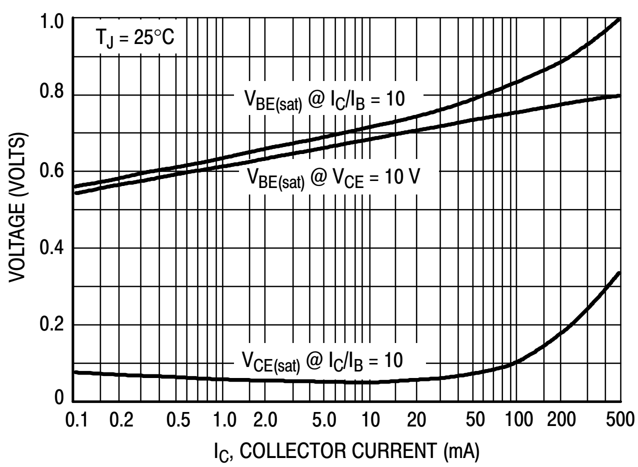


Figure 16. "On" Voltages

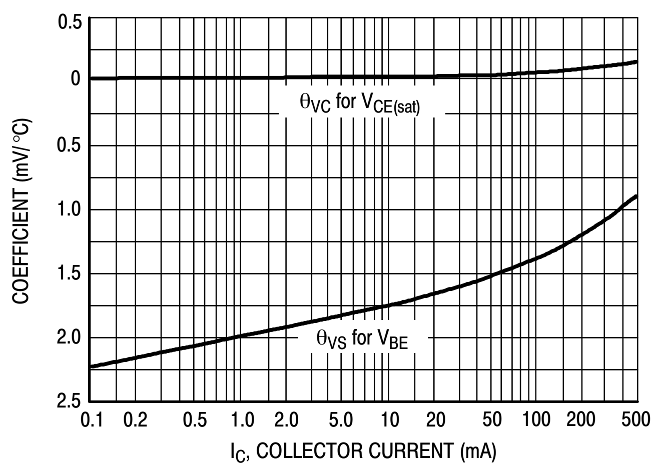
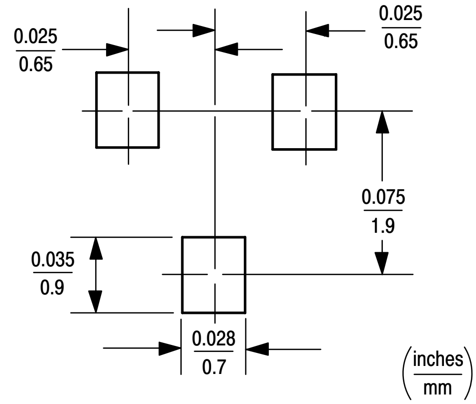


Figure 17. Temperature Coefficients

INFORMATION FOR USING THE SC–70/SOT–323 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SC–70/SOT–323 POWER DISSIPATION

The power dissipation of the SC–70/SOT–323 is a function of the pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 150 milliwatts.

$$P_D = \frac{150°C - 25°C}{833°C/W} = 150 \text{ milliwatts}$$

The 833°C/W assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, a higher power dissipation can be achieved using the same footprint.

SOLDERING PRECAUTIONS

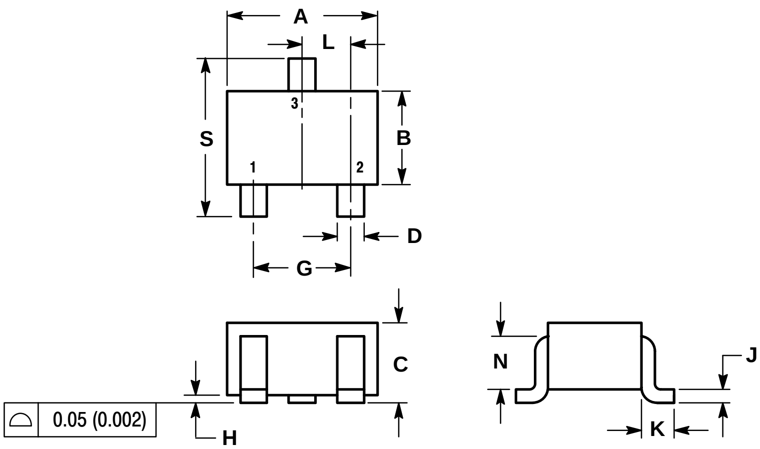
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS

SC–70/SOT–323
CASE 419–04
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.032	0.040	0.80	1.00
D	0.012	0.016	0.30	0.40
G	0.047	0.055	1.20	1.40
H	0.000	0.004	0.00	0.10
J	0.004	0.010	0.10	0.25
K	0.017 REF		0.425 REF	
L	0.026 BSC		0.650 BSC	
N	0.028 REF		0.700 REF	
S	0.079	0.095	2.00	2.40

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

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