MMBTA56W, SMMBTA56W

Driver Transistor

PNP Silicon

Features

- Moisture Sensitivity Level: 1
- ESD Rating:
  - Human Body Model – 4 kV
  - Machine Model – 400 V
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	–80	Vdc
Collector–Base Voltage	V_{CBO}	–80	Vdc
Emitter–Base Voltage	V_{EBO}	–4.0	Vdc
Collector Current – Continuous	I_C	–500	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board T_A = 25°C	P_D	150	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	833	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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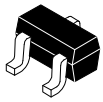
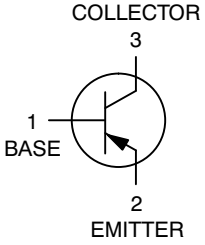
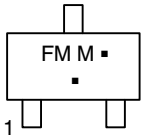


SC–70 (SOT–323)
CASE 419
STYLE 3



MARKING DIAGRAM



FM = Device Code
M = Date Code*
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

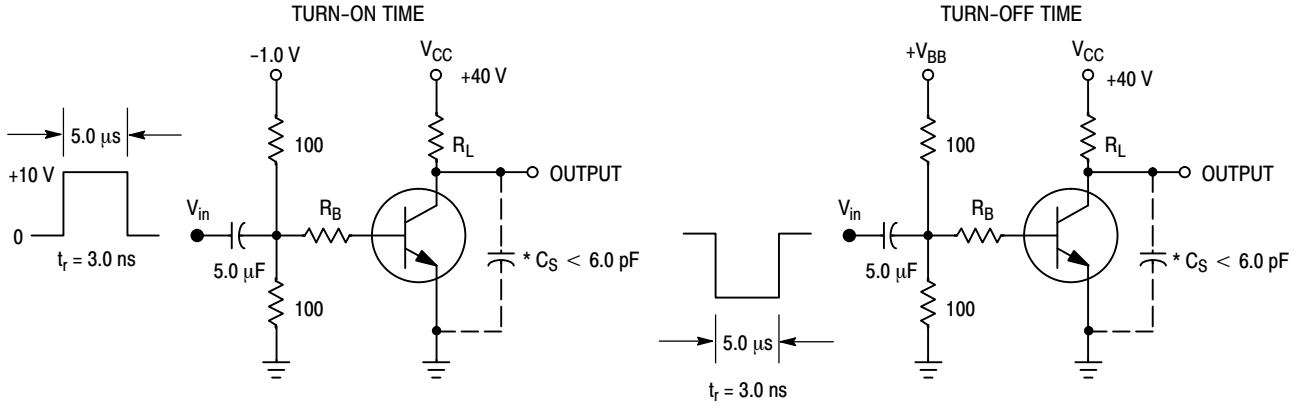
Device	Package	Shipping†
MMBTA56WT1G	SC–70 (Pb–Free)	3,000 / Tape & Reel
SMMBTA56WT1G	SC–70 (Pb–Free)	3,000 / Tape & Reel
SMMBTA56WT3G	SC–70 (Pb–Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (Note 1) (I_C = −1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	−80	−	Vdc
Emitter−Base Breakdown Voltage (I_E = −100 μAdc, I_C = 0)	$V_{(BR)EBO}$	−4.0	−	Vdc
Collector Cutoff Current (V_{CE} = −60 Vdc, I_B = 0)	I_{CES}	−	−0.1	μAdc
Collector Cutoff Current (V_{CB} = −60 Vdc, I_E = 0) (V_{CB} = −80 Vdc, I_E = 0)	I_{CBO}	− −	− −0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = −10 mAdc, V_{CE} = −1.0 Vdc) (I_C = −100 mAdc, V_{CE} = −1.0 Vdc)	h_{FE}	100 100	− −	−
Collector−Emitter Saturation Voltage (I_C = −100 mAdc, I_B = −10 mAdc)	$V_{CE(sat)}$	−	−0.25	Vdc
Base−Emitter On Voltage (I_C = −100 mAdc, V_{CE} = −1.0 Vdc)	$V_{BE(on)}$	−	−1.2	Vdc
SMALL−SIGNAL CHARACTERISTICS				
Current−Gain − Bandwidth Product (Note 2) (I_C = −100 mAdc, V_{CE} = −1.0 Vdc, f = 100 MHz)	f_T	50	−	MHz

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
2. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.



*Total Shunt Capacitance of Test Jig and Connectors
For PNP Test Circuits, Reverse All Voltage Polarities

Figure 1. Switching Time Test Circuits

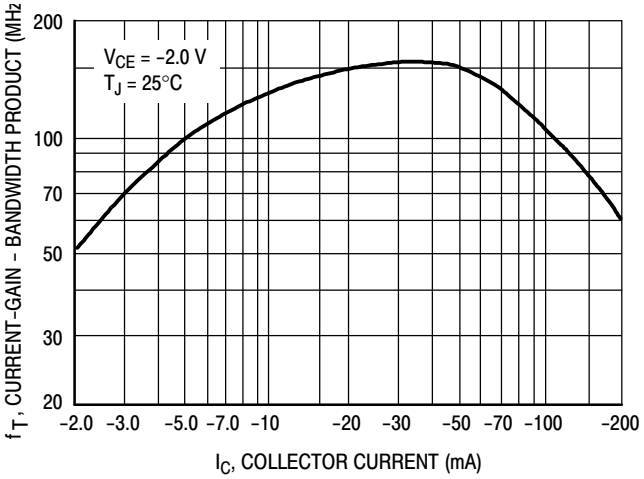


Figure 2. Current−Gain — Bandwidth Product

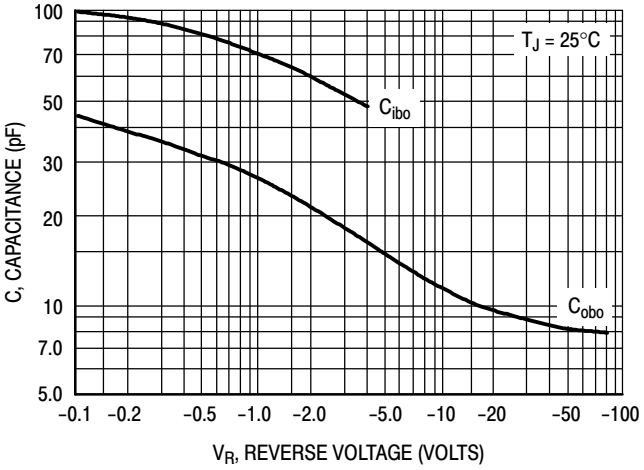


Figure 3. Capacitance

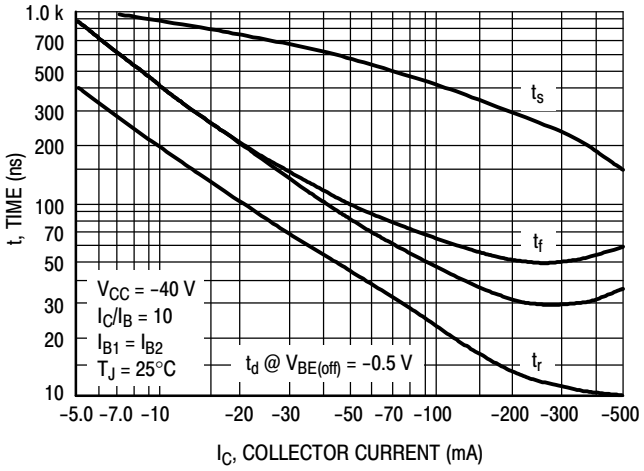


Figure 4. Switching Time

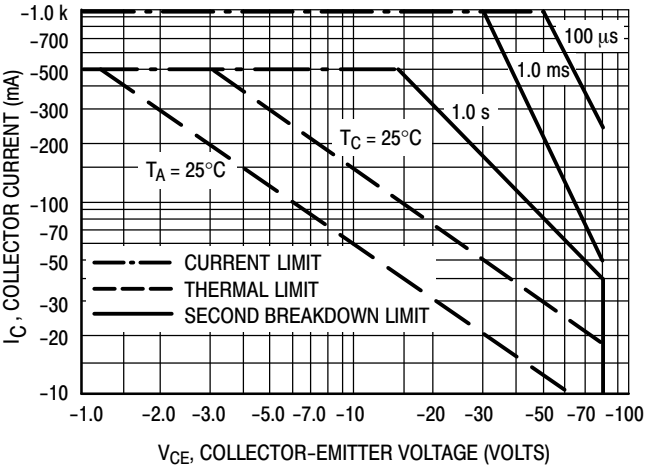


Figure 5. Active−Region Safe Operating Area

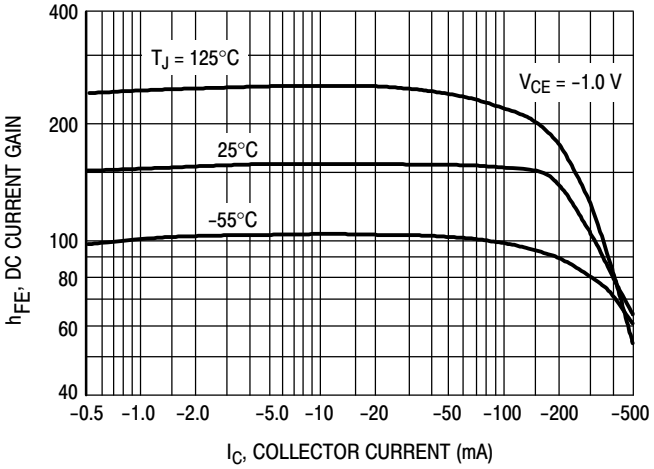


Figure 6. DC Current Gain

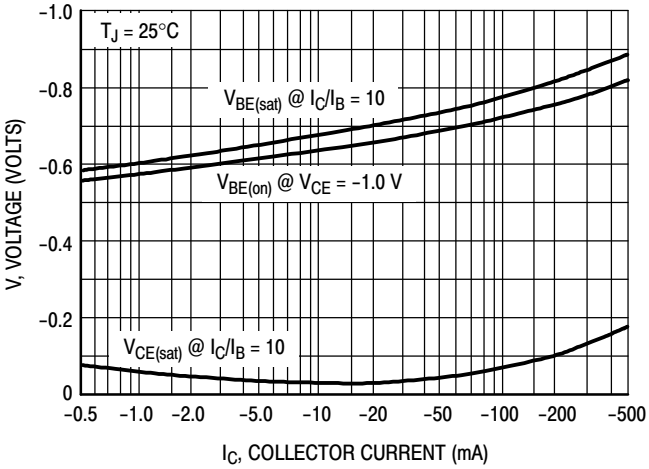


Figure 7. “ON” Voltages

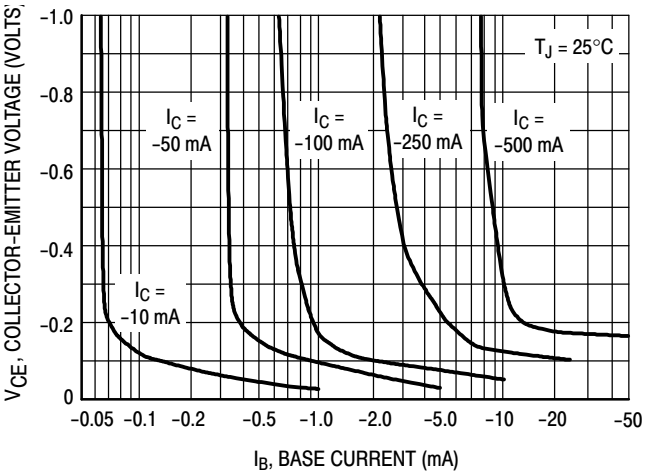


Figure 8. Collector Saturation Region

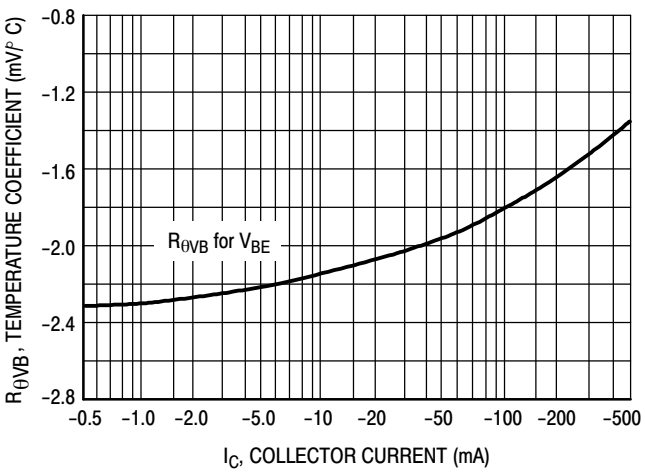
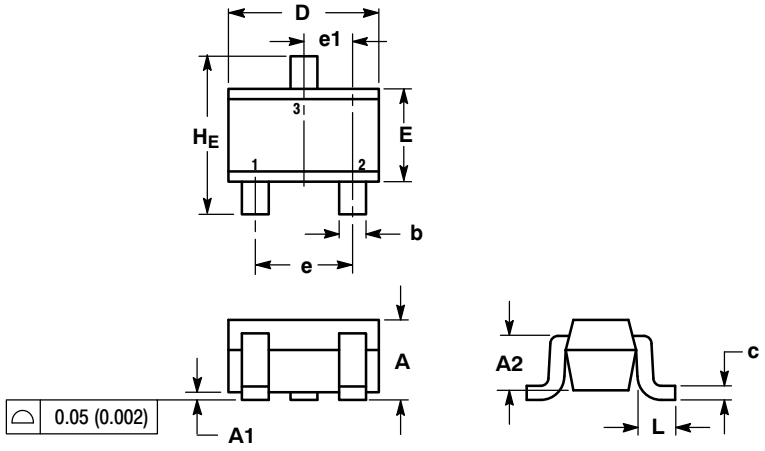


Figure 9. Base−Emitter Temperature Coefficient

PACKAGE DIMENSIONS

SC−70 (SOT−323)
CASE 419−04
ISSUE N

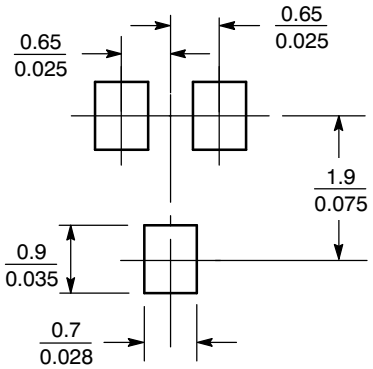


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2		0.70 REF			0.028 REF	
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1		0.65 BSC			0.026 BSC	
L	0.20	0.38	0.56	0.008	0.015	0.022
H_E	2.00	2.10	2.40	0.079	0.083	0.095

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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