MMSF2P02E

Preferred Device

Power MOSFET 2 Amps, 20 Volts

P–Channel SO–8

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided
- I_{DSS} Specified at Elevated Temperature

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted) (Note 1.)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Gate–to–Source Voltage – Continuous	V_{GS}	± 20	Vdc
Drain Current – Continuous @ T_A = 25°C (Note 2.) – Continuous @ T_A = 100°C – Single Pulse ($t_p \leq 10\ \mu s$)	 I_D I_D I_{DM}	 2.5 1.7 13	 Adc Apk
Total Power Dissipation @ T_A = 25°C (Note 2.)	P_D	2.5	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 20 Vdc, V_{GS} = 5.0 Vdc, I_L = 6.0 Apk, L = 12 mH, R_G = 25 Ω)	E_{AS}	216	mJ
Thermal Resistance – Junction to Ambient (Note 2.)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

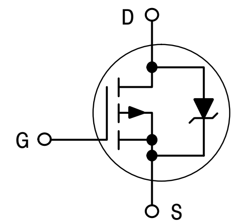
1. Negative sign for P–Channel device omitted for clarity.
2. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided), 10 sec. max.

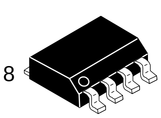
ON Semiconductor™

http://onsemi.com

2 AMPERES
20 VOLTS
$R_{DS(on)}$ = 250 mΩ

P–Channel





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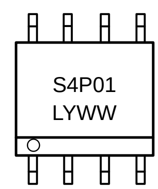
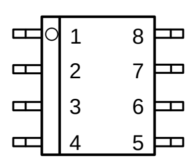
SO–8
CASE 751
STYLE 13

MARKING DIAGRAM



L = Location Code
Y = Year
WW = Work Week

PIN ASSIGNMENT



Top View

ORDERING INFORMATION

Device	Package	Shipping
MMSF2P02ER2	SO–8	2500 Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Note 1.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	20	–	–	Vdc
Temperature Coefficient (Positive)			–	24.7	–	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	–	–	1.0	μAdc
(V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			–	–	10	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	–	–	100	nAdc
ON CHARACTERISTICS (Note 3.)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	2.0	3.0	Vdc
Threshold Temperature Coefficient (Negative)				4.7	–	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.0 Adc)		$R_{DS(on)}$	–	0.19	0.25	Ohm
(V_{GS} = 4.5 Vdc, I_D = 1.0 Adc)			–	0.3	0.4	
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.0 Adc)		g_{FS}	1.0	2.8	–	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	340	475	pF
Output Capacitance		C_{oss}	–	220	300	
Transfer Capacitance		C_{rss}	–	75	150	
SWITCHING CHARACTERISTICS (Note 4.)						
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 5.0 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	–	20	40	ns
Rise Time		t_r	–	40	80	
Turn–Off Delay Time		$t_{d(off)}$	–	53	106	
Fall Time		t_f	–	41	82	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	–	13	26	ns
Rise Time		t_r	–	29	58	
Turn–Off Delay Time		$t_{d(off)}$	–	30	60	
Fall Time		t_f	–	28	56	
Gate Charge	(V_{DS} = 16 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	–	10	15	nC
		Q_1	–	1.1	–	
		Q_2	–	3.3	–	
		Q_3	–	2.5	–	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (Note 3.)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	–	1.5	2.0	Vdc
Reverse Recovery Time	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	–	34	64	ns
		t_a	–	18	–	
		t_b	–	16	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.035	–	μC

1. Negative sign for P–Channel device omitted for clarity.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

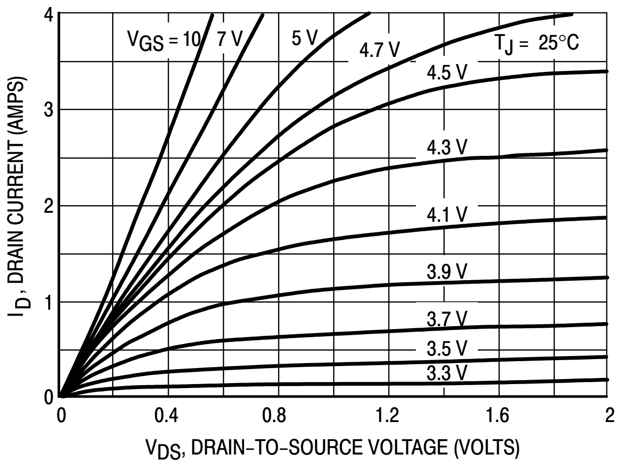


Figure 1. On−Region Characteristics

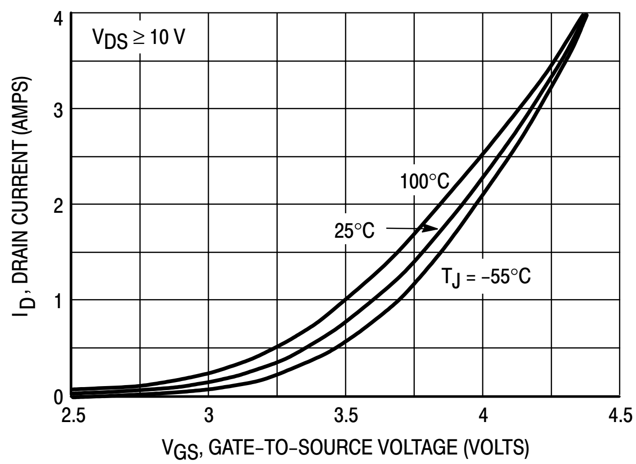


Figure 2. Transfer Characteristics

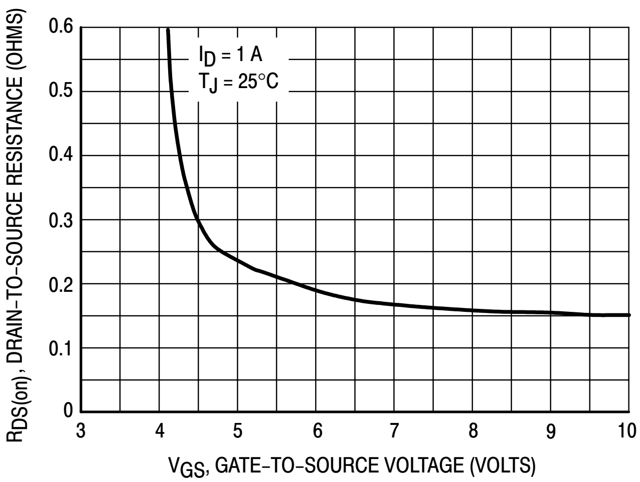


Figure 3. On−Resistance versus Gate−to−Source Voltage

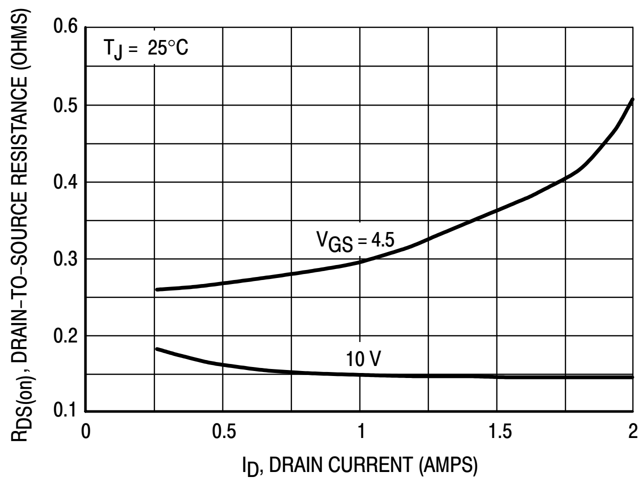


Figure 4. On−Resistance versus Drain Current and Gate Voltage

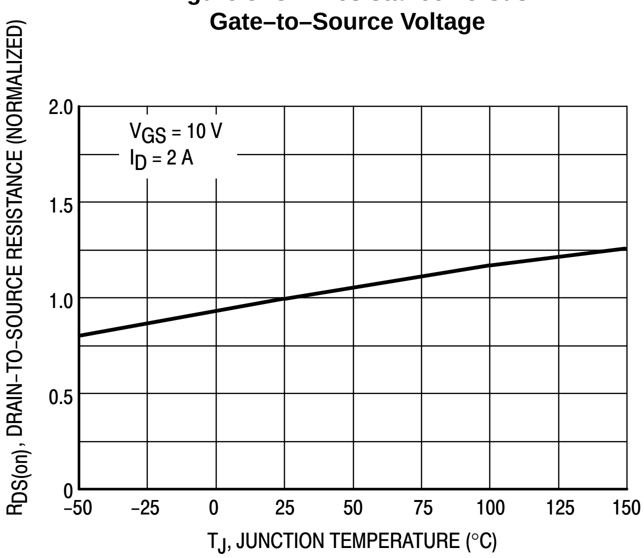


Figure 5. On−Resistance Variation with Temperature

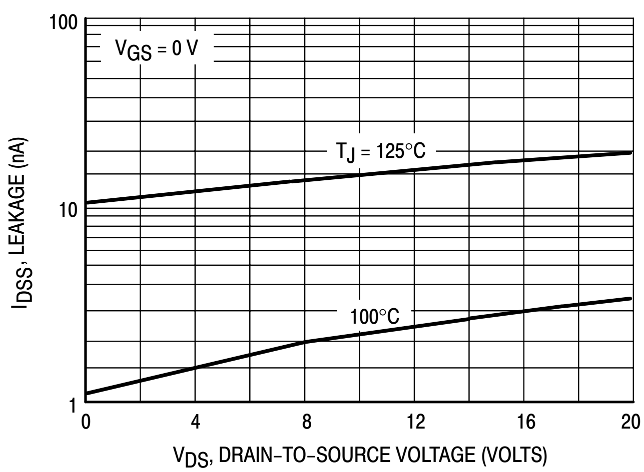


Figure 6. Drain−to−Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}
R_G = the gate drive resistance
and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

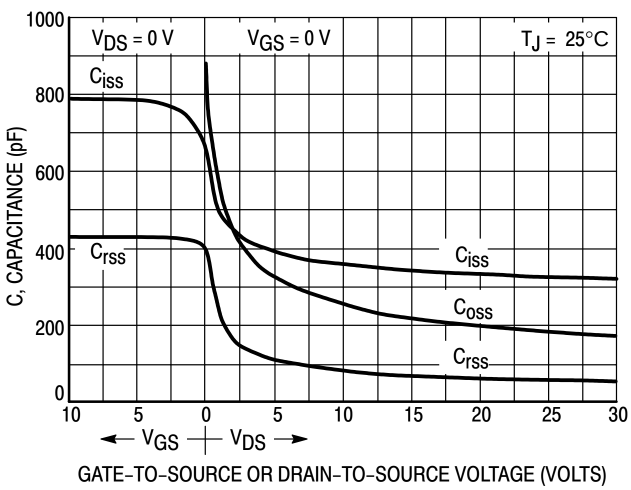


Figure 7. Capacitance Variation

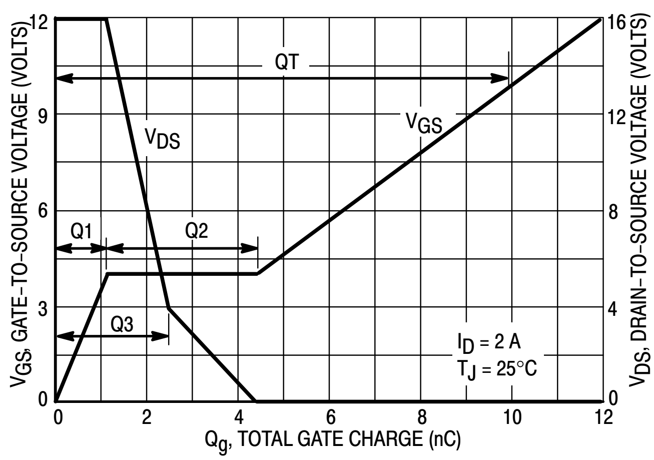


Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

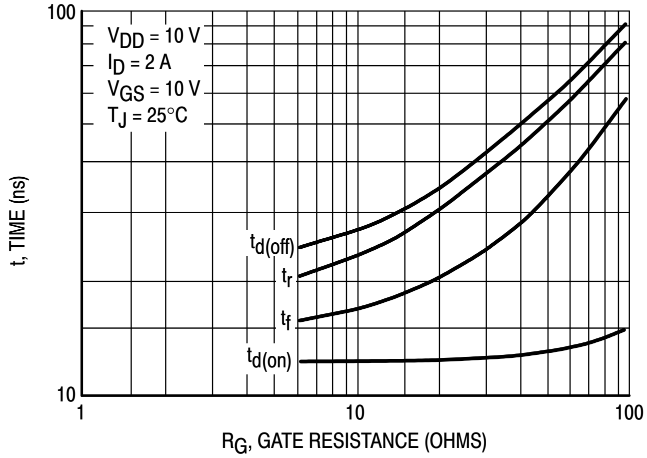


Figure 9. Resistive Switching Time Variation versus Gate Resistance

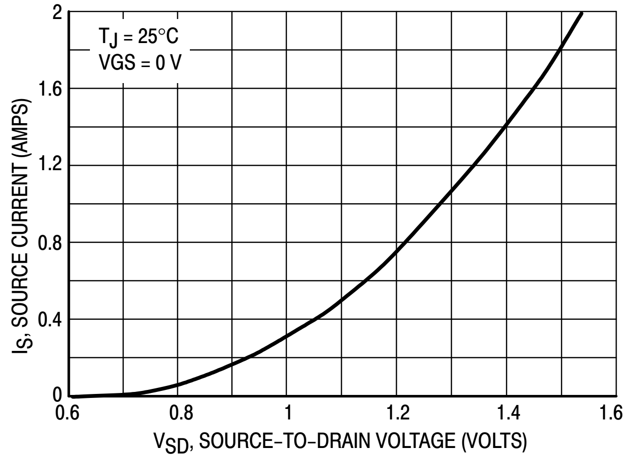


Figure 10. Diode Forward Voltage versus Current

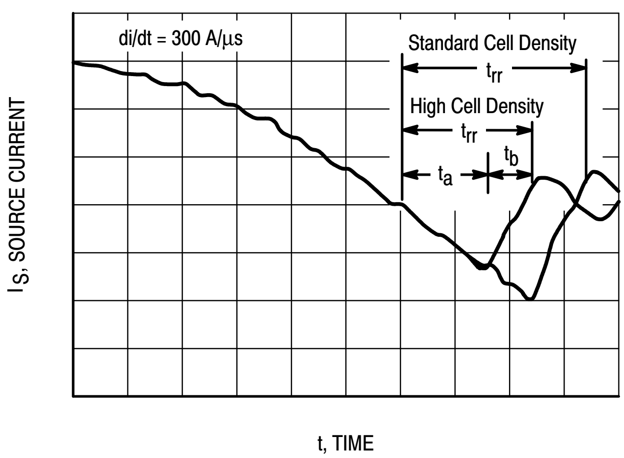


Figure 11. Reverse Recovery Time (t_{rr})

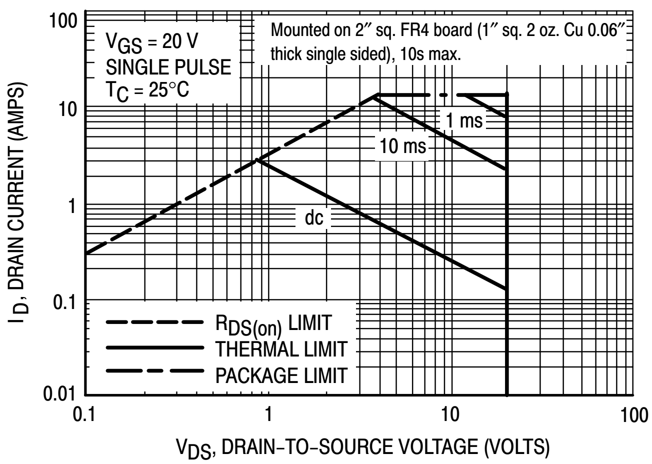


Figure 12. Maximum Rated Forward Biased Safe Operating Area

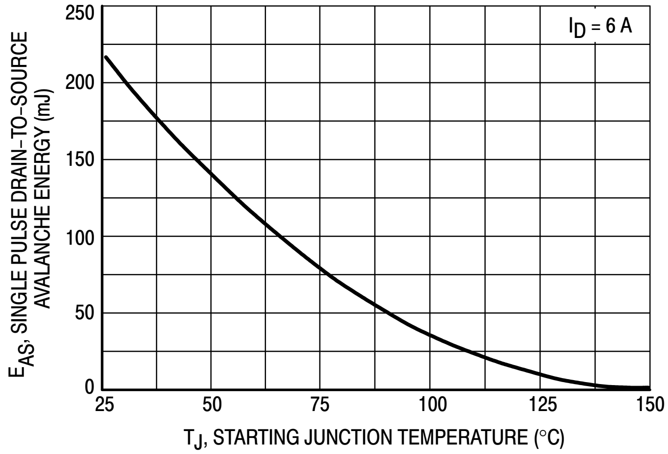


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

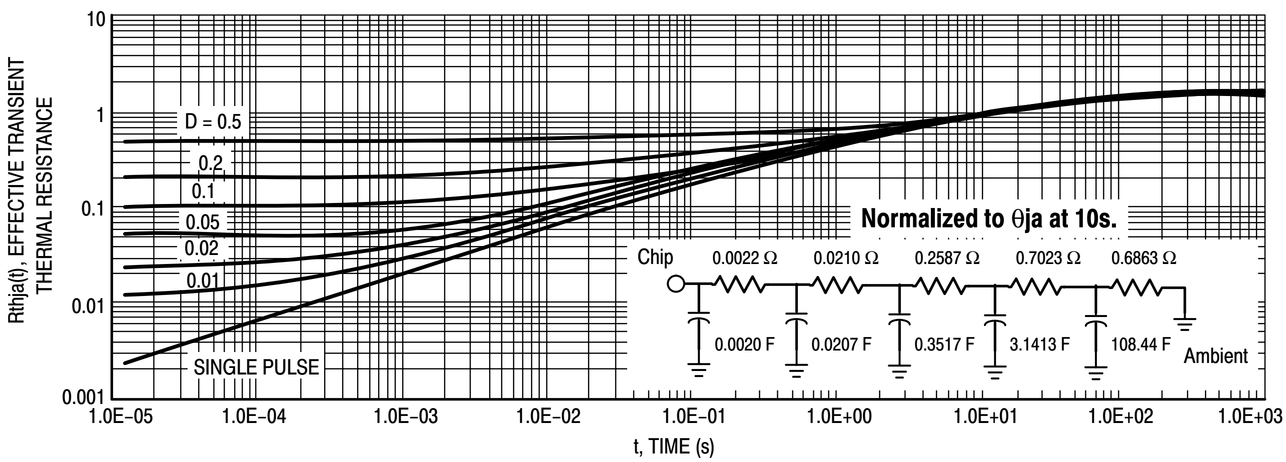


Figure 14. Thermal Response

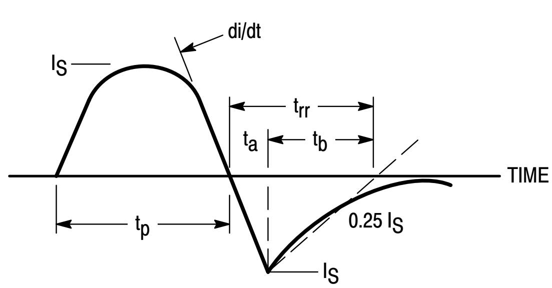
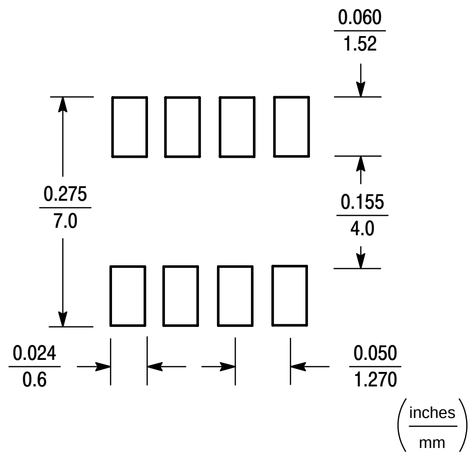


Figure 15. Diode Reverse Recovery Waveform

INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.



SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, T_A. Using the values provided on the data sheet for the SO–8 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 2.5 Watts.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 13 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

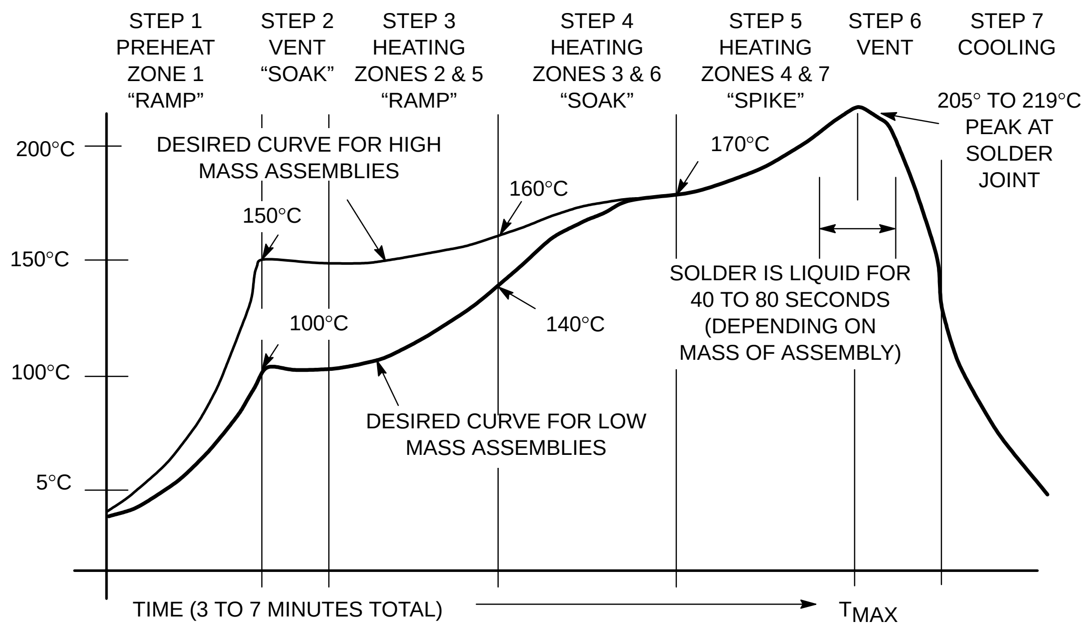
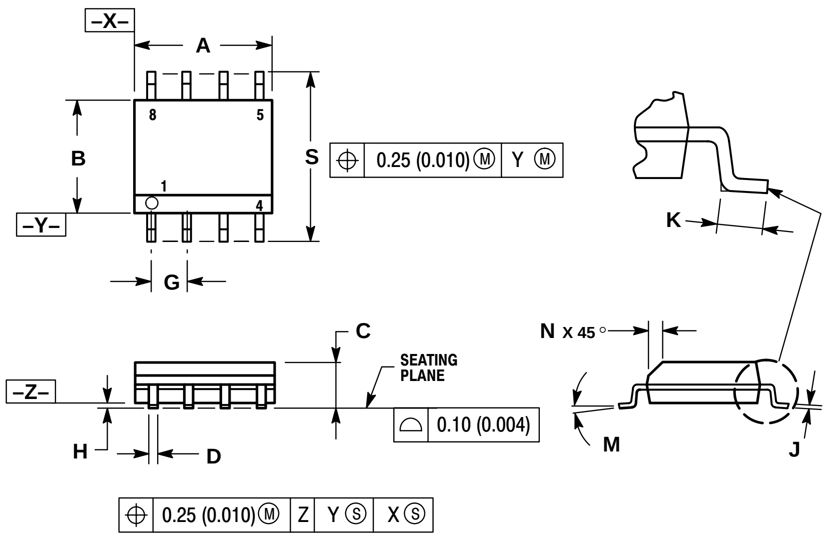


Figure 16. Typical Solder Heating Profile

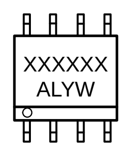
PACKAGE DIMENSIONS

SO–8
CASE 751–07
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244



STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

Notes

Notes

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