

Switching Transistor

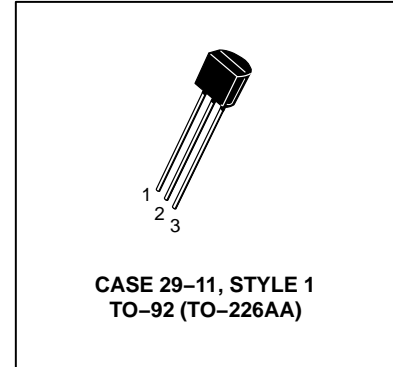
NPN Silicon

MPS3646

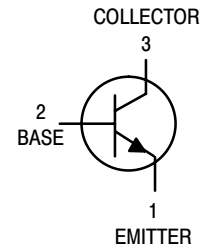
ON Semiconductor Preferred Device

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	15	Vdc
Collector–Emitter Voltage	V_{CES}	40	Vdc
Collector–Base Voltage	V_{CBO}	40	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous	I_C	300	mAdc
— 10 μ s Pulse		500	
Total Device Dissipation @ $T_A = 25^\circ\text{C}$	P_D	625	mW
Derate above 25°C		5.0	mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$	P_D	1.5	Watts
Derate above 25°C		12	mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$



CASE 29-11, STYLE 1
TO-92 (TO-226AA)



THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage	($I_C = 100 \mu\text{Adc}, V_{BE} = 0$)	$V_{(BR)CES}$	40	—	Vdc
Collector–Emitter Sustaining Voltage ⁽¹⁾	($I_C = 10 \text{ mAdc}, I_B = 0$)	$V_{CEO(sus)}$	15	—	Vdc
Collector–Base Breakdown Voltage	($I_C = 100 \mu\text{Adc}, I_E = 0$)	$V_{(BR)CBO}$	40	—	Vdc
Emitter–Base Breakdown Voltage	($I_E = 100 \mu\text{Adc}, I_C = 0$)	$V_{(BR)EBO}$	5.0	—	Vdc
Collector Cutoff Current	($V_{CE} = 20 \text{ Vdc}, V_{BE} = 0$) ($V_{CE} = 20 \text{ Vdc}, V_{BE} = 0, T_A = 65^\circ\text{C}$)	I_{CES}	—	0.5 3.0	μAdc

ON CHARACTERISTICS⁽¹⁾

DC Current Gain	($I_C = 30 \text{ mAdc}, V_{CE} = 0.4 \text{ Vdc}$) ($I_C = 100 \text{ mAdc}, V_{CE} = 0.5 \text{ Vdc}$) ($I_C = 300 \text{ mA}, V_{CE} = 1.0 \text{ Vdc}$)	h_{FE}	30 25 15	120 — —	—
Collector–Emitter Saturation Voltage	($I_C = 30 \text{ mAdc}, I_B = 3.0 \text{ mAdc}$) ($I_C = 100 \text{ mAdc}, I_B = 10 \text{ mAdc}$) ($I_C = 300 \text{ mAdc}, I_B = 30 \text{ mAdc}$) ($I_C = 30 \text{ mA}, I_B = 3.0 \text{ mA}, T_A = 65^\circ\text{C}$)	$V_{CE(sat)}$	— — — —	0.2 0.28 0.5 0.3	Vdc
Base–Emitter Saturation Voltage	($I_C = 30 \text{ mAdc}, I_B = 3.0 \text{ mAdc}$) ($I_C = 100 \text{ mAdc}, I_B = 10 \text{ mAdc}$) ($I_C = 300 \text{ mAdc}, I_B = 30 \text{ mA}$)	$V_{BE(sat)}$	0.73 — —	0.95 1.2 1.7	Vdc

1. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$; Duty Cycle $\leq 2.0\%$.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Max	Unit
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain — Bandwidth Product ($I_C = 30\text{ mA}$, $V_{CE} = 10\text{ V}$, $f = 100\text{ MHz}$)	f_T	350	—	MHz
Output Capacitance ($V_{CB} = 5.0\text{ V}$, $I_E = 0$, $f = 1.0\text{ MHz}$)	C_{obo}	—	5.0	pF
Input Capacitance ($V_{EB} = 0.5\text{ V}$, $I_C = 0$, $f = 1.0\text{ MHz}$)	C_{ibo}	—	9.0	pF

SWITCHING CHARACTERISTICS

Turn-On Time	$(V_{CC} = 10\text{ V}$, $I_C = 300\text{ mA}$, $I_{B1} = 30\text{ mA}$) (Figure 1)	t_{on}	—	18	ns
Delay Time		t_d	—	10	ns
Rise Time		t_r	—	15	ns
Turn-Off Time	$(V_{CC} = 10\text{ V}$, $I_C = 300\text{ mA}$, $I_{B1} = I_{B2} = 30\text{ mA}$) (Figure 1)	t_{off}	—	28	ns
Fall Time		t_f	—	15	ns
Storage Time ($V_{CC} = 10\text{ V}$, $I_C = 10\text{ mA}$, $I_{B1} = I_{B2} = 10\text{ mA}$) (Figure 2)		t_s	—	18	ns

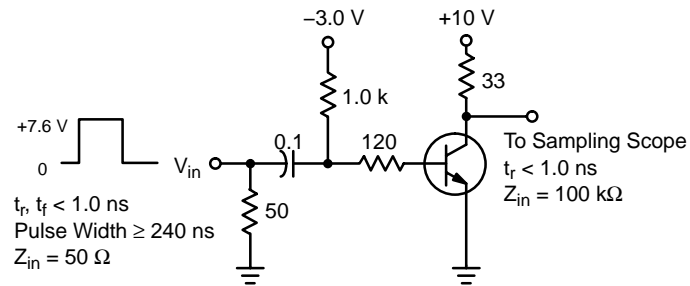


Figure 1. Switching Time Test Circuit

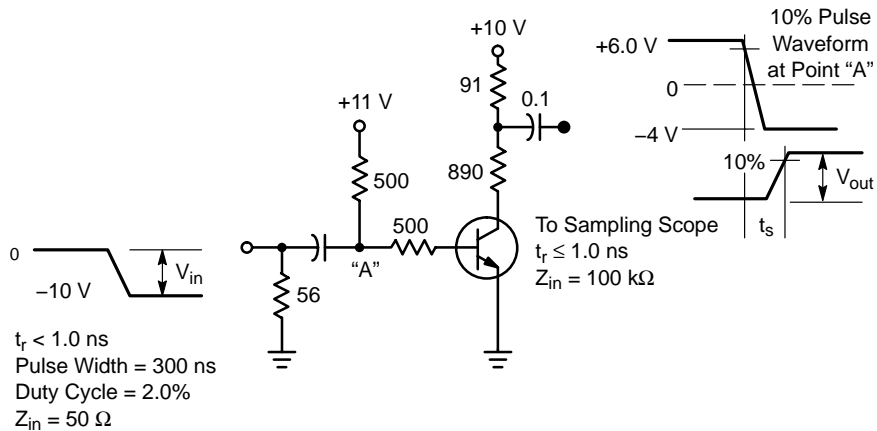


Figure 2. Charge Storage Time Test Circuit

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CURRENT GAIN CHARACTERISTICS

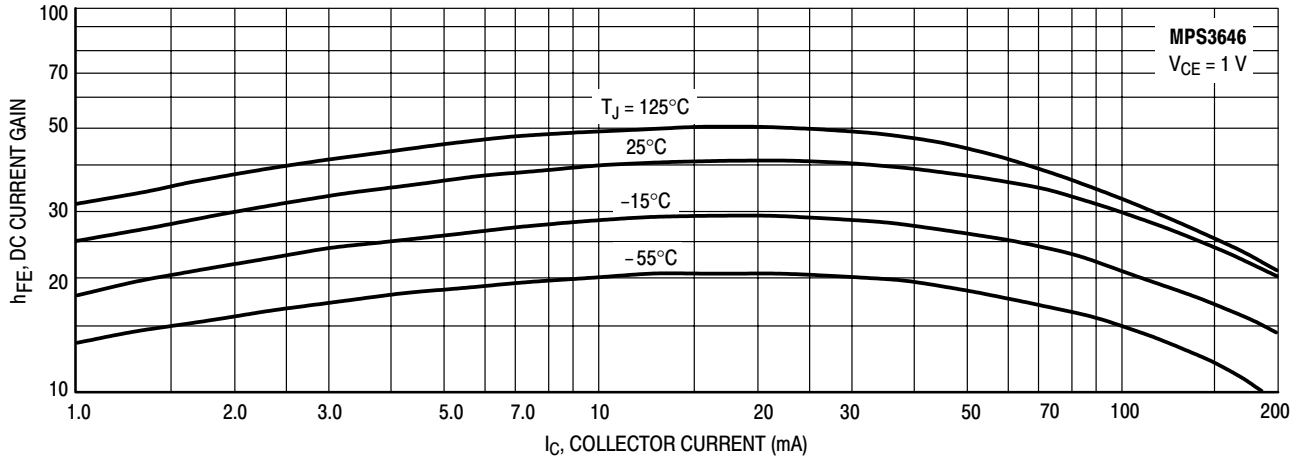


Figure 3. Minimum Current Gain

“ON” CONDITION CHARACTERISTICS

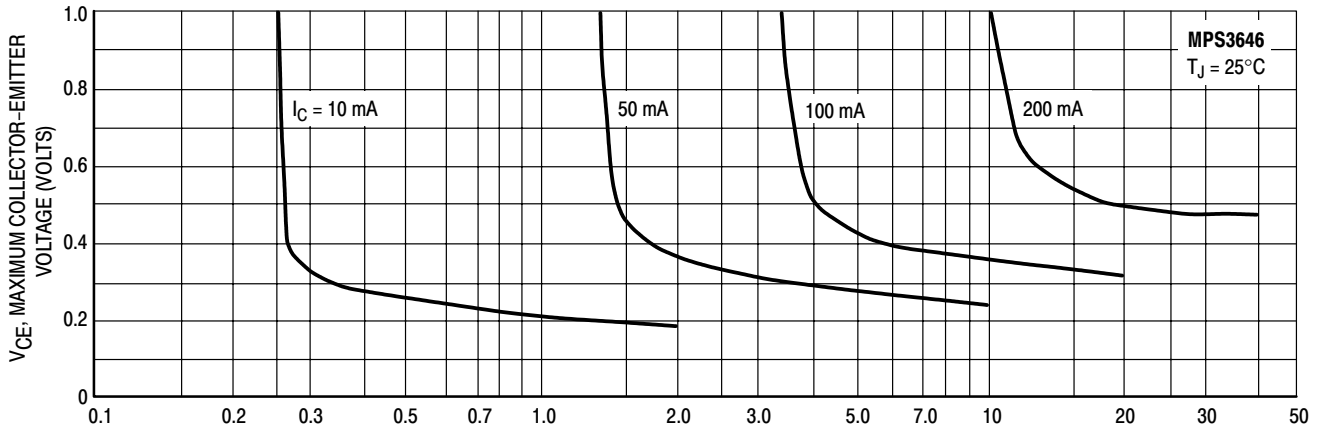


Figure 4. Collector Saturation Region

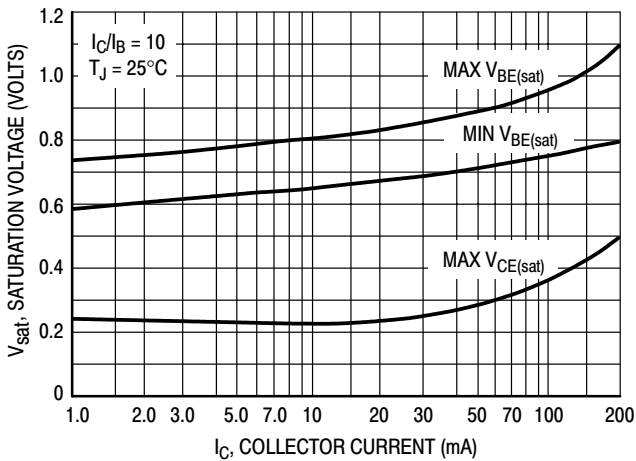


Figure 5. Saturation Voltage Limits

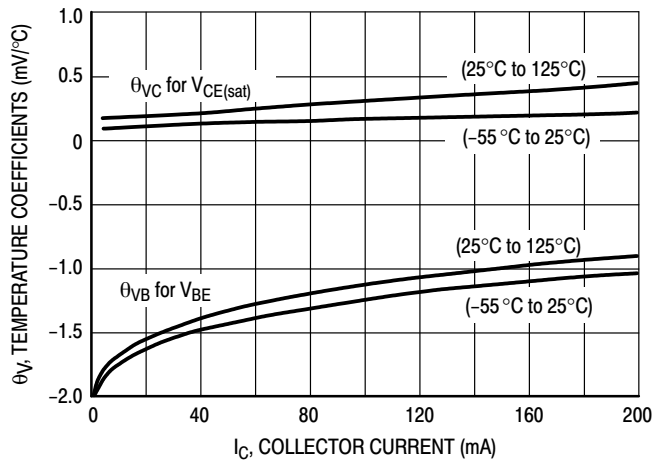


Figure 6. Temperature Coefficients

DYNAMIC CHARACTERISTICS

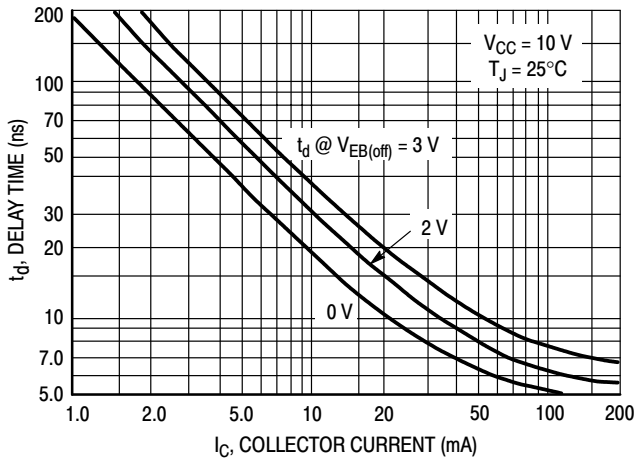


Figure 7. Delay Time

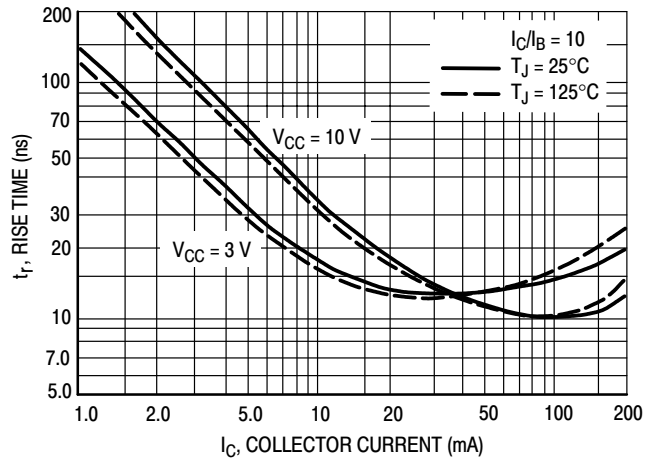


Figure 8. Rise Time

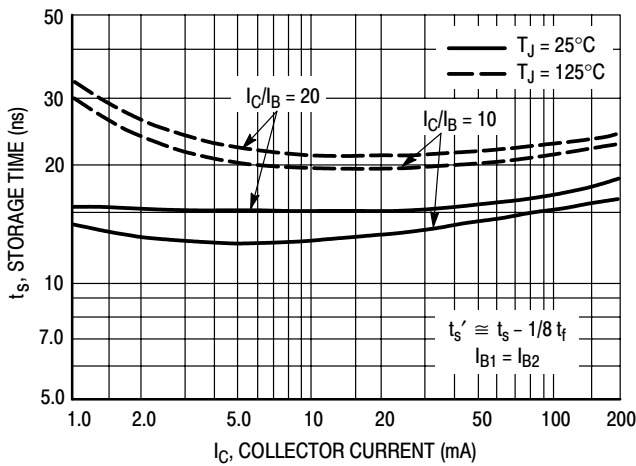


Figure 9. Storage Time

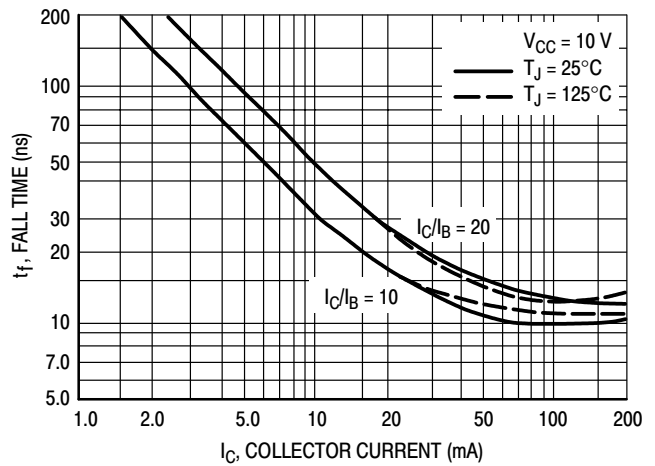


Figure 10. Fall Time

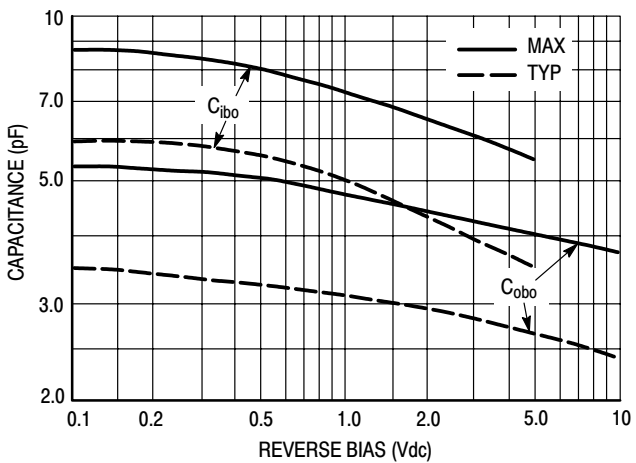


Figure 11. Junction Capacitance

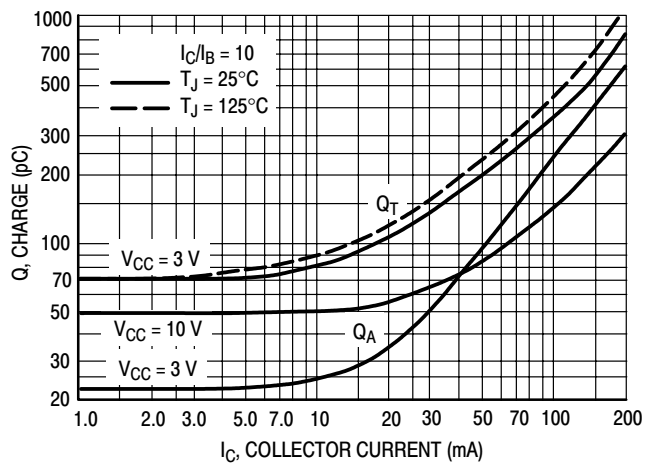
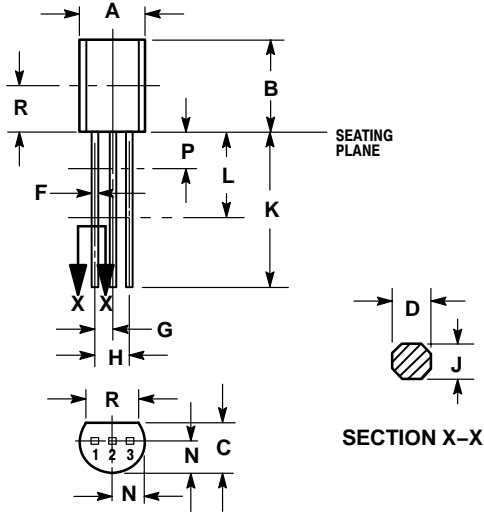


Figure 12. Maximum Charge Data

MPS3646

PACKAGE DIMENSIONS

CASE 029-11 (TO-226AA) ISSUE AD



STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSIONS D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.457	0.533
F	0.016	0.019	0.407	0.482
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---

Notes

Notes

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