

NL27WZ86

Dual 2-Input Exclusive-OR Gate

The NL27WZ86 is a high performance dual 2-input Exclusive-OR Gate operating from a 1.65 V to 5.5 V supply.

- Extremely High Speed: t_{PD} 2.4 ns (typical) at $V_{CC} = 5.0$ V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs and Outputs
- LVTTL Compatible – Interface Capability With 5.0 V TTL Logic with $V_{CC} = 3.0$ V
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- Replacement for NC7WZ86

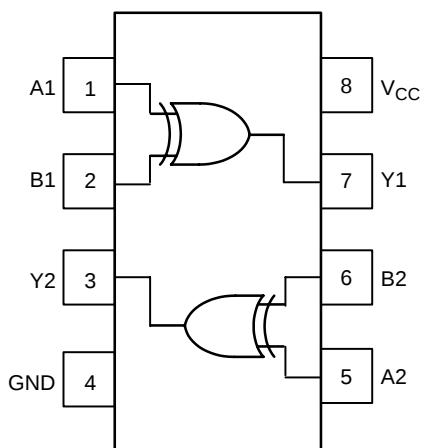


Figure 1. Pinout (Top View)

PIN ASSIGNMENT

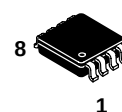
Pin	Function
1	A1
2	B1
3	Y2
4	GND
5	A2
6	B2
7	Y1
8	V_{CC}



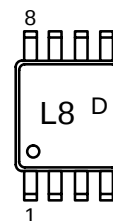
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM



US8
US SUFFIX
CASE 493



D = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

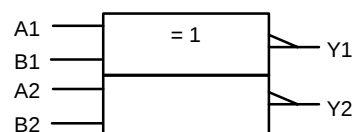


Figure 2. Logic Symbol

FUNCTION TABLE

Input		Output $Y = A + B$
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	− 0.5 to + 7.0	V
V _I	DC Input Voltage	− 0.5 to + 7.0	V
V _O	DC Output Voltage	− 0.5 to + 7.0	V
I _{IK}	DC Input Diode Current V _I < GND	− 50	mA
I _{OK}	DC Output Diode Current V _O < GND	− 50	mA
I _O	DC Output Sink Current	± 50	mA
I _{CC}	DC Supply Current per Supply Pin	± 100	mA
I _{GND}	DC Ground Current per Ground Pin	± 100	mA
T _{STG}	Storage Temperature Range	− 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature under Bias	+ 150	°C
θ _{JA}	Thermal Resistance (Note 1)	250	°C/W
P _D	Power Dissipation in Still Air at 85°C	250	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V _I	Input Voltage (Note 5)	0	5.5	V
V _O	Output Voltage (HIGH or LOW State)	0	5.5	V
T _A	Operating Free-Air Temperature	− 40	+ 125	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _{CC} = 1.8 V ± 0.15 V V _{CC} = 2.5 V ± 0.2 V V _{CC} = 3.0 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0 0 0	20 20 10 5	ns/V

5. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Unit	Condition
			Min	Typ	Max	Min	Max		
V _{IH}	High-Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.75 V _{CC} 0.7 V _{CC}			0.75 V _{CC} 0.7 V _{CC}		V	
V _{IL}	Low-Level Input Voltage	1.65 to 1.95 2.3 to 5.5			0.25 V _{CC} 0.3 V _{CC}		0.25 V _{CC} 0.3 V _{CC}	V	
V _{OH}	High-Level Output Voltage V _{IN} = V _{IH}	1.65 1.8 2.3 3.0 4.5	1.55 1.7 2.2 2.9 4.4	1.65 1.8 2.3 3.0 4.5		1.55 1.7 2.2 2.9 4.4		V	I _{OH} = -100 μA
		1.65 2.3 3.0 3.0 4.5	1.29 1.9 2.4 2.3 3.8	1.52 2.15 2.80 2.68 4.20		1.29 1.9 2.4 2.3 3.8		V	I _{OH} = -4 mA I _{OH} = -8 mA I _{OH} = -16 mA I _{OH} = -24 mA I _{OH} = -32 mA
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IL}	1.65 1.8 2.3 3.0 4.5		0.0 0.0 0.0 0.0 0.0	0.1 0.1 0.1 0.1 0.1		0.1 0.1 0.1 0.1 0.1	V	I _{OL} = 100 μA
		1.65 2.3 3.0 3.0 4.5		0.08 0.10 0.15 0.22 0.22	0.24 0.30 0.40 0.55 0.55		0.24 0.30 0.40 0.55 0.55	V	I _{OL} = 4 mA I _{OL} = 8 mA I _{OL} = 16 mA I _{OL} = 24 mA I _{OL} = 32 mA
I _{IN}	Input Leakage Current	0 to 5.5			±1.0		±1.0	μA	0 V ≤ V _{IN} ≤ 5.5 V
I _{OFF}	Power Off Leakage Current	0.0			1.0		10	μA	V _{IN} or V _{OUT} = 5.5 V
I _{CC}	Quiescent Supply Current	1.65 to 5.5			1.0		10	μA	V _{IN} = 5.5 V, GND

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 3.0 ns

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation Delay (Figure 3 and 4)	R _L = 1 MΩ, C _L = 15 pF	1.8 ± 0.15	2.0	7.9	9.0	2.0	10.5	ns
		R _L = 1 MΩ, C _L = 15 pF	2.5 ± 0.2	1.2	4.1	7.0	1.2	7.5	
		R _L = 1 MΩ, C _L = 15 pF	3.3 ± 0.3	0.8	3.0	4.8	0.8	5.2	
		R _L = 500 Ω, C _L = 50 pF		1.2	3.8	5.4	1.2	5.9	
		R _L = 1 MΩ, C _L = 15 pF	5.0 ± 0.5	0.5	2.2	3.5	0.5	3.8	
		R _L = 500 Ω, C _L = 50 pF		0.8	2.9	4.2	1.0	4.6	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	2.5	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	9	pF
		10 MHz, V _{CC} = 5.5 V, V _I = 0 V or V _{CC}	11	

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NL27WZ86

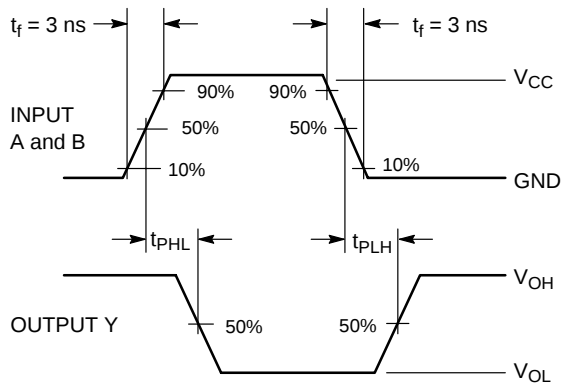
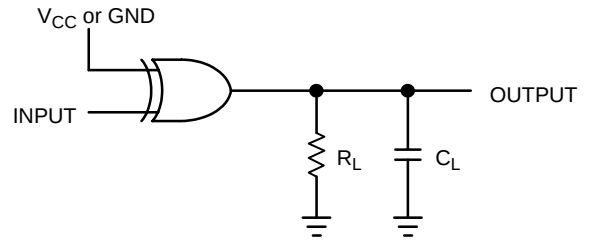


Figure 3. Switching Waveform



A 1-MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

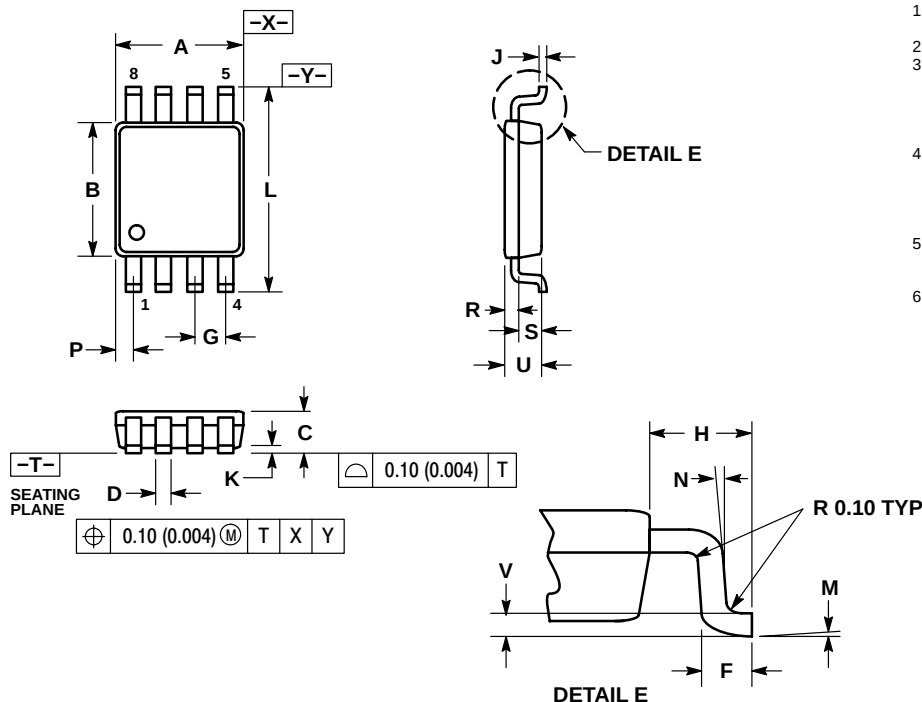
DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type	Tape and Reel Size
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape and Reel Suffix		
NL27WZ86US	NL	2	7	WZ	86	US		US8	178 mm, 3000 Units

NL27WZ86

PACKAGE DIMENSIONS

US8
US SUFFIX
CASE 493-02
ISSUE A

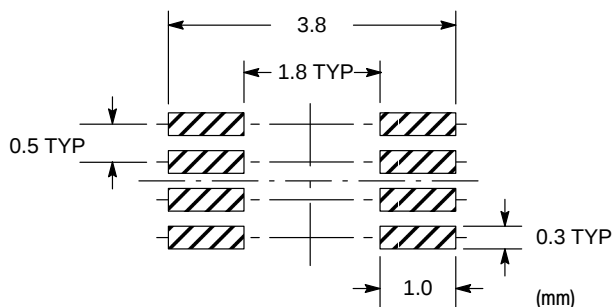


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800 °).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.002 °).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0 °	6 °	0 °	6 °
N	5 °	10 °	5 °	10 °
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.