

NLAS4685

Ultra-Low Resistance Dual SPDT Analog Switch

The NLAS4685 is an advanced CMOS analog switch fabricated in Sub-micron silicon gate CMOS technology. The device is a dual Independent Single Pole Double Throw (SPDT) switch featuring Ultra-Low R_{ON} of $0.8\ \Omega$, for the Normally Closed (NC) switch and for the Normally Opened switch (NO) at 2.7 V.

The part also features guaranteed Break Before Make switching, assuring the switches never short the driver.

The NLAS4685 is available in a 2.0×1.5 mm bumped die array, with a 3×4 arrangement of solder bumps. The pitch of the solder bumps is 0.5 mm for easy handling.

Features

- Ultra-Low R_{ON} , $< 0.8\ \Omega$ at 2.7 V
- Threshold Adjusted to Function with 1.8 V Control at $V_{CC} = 2.7\text{--}3.3$ V
- Single Supply Operation from 1.8–5.5 V
- Tiny 2×1.5 mm Bumped Die
- Low Crosstalk, < 81 dB at 100 kHz
- Full $0\text{--}V_{CC}$ Signal Handling Capability
- High Isolation, -65 dB at 100 kHz
- Low Standby Current, < 50 nA
- Low Distortion, $< 0.14\%$ THD
- R_{ON} Flatness of $0.15\ \Omega$
- Pin for Pin Replacement for MAX4685

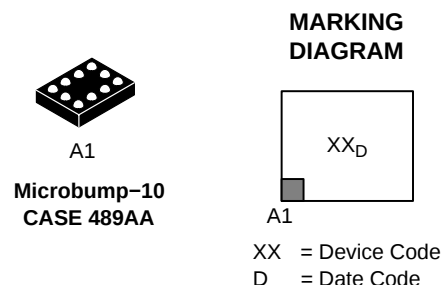
Applications

- Cell Phone
- Speaker Switching
- Power Switching (Up to 100 mA)
- Modems
- Automotive

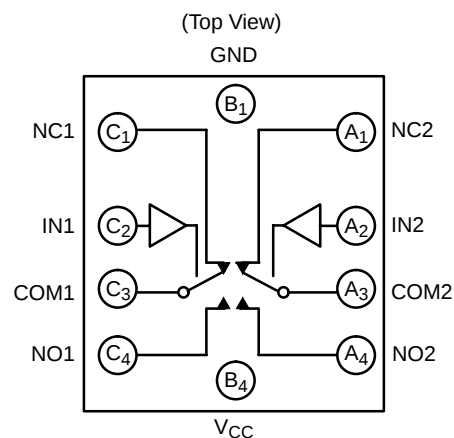


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PIN CONNECTIONS AND LOGIC DIAGRAM



FUNCTION TABLE

IN 1, 2	NO 1, 2	NC 1, 2
0	OFF	ON
1	ON	OFF

ORDERING INFORMATION

Device	Package	Shipping
NLAS4685	Microbump-10	3000/Tape & Reel

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Positive DC Supply Voltage	− 0.5 to + 7.0	V
V _{IS}	Analog Input Voltage (V _{NO} , V _{NC} , or V _{COM}) (Note 1)	− 0.5 ≤ V _{IS} ≤ V _{CC} + 0.5	V
V _{IN}	Digital Select Input Voltage	− 0.5 ≤ V _I ≤ + 7.0	V
I _{IK}	DC Current, Into or Out of Any Pin	± 50	mA

1. Signal voltage on NC, NO, and COM exceeding V_{CC} or GND are clamped by the internal diodes. Limit forward diode current to maximum current rating.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	1.8	5.5	V
V _{IN}	Digital Select Input Voltage	GND	5.5	V
V _{IS}	Analog Input Voltage (NC, NO, COM)	GND	V _{CC}	V
T _A	Operating Temperature Range	− 55	+ 125	°C
t _r , t _f	Input Rise or Fall Time, SELECT	V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V		ns/V
		0	100	
		0	20	

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC} ± 10%	Guaranteed Limit			Unit
				− 55°C to 25°C	< 85°C	< 125°C	
V _{IH}	Minimum High-Level Input Voltage, Select Inputs		2.0	1.4	1.4	1.4	V
			2.5	1.4	1.4	1.4	
			3.0	1.4	1.4	1.4	
			5.0	2.0	2.0	2.0	
V _{IL}	Maximum Low-Level Input Voltage, Select Inputs		2.0	0.5	0.5	0.5	V
			2.5	0.5	0.5	0.5	
			3.0	0.5	0.5	0.5	
			5.0	0.8	0.8	0.8	
I _{IN}	Maximum Input Leakage Current, Select Inputs	V _{IN} = 5.5 V or GND	5.5	± 1.0	± 1.0	± 1.0	µA
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V or GND	0	± 10	± 10	± 10	µA
I _{CC}	Maximum Quiescent Supply Current	Select and V _{IS} = V _{CC} or GND	5.5	± 50	± 200	± 200	nA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Condition	V _{CC} ±10%	Guaranteed Maximum Limit						Unit
				−55°C to 25°C		< 85°C		< 125°C		
				Min	Max	Min	Max	Min	Max	
R _{ON} (NC, NO)	“ON” Resistance (Note 2)	V _{IN} ≥ V _{IH}	2.5		2.0		2.0		2.0	Ω
		V _{IS} = GND to V _{CC}	3.0		0.8		0.8		1.0	
		I _{INL} ≤ 100 mA	5.0		0.8		0.8		0.9	
R _{FLAT} (NC, NO)	On-Resistance Flatness (Notes 2, 4)	I _{COM} = 100 mA	2.5		0.35		0.35		0.35	Ω
		V _{IS} = 0 to V _{CC}	3.0		0.35		0.35		0.35	
			5.0		0.35		0.35		0.35	
ΔR _{ON}	On-Resistance Match Between Channels (Notes 2 and 3)	V _{IS} = 1.3 V; I _{COM} = 100 mA	2.5		0.18		0.18		0.18	Ω
		V _{IS} = 1.5 V; I _{COM} = 100 mA	3.0		0.06		0.06		0.06	
		V _{IS} = 2.8 V; I _{COM} = 100 mA	5.0		0.06		0.06		0.06	
I _{NC(OFF)} I _{NO(OFF)}	NC or NO Off Leakage Current (Figure 10)	V _{IN} = V _{IL} or V _{IH} V _{NO} or V _{NC} = 1.0 V _{COM} = 4.5 V	5.5	−1	1	−10	10	−150	150	nA
I _{COM(ON)}	COM ON Leakage Current (Figure 10)	V _{IN} = V _{IL} or V _{IH} V _{NO} 1.0 V or 4.5 V with V _{NC} floating or V _{NC} 1.0 V or 4.5 V with V _{NO} floating V _{COM} = 1.0 V or 4.5 V	5.5	−1	1	−10	10	−150	150	nA

2. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.
3. $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$ between all switches.
4. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	V _{CC} (V)	V _{IS} (V)	Guaranteed Maximum Limit						Unit	
					−55°C to 25°C			< 85°C		< 125°C		
					Min	Typ*	Max	Min	Max	Min		Max
t _{ON}	Turn-On Time	R _L = 50 Ω, C _L = 35 pF (Figures 2 and 3)	2.5 3.0 5.0	1.3 1.5 2.8			55 50 30		65 60 35		70 60 35	ns
t _{OFF}	Turn-Off Time	R _L = 50 Ω, C _L = 35 pF (Figures 2 and 3)	2.5 3.0 5.0	1.3 1.5 2.8			55 50 25		65 60 30		70 60 30	ns
t _{BBM}	Minimum Break-Before-Make Time	V _{IS} = 3.0 R _L = 300 Ω, C _L = 35 pF (Figure 1)	3.0	1.5	2	15						ns

C _{NC} Off C _{NO} Off C _{NC} On C _{NO} On	NC Off Capacitance, f = 1 MHz NO Off Capacitance, f = 1 MHz NC On Capacitance, f = 1 MHz NO On Capacitance, f = 1 MHz	Typical @ 25, $V_{CC} = 5.0$ V	$V_{CC} = 3.0$ V	pF
			208 102 547 431	

*Typical Characteristics are at 25°C.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted) (Note 6)

Symbol	Parameter	Condition	V_{CC} V	Typical	Unit
				25°C	
BW	Maximum On-Channel –3dB Bandwidth or Minimum Frequency Response	$V_{IN} = 0$ dBm V_{IN} centered between V_{CC} and GND (Figure 4)	3.0	11.5	MHz
V_{ONL}	Maximum Feedthrough On Loss	$V_{IN} = 0$ dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 4)	3.0	–0.05	dB
V_{ISO}	Off-Channel Isolation	f = 100 kHz; $V_{IS} = 1$ V RMS; $C_L = 5$ nF V_{IN} centered between V_{CC} and GND (Figure 4)	3.0	–65	dB
Q	Charge Injection Select Input to Common I/O	$V_{IN} = V_{CC}$ to GND, $R_{IS} = 0 \Omega$, $C_L = 1$ nF $Q = C_L - \Delta V_{OUT}$ (Figure 5)	3.0 5.0	15 20	pC
THD	Total Harmonic Distortion THD + Noise	$F_{IS} = 20$ Hz to 20 kHz, $R_L = R_{gen} = 600 \Omega$, $C_L = 50$ pF $V_{IS} = 1$ V RMS	3.0	0.14	%
VCT	Channel-to-Channel Crosstalk	f = 100 kHz; $V_{IS} = 1$ V RMS, $C_L = 5$ pF, $R_L = 50 \Omega$ V_{IN} centered between V_{CC} and GND (Figure 4)	3.0	–81	dB

5. Off-Channel Isolation = $20\log_{10}(V_{com}/V_{no})$, V_{com} = output, V_{no} = input to off switch.

6. –40°C specifications are guaranteed by design.

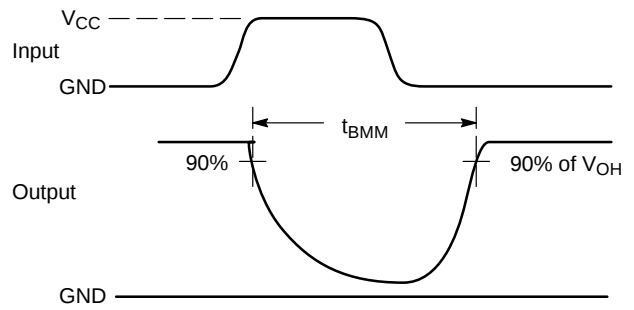
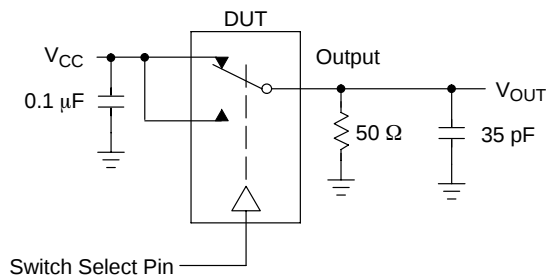


Figure 1. t_{BMM} (Time Break-Before-Make)

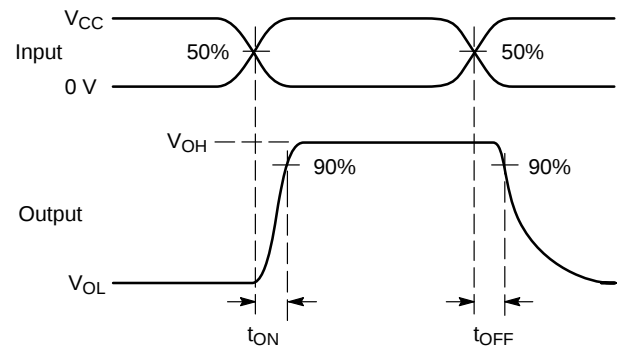
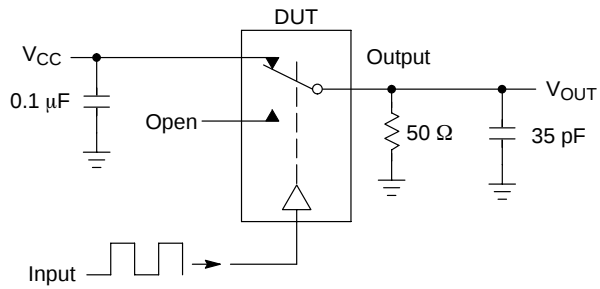


Figure 2. t_{ON}/t_{OFF}

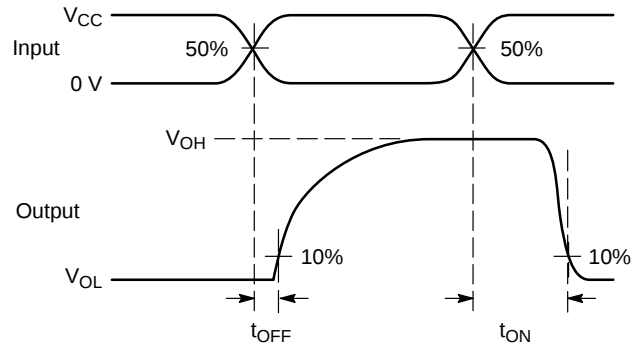
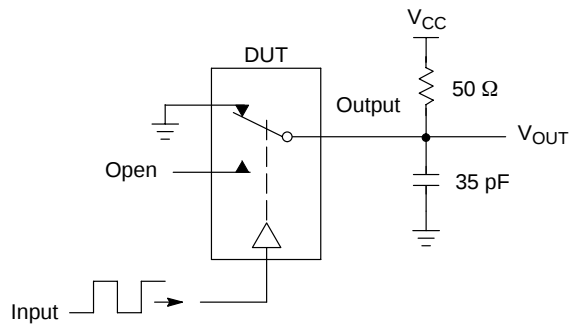
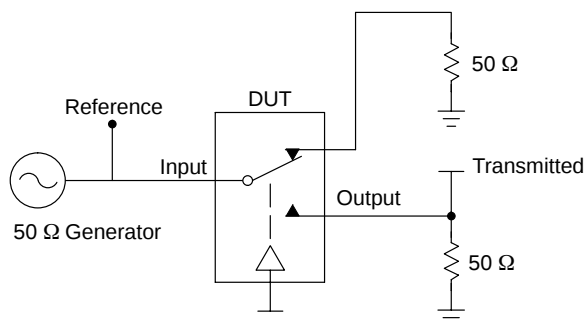


Figure 3. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 4. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

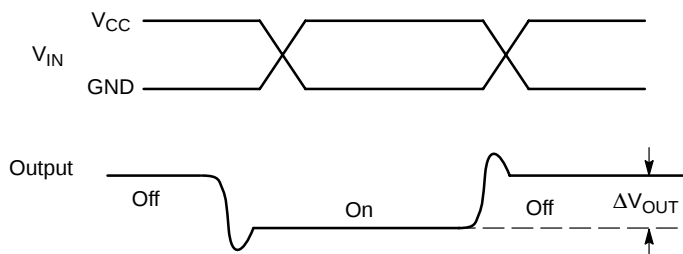
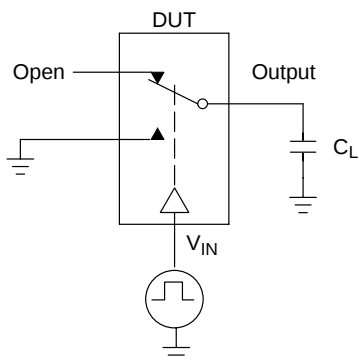


Figure 5. Charge Injection: (Q)

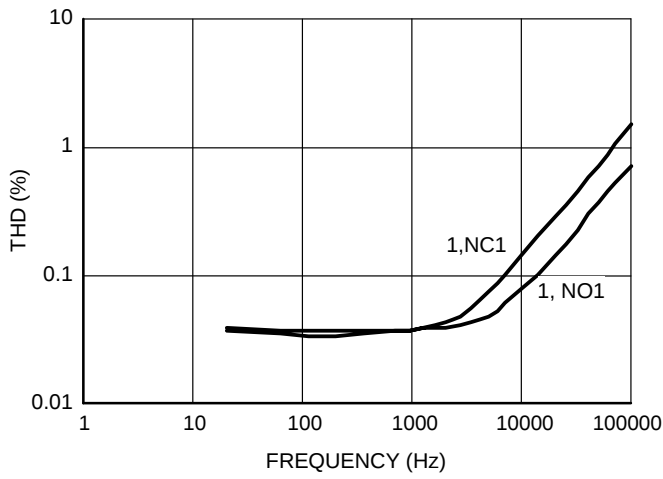


Figure 6. Total Harmonic Distortion Plus Noise versus Frequency

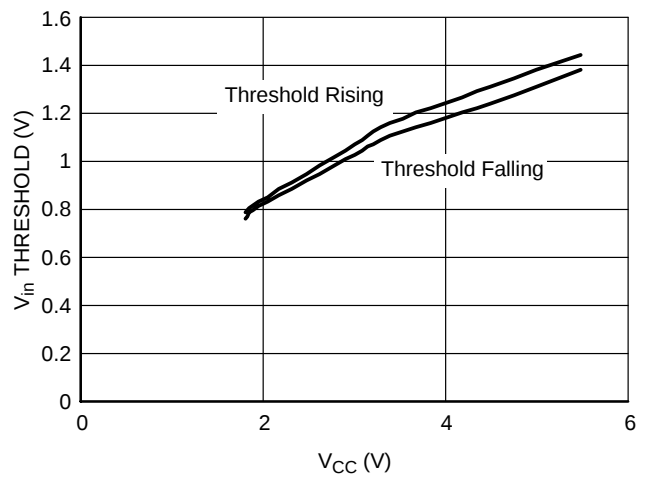


Figure 7. Voltage in Threshold on Logic Pins

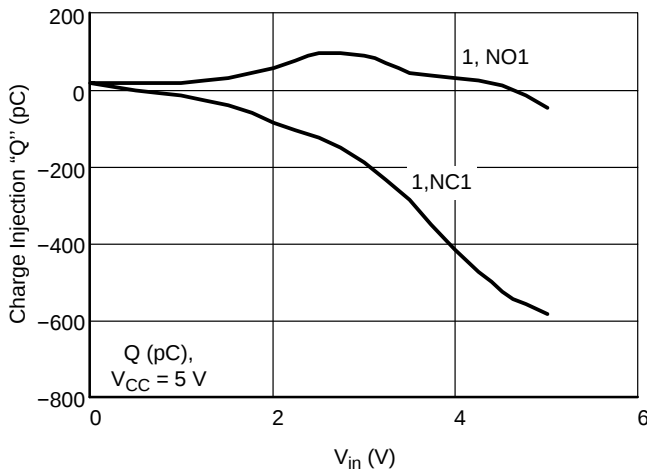


Figure 8. Charge Injection versus V_{is}

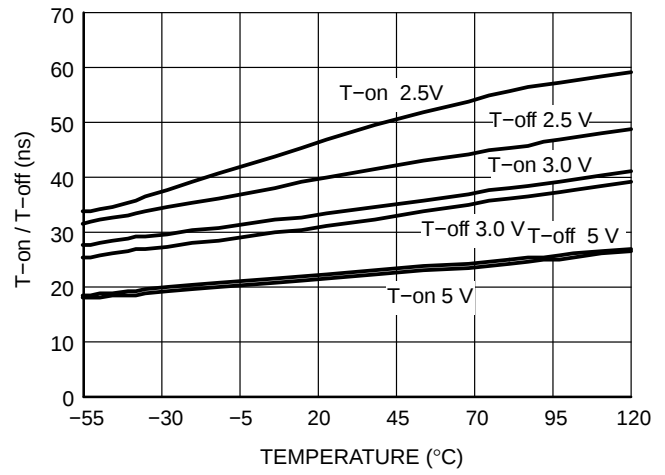


Figure 9. T-on/T-off Time versus Temperature

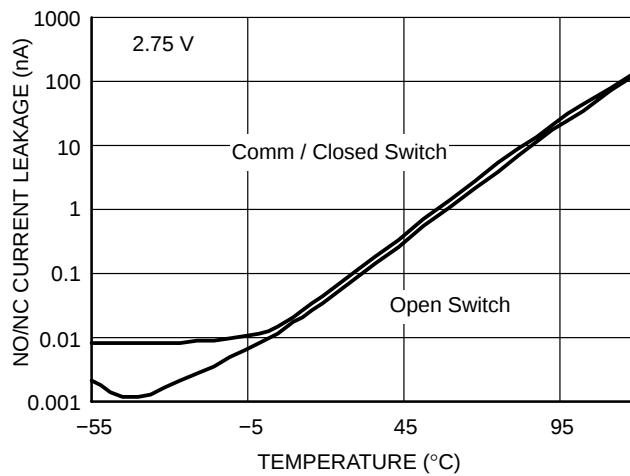


Figure 10. NO/NC Current Leakage Off and On, $V_{CC} = 5 V$

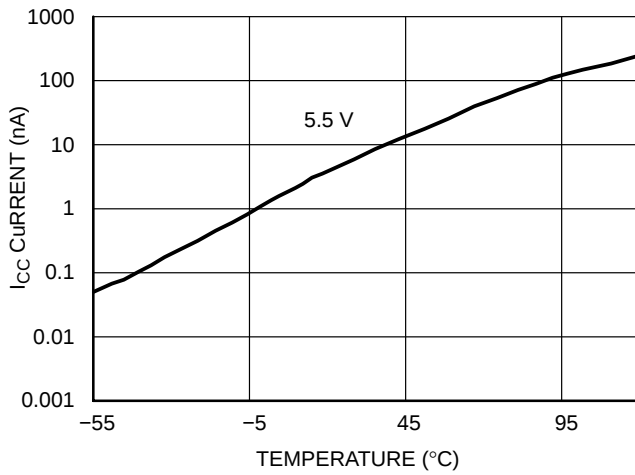


Figure 11. I_{CC} Current Leakage versus Temperature $V_{CC} = 5.5\text{ V}$

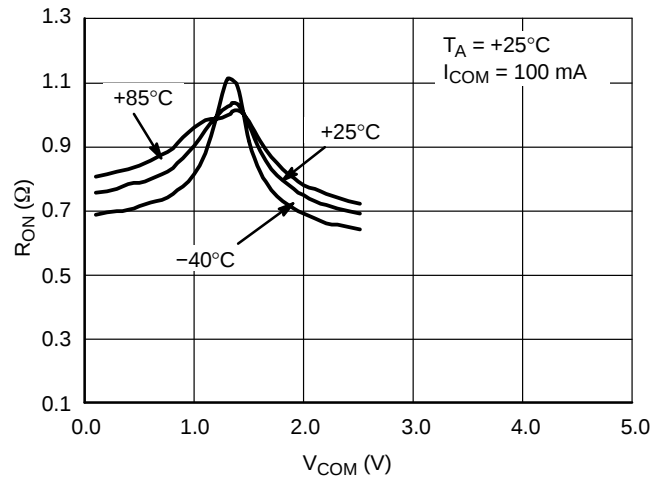


Figure 12. NC/NO On-Resistance versus COM Voltage

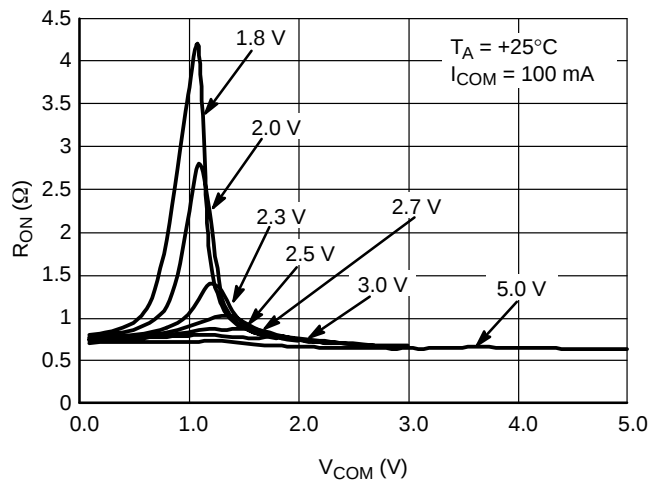


Figure 13. NC/NO On-Resistance versus COM Voltage

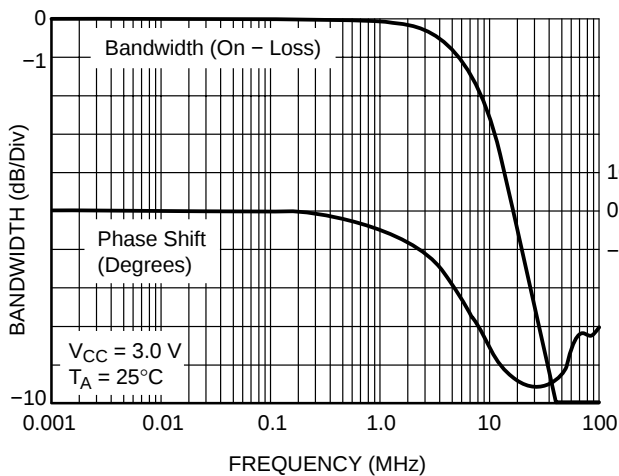


Figure 14. NC/NO Bandwidth and Phase Shift versus Frequency

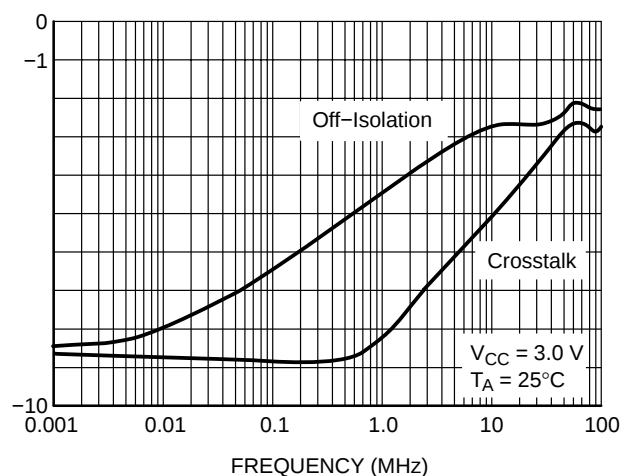


Figure 15. NC/NO Off Isolation and Crosstalk

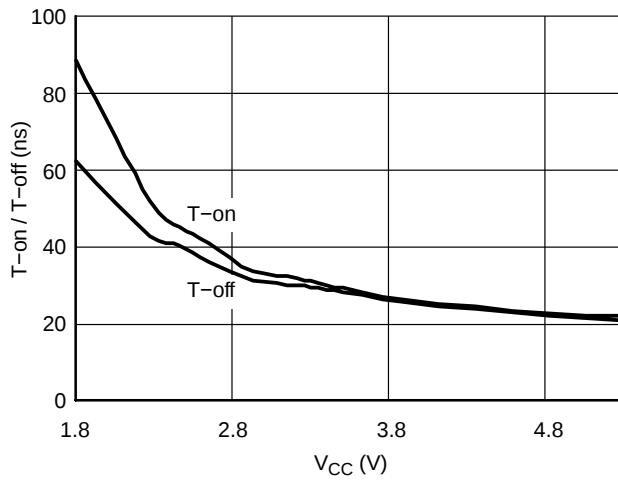


Figure 16. T-on/T-off versus V_{CC}

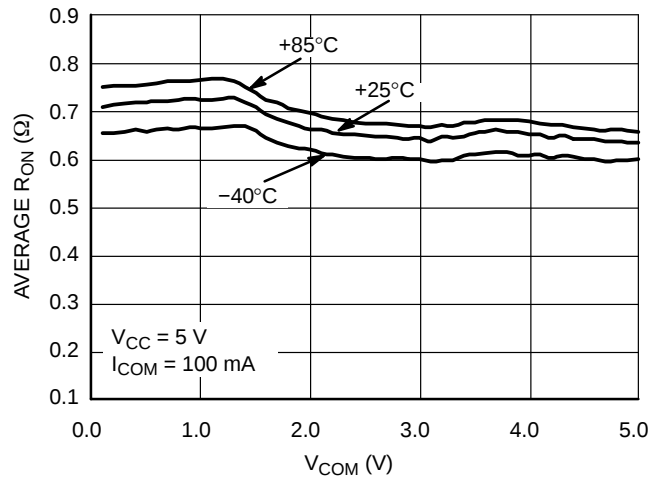


Figure 17. NC/NO On-Resistance versus COM Voltage

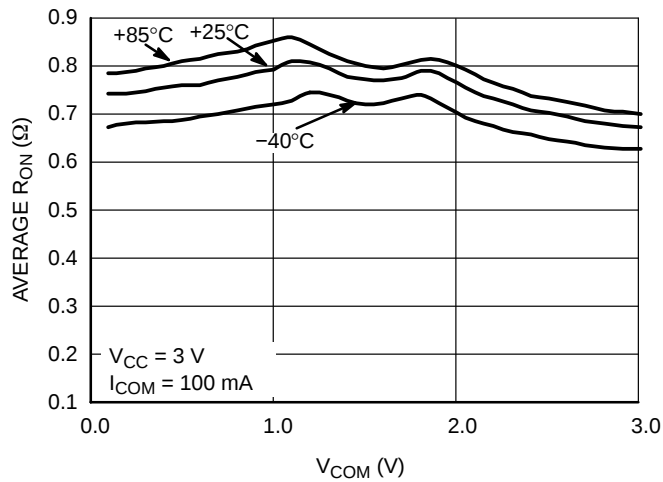
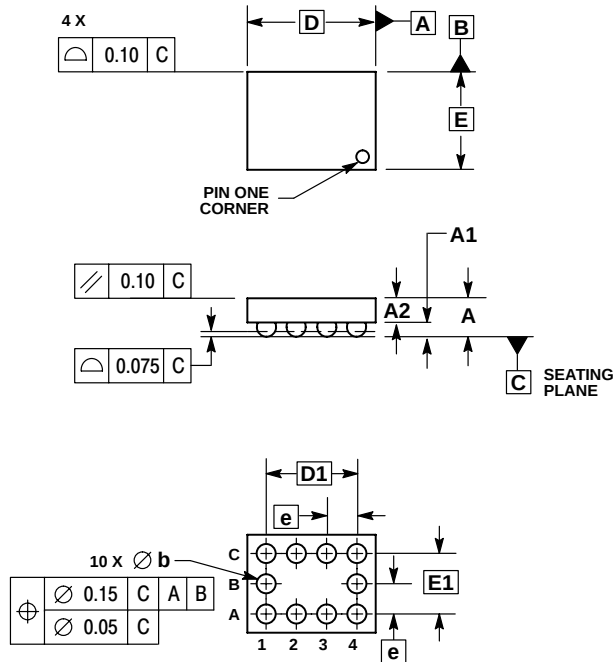


Figure 18. NC/NO On-Resistance versus COM Voltage

PACKAGE DIMENSIONS

Microbump-10 CASE 489AA-01 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.650
A1	0.210	0.270
A2	0.280	0.380
D	1.965 BSC	
E	1.465 BSC	
b	0.250	0.350
e	0.500 BSC	
D1	1.500 BSC	
E1	1.000 BSC	

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