

NLAST4599

Low Voltage Single Supply SPDT Analog Switch

The NLAST4599 is an advanced high speed CMOS single pole – double throw analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining low power dissipation. This switch controls analog and digital voltages that may vary across the full power-supply range (from V_{CC} to GND).

The device has been designed so the ON resistance (R_{ON}) is much lower and more linear over input voltage than R_{ON} of typical CMOS analog switches.

The channel select input structure provides protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. This input structure helps prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- Select Pin Compatible with TTL Levels
- Channel Select Input Over-Voltage Tolerant to 5.5 V
- Fast Switching and Propagation Speeds
- Break-Before-Make Circuitry
- Low Power Dissipation: $I_{CC} = 2 \mu A$ (Max) at $T_A = 25^\circ C$
- Diode Protection Provided on Channel Select Input
- Improved Linearity and Lower ON Resistance over Input Voltage
- Latch-up Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; MM > 200 V
- Chip Complexity: 38 FETs

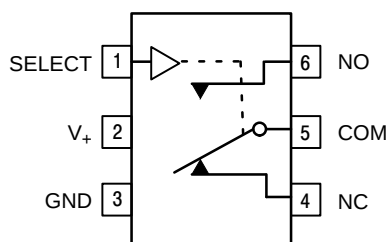


Figure 1. Pin Assignment

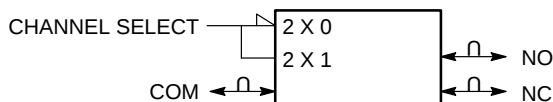


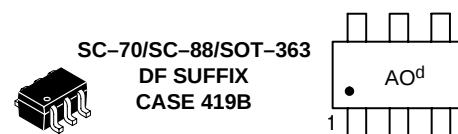
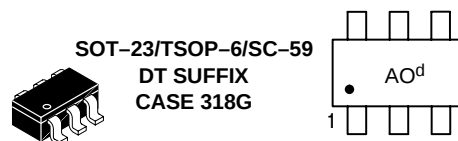
Figure 2. Logic Symbol



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAMS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section of this data sheet.

FUNCTION TABLE

Select	ON Channel
L	NC
H	NO

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage	-0.5 to +7.0	V
V_{IS}	Analog Input Voltage (V_{NO} or V_{COM})	$-0.5 \leq V_{IS} \leq V_{CC} + 0.5$	V
V_{IN}	Digital Select Input Voltage	$-0.5 \leq V_I \leq +7.0$	V
I_{IK}	DC Current, Into or Out of Any Pin	± 50	mA
P_D	Power Dissipation in Still Air	SC-88 TSOP6 200 200	mW
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1mm from Case for 10 seconds	260	°C
T_J	Junction Temperature Under Bias	150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) 2000 200 N/A	V
$I_{LATCH-UP}$	Latch-Up Performance	Above V_{CC} and Below GND at 125°C (Note 5) ± 300	mA
θ_{JA}	Thermal Resistance	SC-88 TSOP6 333 333	°C/W

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22-A114-A
3. Tested to EIA/JESD22-A115-A
4. Tested to JESD22-C101-A
5. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{IN}	Digital Select Input Voltage	GND	5.5	V
V_{IS}	Analog Input Voltage (NC, NO, COM)	GND	V_{CC}	V
T_A	Operating Temperature Range	-55	+125	°C
t_r, t_f	Input Rise or Fall Time, SELECT	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ 0 0	100 20	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

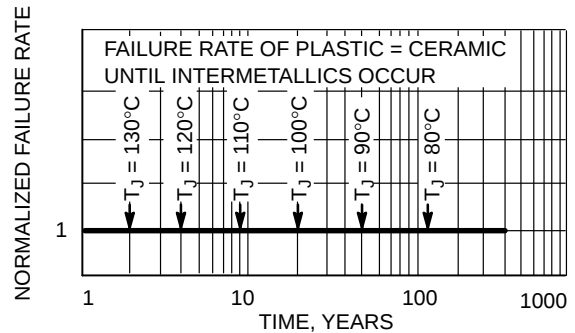


Figure 3. Failure Rate vs. Time Junction Temperature

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC}	Guaranteed Limit			Unit
				-55 to 25°C	<85°C	<125°C	
V _{IH}	Minimum High-Level Input Voltage, Select Input		3.0	2.0	2.0	2.0	V
			4.5	2.0	2.0	2.0	
			5.5	2.0	2.0	2.0	
V _{IL}	Maximum Low-Level Input Voltage, Select Input		3.0	0.5	0.5	0.5	V
			4.5	0.8	0.8	0.8	
			5.5	0.8	0.8	0.8	
I _{IN}	Maximum Input Leakage Current, Select Input	V _{IN} = 5.5 V or GND	5.5	±0.1	±1.0	±1.0	µA
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V or GND	0	±10	±10	±10	µA
I _{CC}	Maximum Quiescent Supply Current	Select and V _{IS} = V _{CC} or GND	5.5	1.0	1.0	2.0	µA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Condition	V _{CC}	Guaranteed Limit			Unit
				-55 to 25°C	<85°C	<125°C	
R _{ON}	Maximum "ON" Resistance (Figures 17 – 23)	V _{IN} = V _{IL} or V _{IH} V _{IS} = GND to V _{CC} I _{IN} ≤ 10.0 mA	2.5	85	95	105	Ω
			3.0	45	50	55	
			4.5	30	35	40	
			5.5	25	30	35	
R _{FLAT} (ON)	ON Resistance Flatness (Figures 17 – 23)	V _{IN} = V _{IL} or V _{IH} I _{IN} ≤ 10.0 mA V _{IS} = 1V, 2V, 3.5V	4.5	4	4	5	Ω
ΔR _{ON} (ON)	ON Resistance Match Between Channels	V _{IN} = V _{IL} or V _{IH} I _{IN} ≤ 10.0 mA V _{NO} or V _{NC} = 3.5 V	4.5	2	2	3	Ω
I _{NC(OFF)} I _{NO(OFF)}	NO or NC Off Leakage Current (Figure 9)	V _{IN} = V _{IL} or V _{IH} V _{NO} or V _{NC} = 1.0 V _{COM} 4.5 V	5.5	1	10	100	nA
I _{COM(ON)}	COM ON Leakage Current (Figure 9)	V _{IN} = V _{IL} or V _{IH} V _{NO} 1.0 V or 4.5 V with V _{NC} floating or V _{NO} 1.0 V or 4.5 V with V _{NO} floating V _{COM} = 1.0 V or 4.5 V	5.5	1	10	100	nA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	V _{CC} (V)	V _{IS} (V)	Guaranteed Max Limit						Unit	
					−55 to 25° C			<85° C		<125° C		
					Min	Typ*	Max	Min	Max	Min		Max
t _{ON}	Turn-On Time (Figures 12 and 13)	R _L = 300 Ω, C _L = 35 pF (Figures 5 and 6)	2.5	2.0	5	23	28	5	30	5	30	ns
			3.0	2.0	5	16	21	5	25	5	25	
			4.5	3.0	2	11	16	2	20	2	20	
			5.5	3.0	2	9	14	2	20	2	20	
t _{OFF}	Turn-Off Time (Figures 12 and 13)	R _L = 300 Ω, C _L = 35 pF (Figures 5 and 6)	2.5	2.0	1	7	12	1	15	1	15	ns
			3.0	2.0	1	5	10	1	15	1	15	
			4.5	3.0	1	4	9	1	12	1	12	
			5.5	3.0	1	3	8	1	12	1	12	
t _{BBM}	Minimum Break-Before-Make Time	V _{IS} = 3.0 V (Figure 4) R _L = 300 Ω, C _L = 35 pF	2.5	2.0	1	12		1		1		ns
			3.0	2.0	1	11		1		1		
			4.5	3.0	1	6		1		1		
			5.5	3.0	1	5		1		1		

*Typical Characteristics are at 25°C.

		Typical @ 25, $V_{CC} = 5.0$ V	
C_{IN}	Maximum Input Capacitance, Select Input	8	pF
C_{NO} or C_{NC}	Analog I/O (switch off)	10	
C_{COM}	Common I/O (switch off)	10	
$C_{(ON)}$	Feedthrough (switch on)	20	

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Condition	V_{CC} V	Typical	Unit
				25°C	
BW	Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response (Figure 10)	$V_{IN} = 0$ dBm V_{IN} centered between V_{CC} and GND (Figure 7)	3.0	170	MHz
			4.5	200	
			5.5	200	
V_{ONL}	Maximum Feedthrough On Loss	$V_{IN} = 0$ dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 7)	3.0	-2	dB
			4.5	-2	
			5.5	-2	
V_{ISO}	Off-Channel Isolation (Figure 10)	$f = 100$ kHz; $V_{IS} = 1$ V RMS V_{IN} centered between V_{CC} and GND (Figure 7)	3.0	-93	dB
			4.5	-93	
			5.5	-93	
Q	Charge Injection Select Input to Common I/O (Figure 15)	$V_{IN} = V_{CC}$ to GND, $F_{IS} = 20$ kHz $t_r = t_f = 3$ ns $R_{IS} = 0 \Omega$, $C_L = 1000$ pF $Q = C_L \cdot \Delta V_{OUT}$ (Figure 8)	3.0	1.5	pC
			5.5	3.0	
THD	Total Harmonic Distortion THD + Noise (Figure 14)	$F_{IS} = 20$ Hz to 100 kHz, $R_L = R_{gen} = 600 \Omega$, $C_L = 50$ pF $V_{IS} = 5.0$ V _{PP} sine wave	5.5	0.1	%

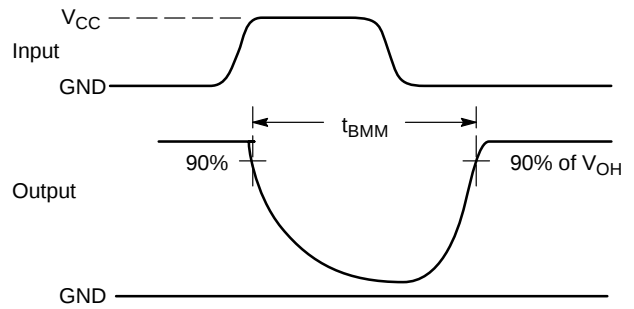
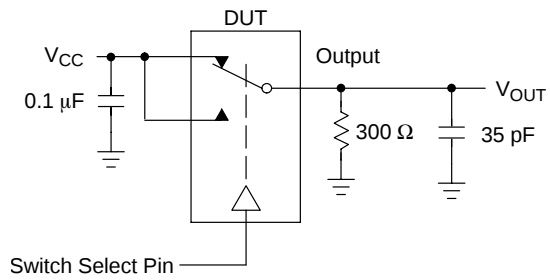


Figure 4. t_{BMM} (Time Break-Before-Make)

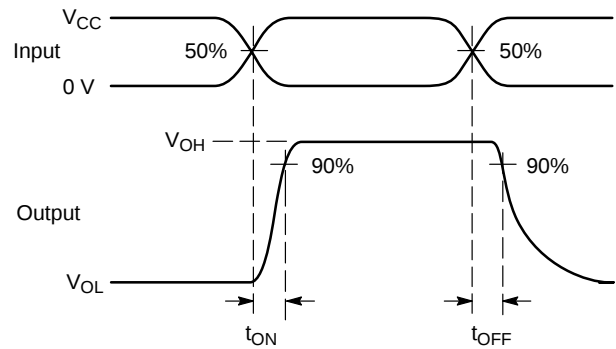
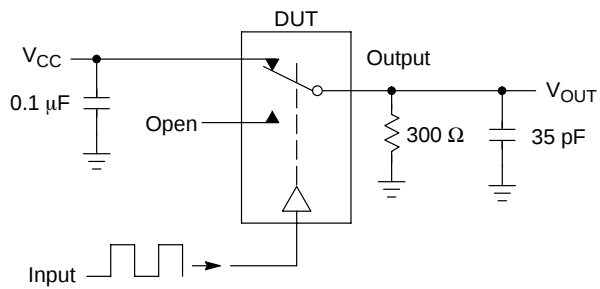


Figure 5. t_{ON}/t_{OFF}

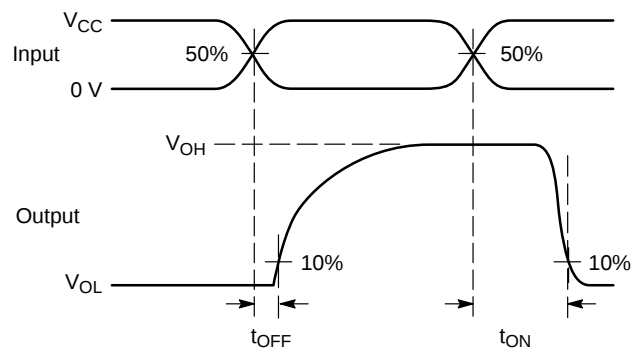
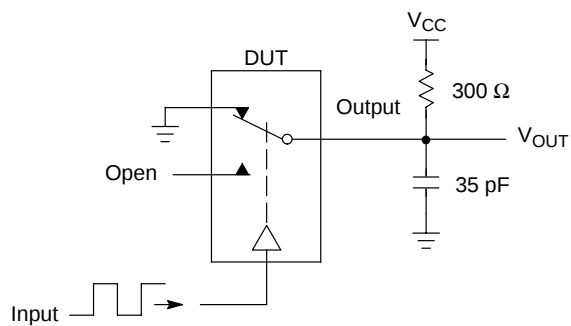
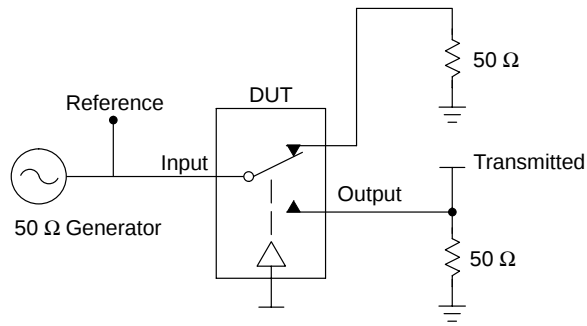


Figure 6. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

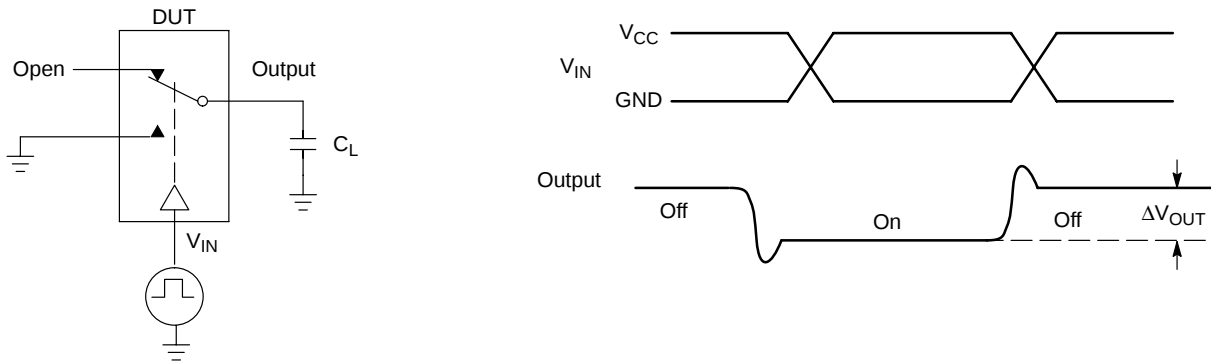


Figure 8. Charge Injection: (Q)

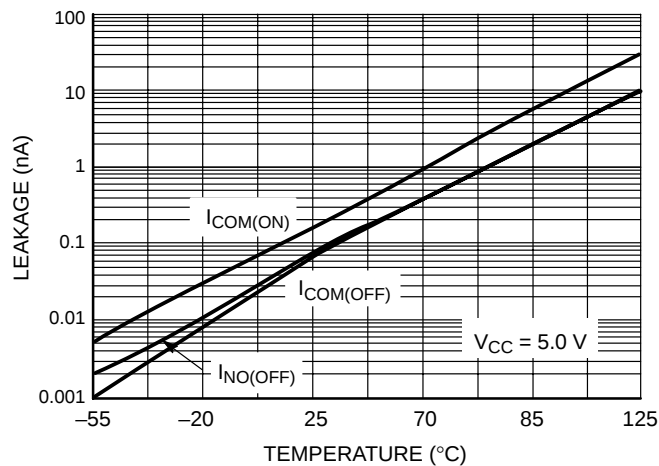


Figure 9. Switch Leakage vs. Temperature

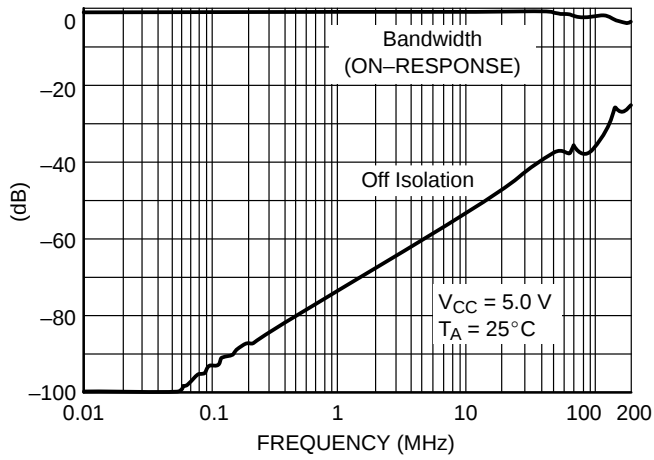


Figure 10. Bandwidth and Off-Channel Isolation

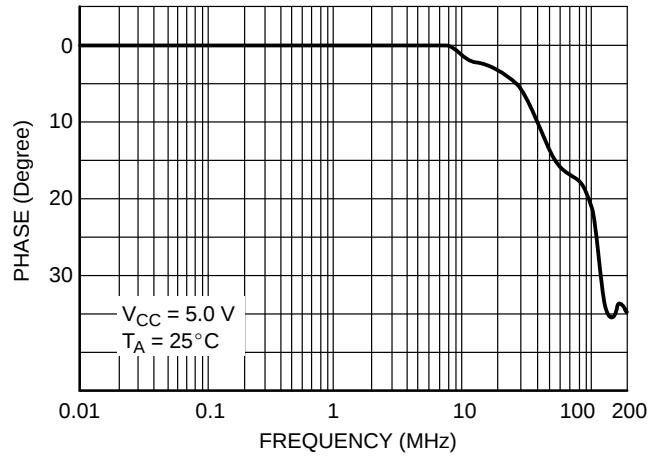


Figure 11. Phase vs. Frequency

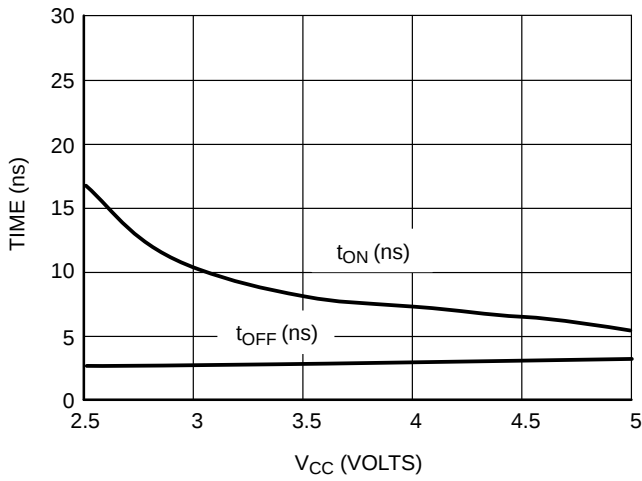


Figure 12. t_{ON} and t_{OFF} vs. V_{CC} at 25°C

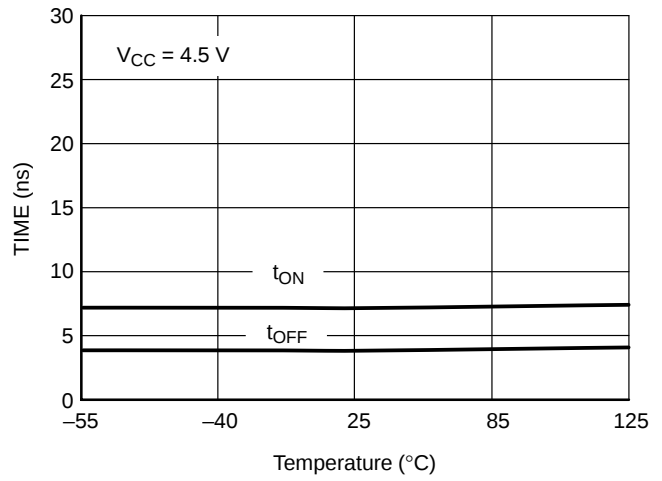


Figure 13. t_{ON} and t_{OFF} vs. Temp

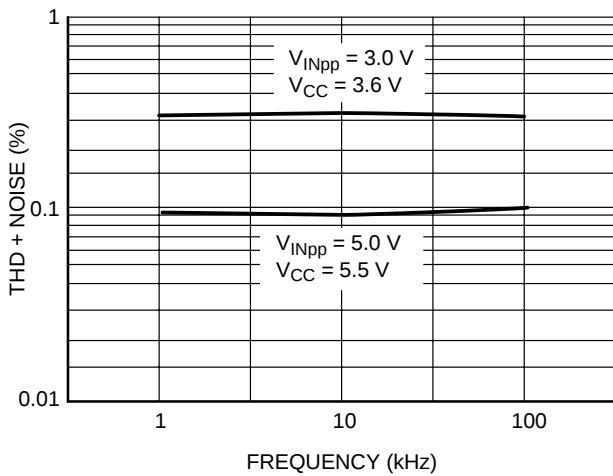


Figure 14. Total Harmonic Distortion Plus Noise vs. Frequency

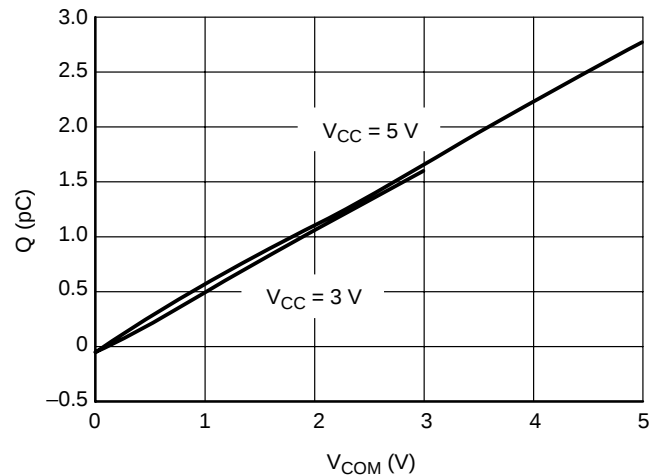


Figure 15. Charge Injection vs. COM Voltage

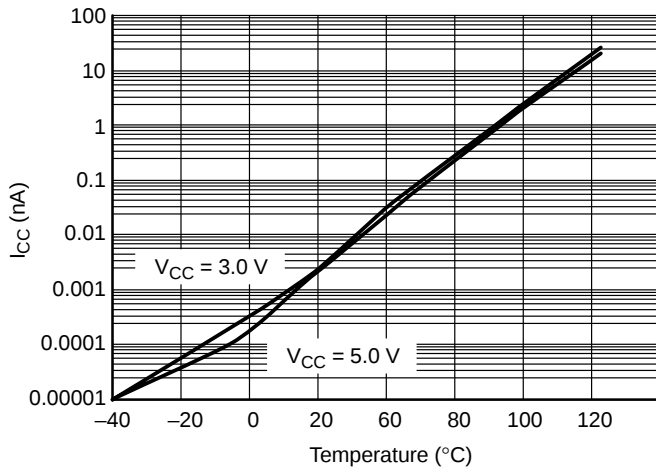


Figure 16. I_{CC} vs. Temp, $V_{CC} = 3\text{ V}$ & 5 V

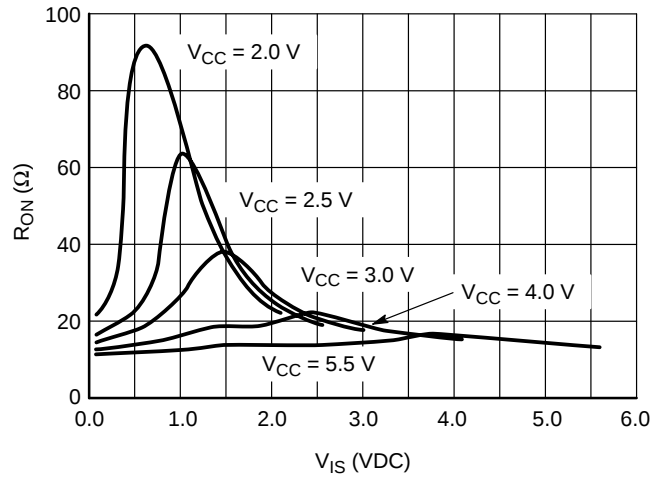


Figure 17. R_{ON} vs. V_{CC} , Temp = 25°C

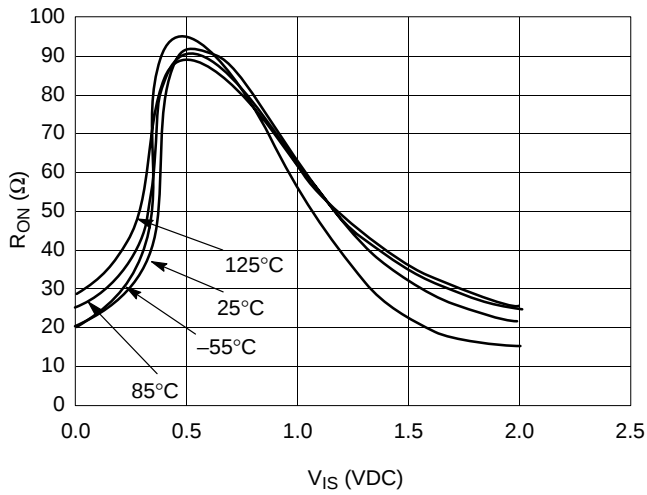


Figure 18. R_{ON} vs Temp, $V_{CC} = 2.0\text{ V}$

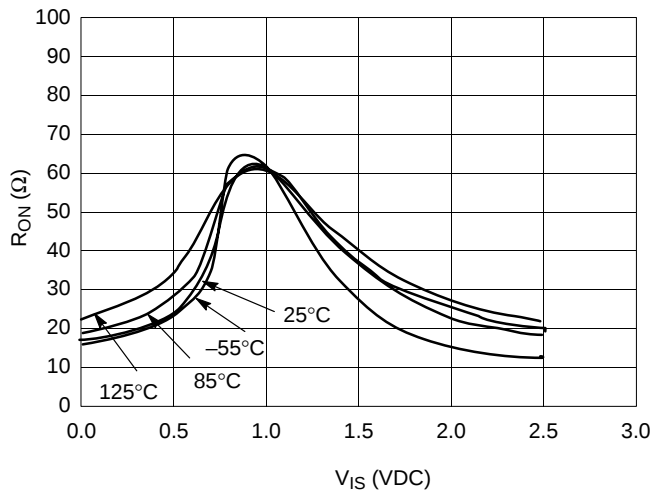


Figure 19. R_{ON} vs. Temp, $V_{CC} = 2.5\text{ V}$

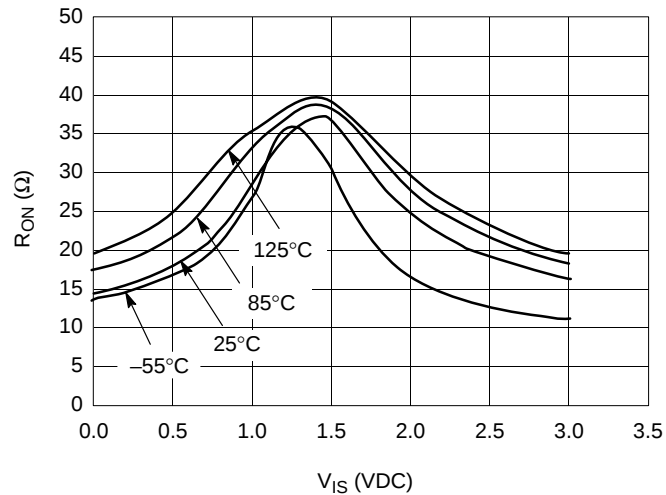


Figure 20. R_{ON} vs. Temp, $V_{CC} = 3.0\text{ V}$

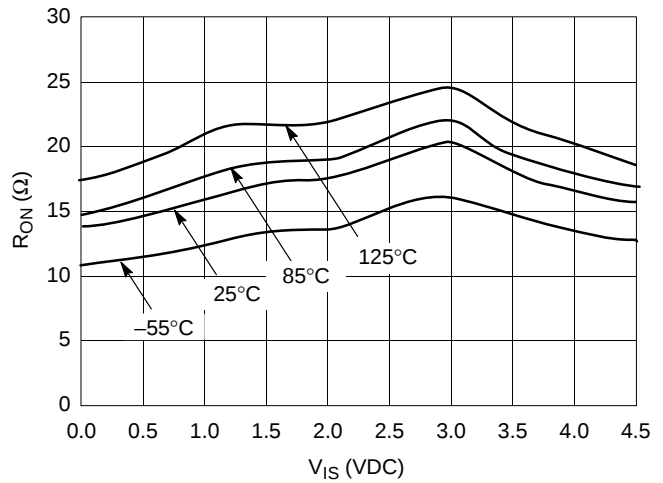


Figure 21. R_{ON} vs. Temp, $V_{CC} = 4.5\text{ V}$

NLAST4599

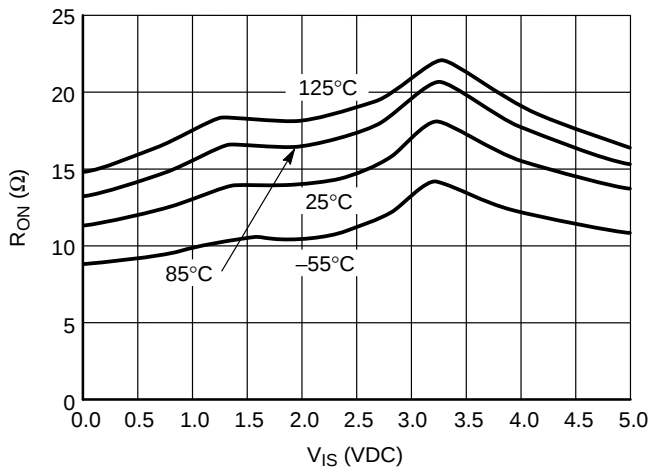


Figure 22. R_{ON} vs. Temp, $V_{CC} = 5.0$ V

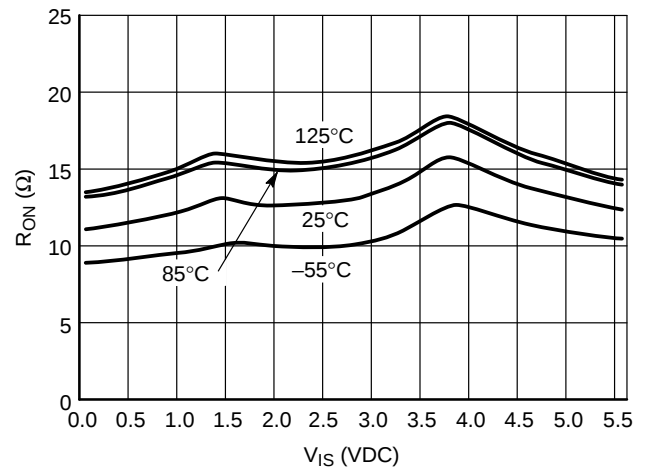


Figure 23. R_{ON} vs. Temp, $V_{CC} = 5.5$ V

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature					Package Type (Name/SOT#/ Common Name)	Tape and Reel Size
	Circuit Indicator	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NLAST4599DFT2	NL	AS	4599	DF	T2	SC-70 / SC-88 / SOT-363	178 mm (7") 3000 Unit
NLAST4599DTT1	NL	AS	4599	DT	T1	SOT-23 / TSOP-6 / SC-59	178 mm (7") 3000 Unit

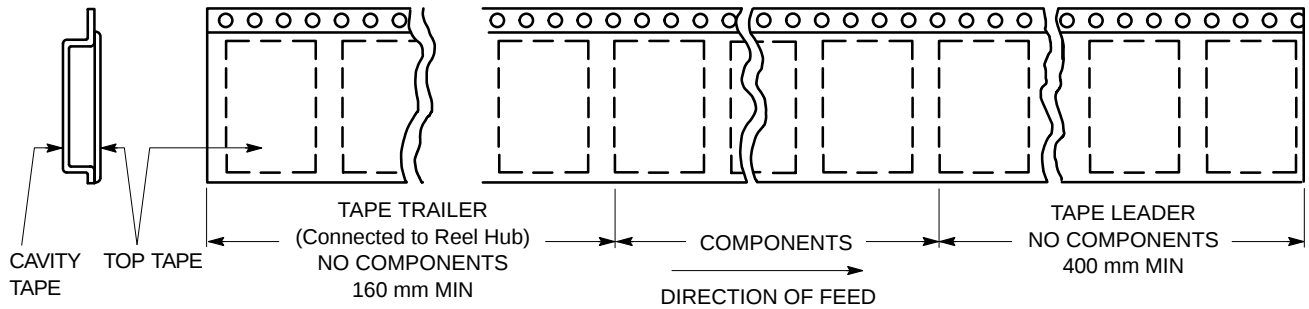


Figure 24. Tape Ends for Finished Goods

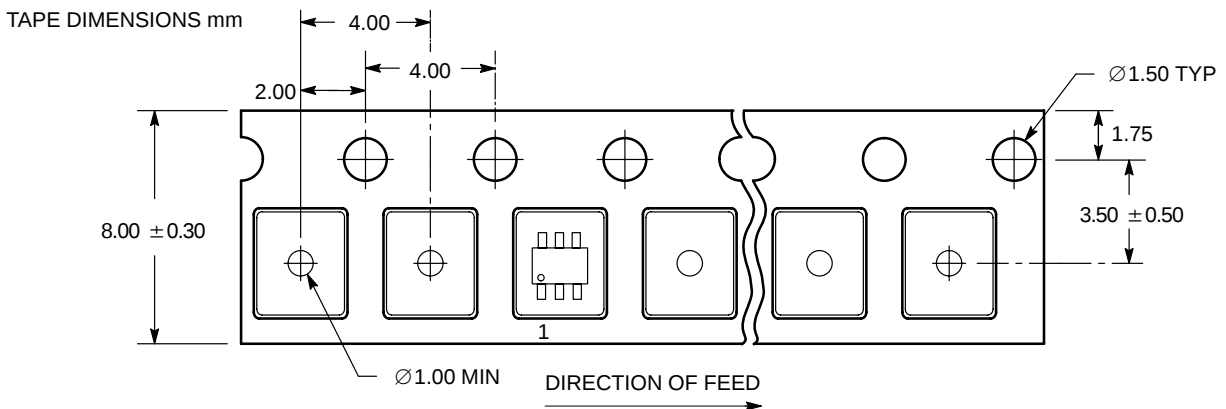


Figure 25. SC70-6/SC-88/SOT-363 DFT2 and SOT23-6/TSOP-6/SC59-6 DTT1 Reel Configuration/Orientation

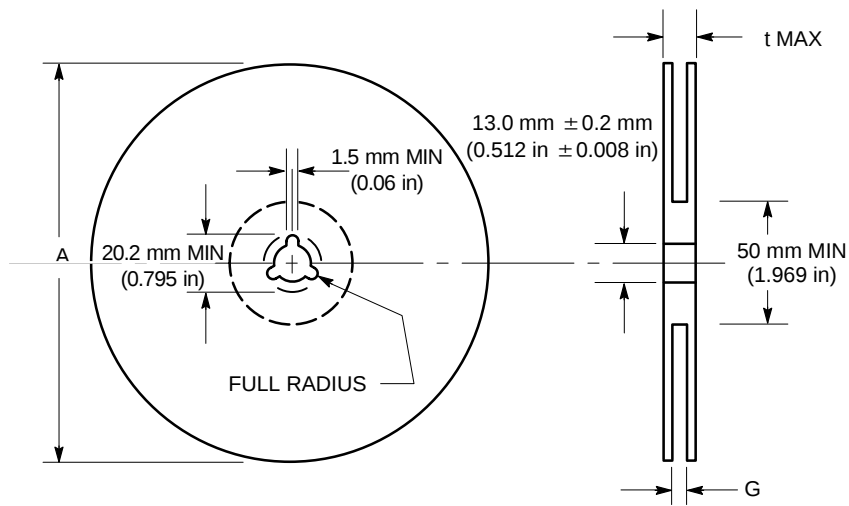


Figure 26. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

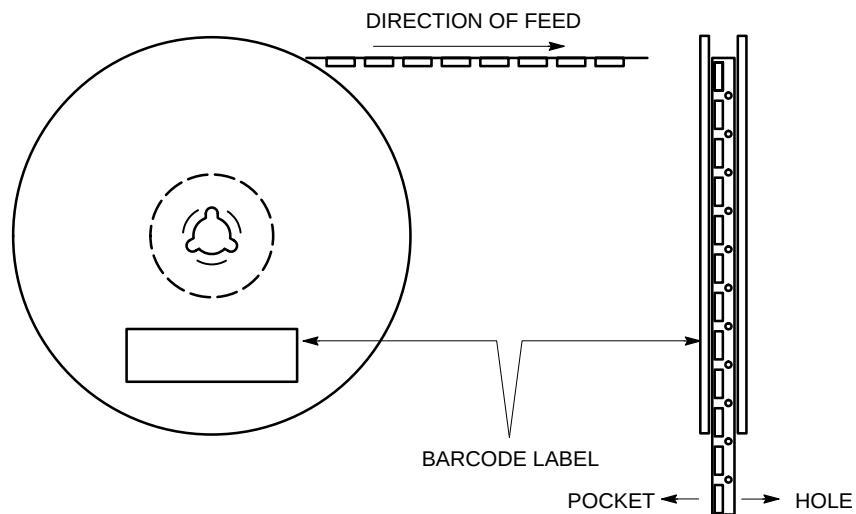


Figure 27. Reel Winding Direction

NLAST4599

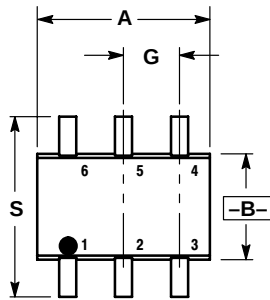
PACKAGE DIMENSIONS

SC70-6/SC-88/SOT-363

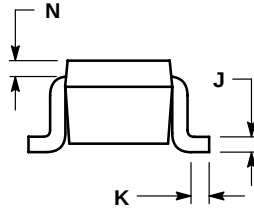
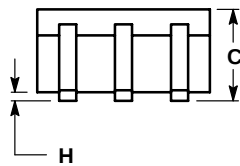
DF SUFFIX

CASE 419B-02

ISSUE J



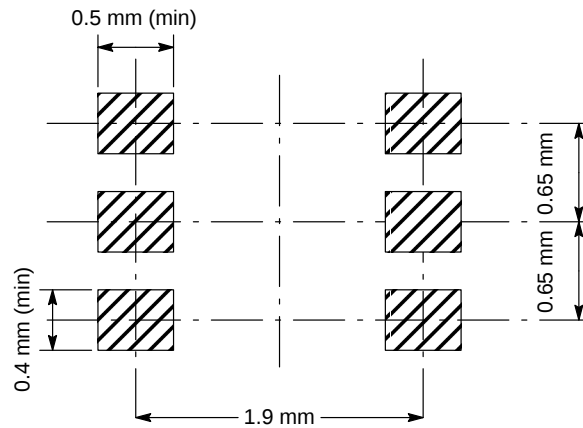
D 6 PL $\oplus$ 0.2 (0.008) M B M



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20



NLAST4599

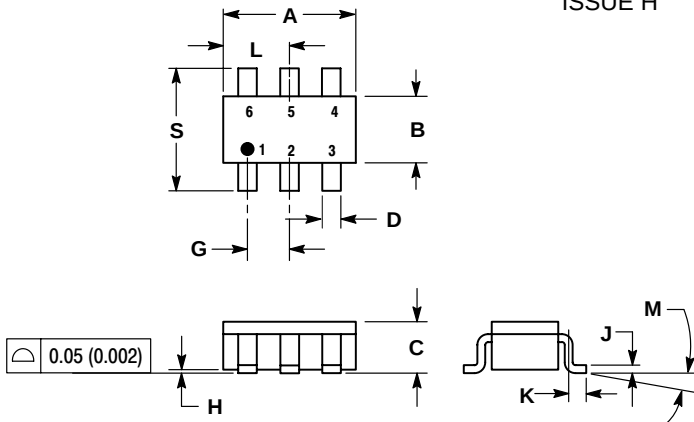
PACKAGE DIMENSIONS

SOT23-6/TSOP-6/SC59-6

DT SUFFIX

CASE 318G-02

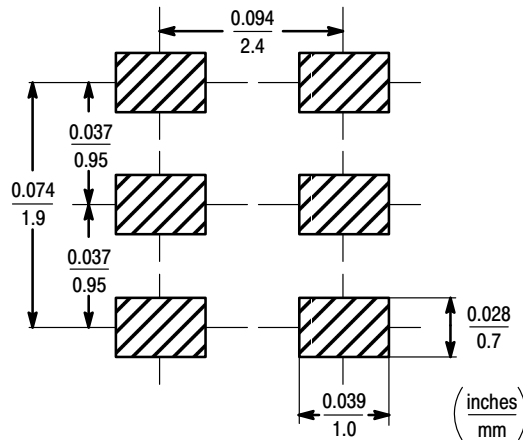
ISSUE H



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
E	0.85	1.05	0.0335	0.0413
F	0.013	0.100	0.0005	0.0040
G	0.10	0.26	0.0040	0.0102
H	0.20	0.60	0.0079	0.0236
I	1.25	1.55	0.0493	0.0610
J	0°	10°	0°	10°
K	2.50	3.00	0.0985	0.1181



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