

NTD80N02

Power MOSFET

24 V, 80 A, N-Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Pb-Free Packages are Available

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	24	Vdc
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	Vdc
Drain Current – Continuous @ $T_C = 25^\circ\text{C}$ – Single Pulse ($t_p = 10 \mu\text{s}$)	I_D I_{DM}	80* 200	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	75	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 24 \text{ Vdc}$, $V_{GS} = 10 \text{ Vdc}$, $I_L = 17 \text{ Apk}$, $L = 5.0 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	733	mJ
Thermal Resistance – Junction-to-Case – Junction-to-Ambient (Note 1) – Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.65 67 120	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in²).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in²).

*Chip current capability limited by package.

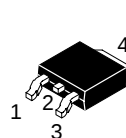
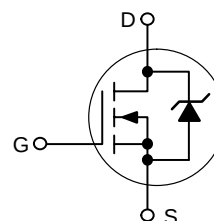


ON Semiconductor®

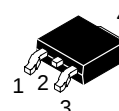
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
24 V	5.0 m Ω	80 A

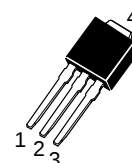
N-Channel



CASE 369AA
DPAK
(Surface Mount)
STYLE 2

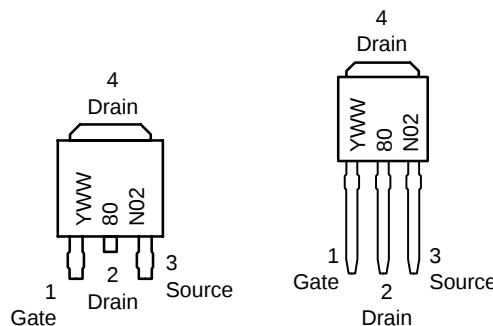


CASE 369C
DPAK
(Surface Mount)
STYLE 2



CASE 369D
DPAK
(Straight Lead)
STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENTS



Y = Year
WW = Work Week
80N02 = Device Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD80N02

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μ Adc) Positive Temperature Coefficient	V _{(BR)DSS}	24 –	27 25	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{GS} = 0 Vdc, V _{DS} = 24 Vdc) (V _{GS} = 0 Vdc, V _{DS} = 24 Vdc, T _J = 125°C)	I _{DSS}	– –	– –	1.0 10	μ Adc
Gate-Body Leakage Current (V _{GS} = $\pm$ 20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	$\pm$ 100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μ Adc) Negative Threshold Temperature Coefficient	V _{GS(th)}	1.0 –	1.9 –3.8	3.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 10 Vdc, I _D = 80 Adc) (V _{GS} = 4.5 Vdc, I _D = 40 Adc) (V _{GS} = 10 Vdc, I _D = 20 Adc) (V _{GS} = 4.5 Vdc, I _D = 20 Adc)	R _{DS(on)}	– – – –	5.0 7.5 5.0 7.5	5.8 9.0 5.8 9.0	m Ω
Forward Transconductance (V _{DS} = 15 Vdc, I _D = 10 Adc) (Note 3)	g _{FS}	–	20	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 20 Vdc, V _{GS} = 0 V, f = 1.0 MHz)	C _{iss}	–	2250	2600	pF
Output Capacitance		C _{oss}	–	900	1100	
Transfer Capacitance		C _{rss}	–	400	525	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{GS} = 4.5 Vdc, V _{DD} = 20 Vdc, I _D = 20 Adc, R _G = 2.5 Ω)	t _{d(on)}	–	17	30	ns
Rise Time		t _r	–	67	125	
Turn-Off Delay Time		t _{d(off)}	–	28	45	
Fall Time		t _f	–	40	75	
Gate Charge	(V _{GS} = 4.5 Vdc, I _D = 20 Adc, V _{DS} = 20 Vdc) (Note 3)	Q _T	–	30	42	nC
		Q ₁	–	7.0	12	
		Q ₂	–	18	28	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage (I _S = 20 Adc, V _{GS} = 0 Vdc) (Note 3) (I _S = 40 Adc, V _{GS} = 0 Vdc) (I _S = 20 Adc, V _{GS} = 0 Vdc, T _J = 150°C)	V _{SD}	– – –	0.92 1.05 0.70	1.2 – –	Vdc
Reverse Recovery Time (I _S = 20 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/ μ s) (Note 3)	t _{rr}	–	38	52	ns
	t _a	–	20	–	
	t _b	–	18	–	
Reverse Recovery Stored Charge	Q _{rr}	–	0.038	–	μ C

3. Pulse Test: Pulse Width $\leq$ 300 μ s, Duty Cycle $\leq$ 2%.

4. Switching characteristics are independent of operating junction temperatures.

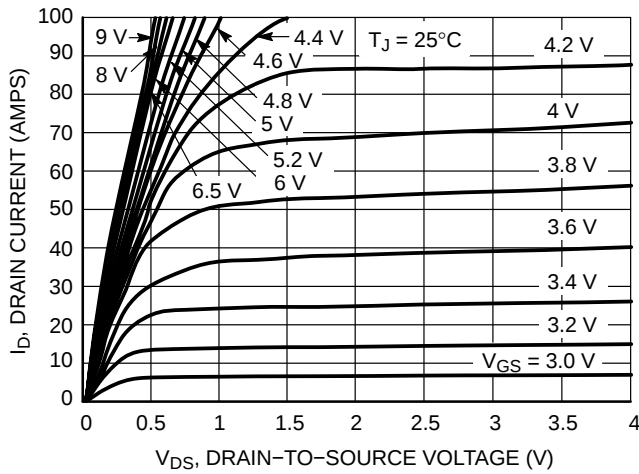


Figure 1. On-Region Characteristics

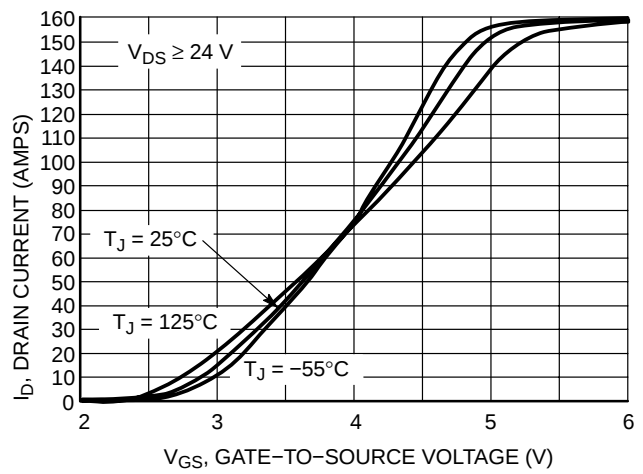


Figure 2. Transfer Characteristics

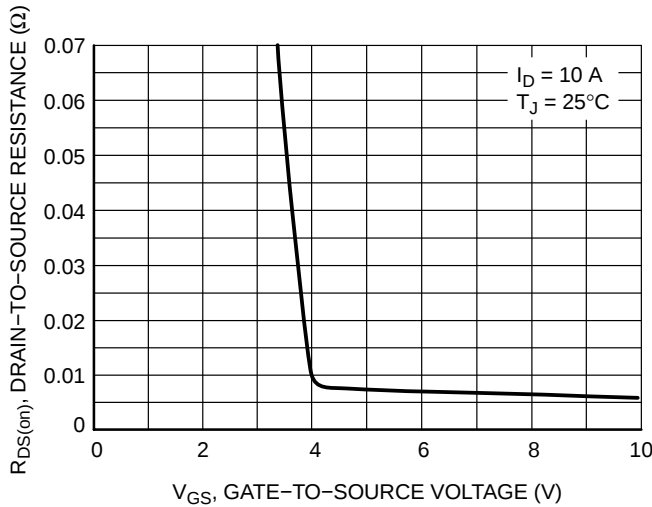


Figure 3. On-Resistance versus Gate-to-Source Voltage

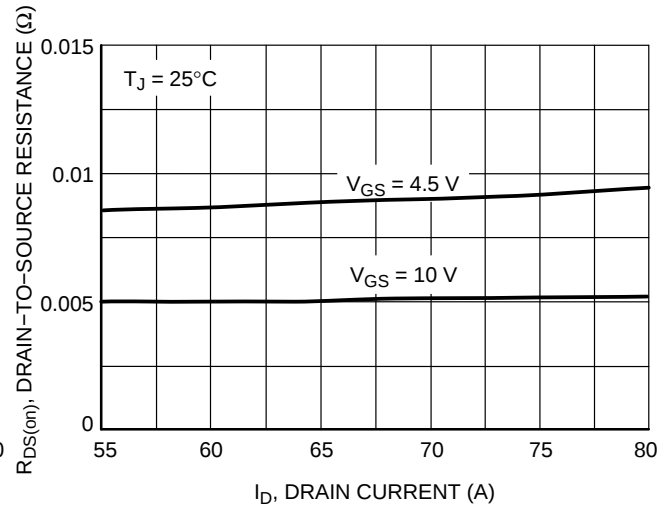


Figure 4. On-Resistance versus Drain Current and Gate Voltage

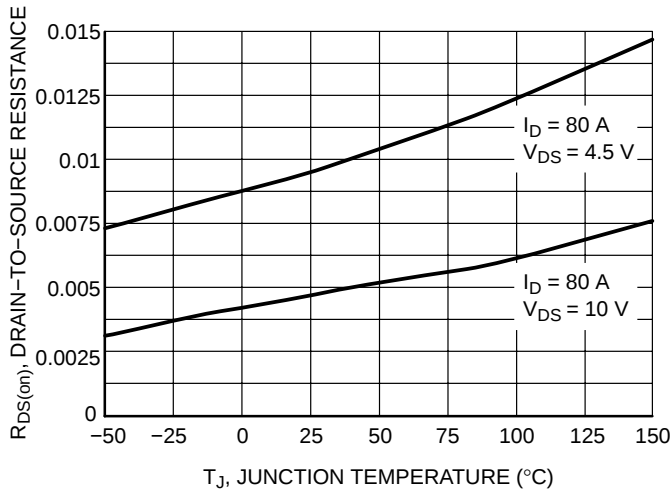


Figure 5. On-Resistance Variation with Temperature

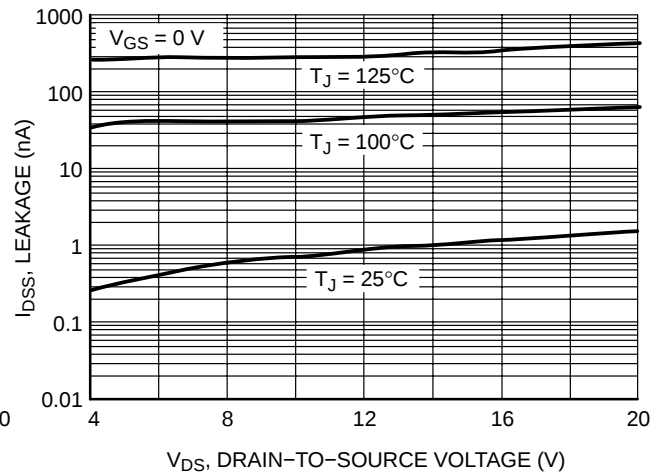


Figure 6. Drain-to-Source Leakage Current versus Voltage

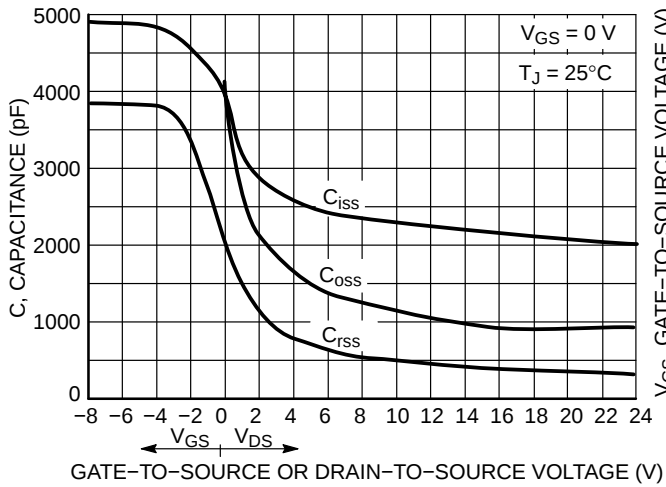


Figure 7. Capacitance Variation

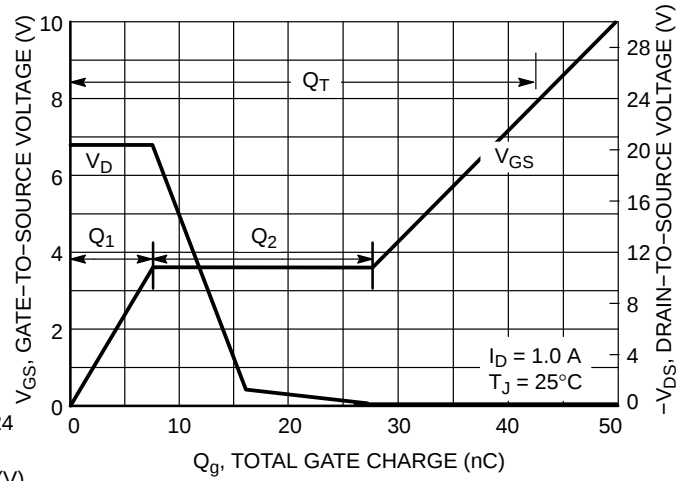


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

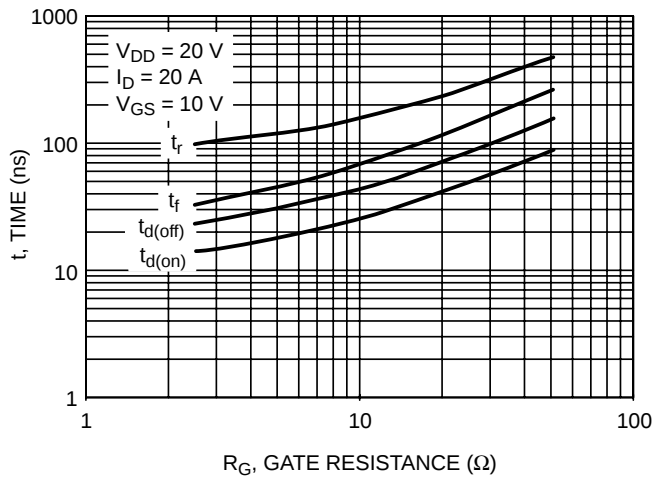


Figure 9. Resistive Switching Time Variation versus Gate Resistance

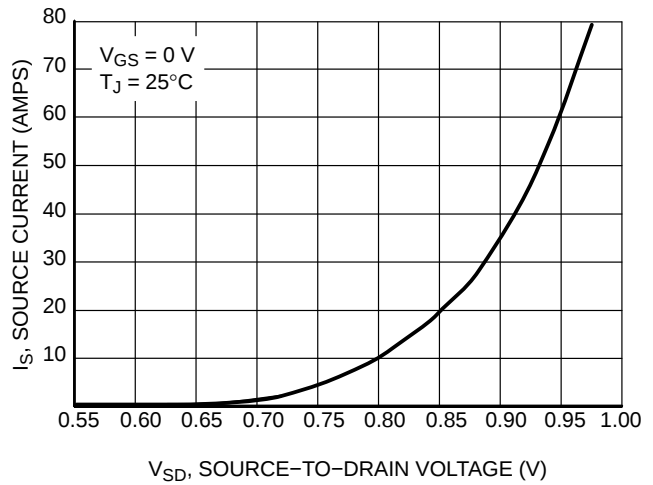


Figure 10. Diode Forward Voltage versus Current

NTD80N02

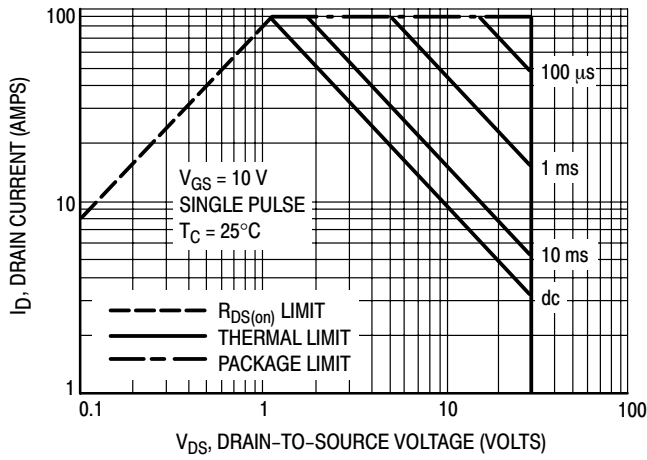


Figure 11. Maximum Rated Forward Biased Safe Operating Area

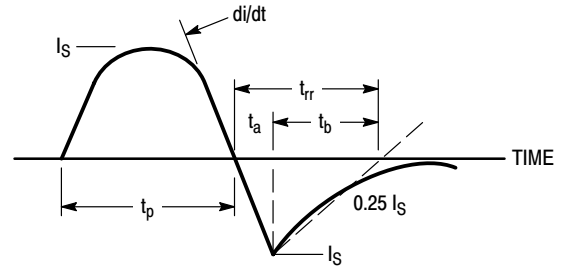


Figure 12. Diode Reverse Recovery Waveform

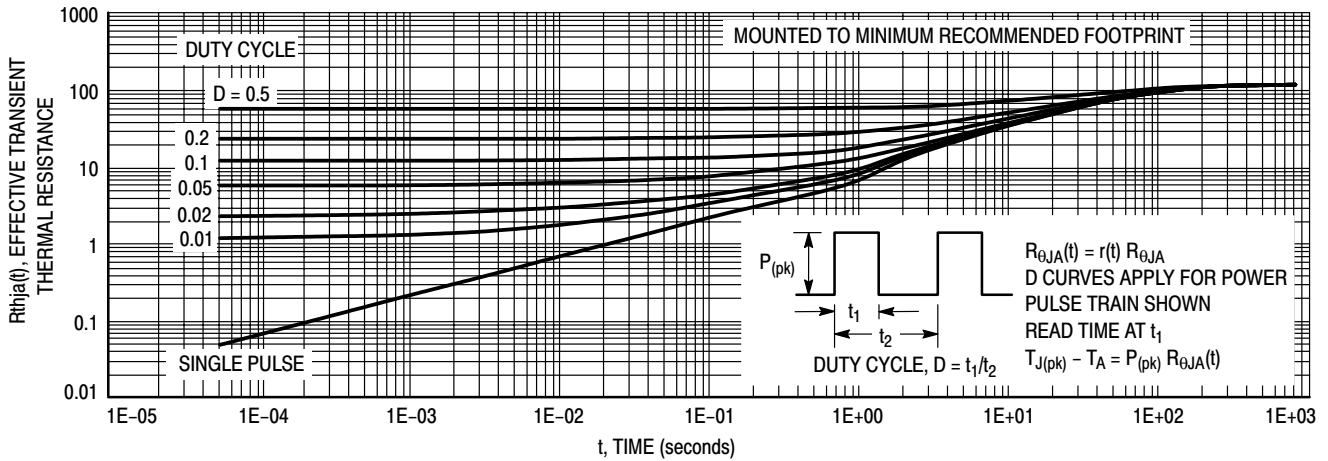


Figure 13. Thermal Response – Various Duty Cycles

ORDERING INFORMATION

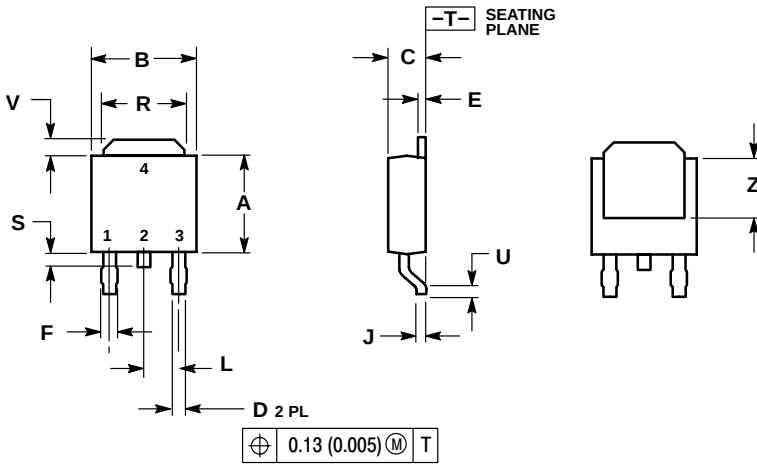
Order Number	Package	Shipping [†]
NTD80N02	DPAK-3	75 Units / Rail
NTD80N02G	DPAK-3 (Pb-Free)	75 Units / Rail
NTD80N02T4	DPAK-3	2500 / Tape & Reel
NTD80N02T4G	DPAK-3 (Pb-Free)	2500 / Tape & Reel
NTD80N02-001	DPAK-3 Straight Lead	75 Units / Rail
NTD80N02-1G	DPAK-3 Straight Lead (Pb-Free)	75 Units / Rail
NTD80N02-032	DPAK-3 Straight Lead (3.2 ± 0.5 mm)	75 Units / Rail
NTD80N02-032G	DPAK-3 Straight Lead (3.2 ± 0.5 mm) (Pb-Free)	75 Units / Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTD80N02

PACKAGE DIMENSIONS

DPAK
CASE 369AA-01
ISSUE O

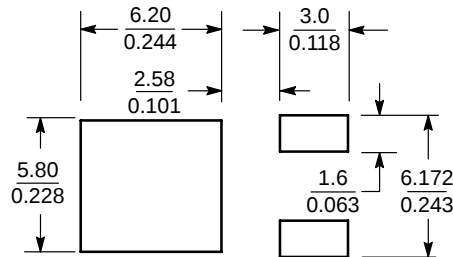


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.88
E	0.018	0.024	0.46	0.61
F	0.033	0.045	0.83	1.14
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:
- PIN 1. GATE
 - DRAIN
 - SOURCE
 - DRAIN

SOLDERING FOOTPRINT*



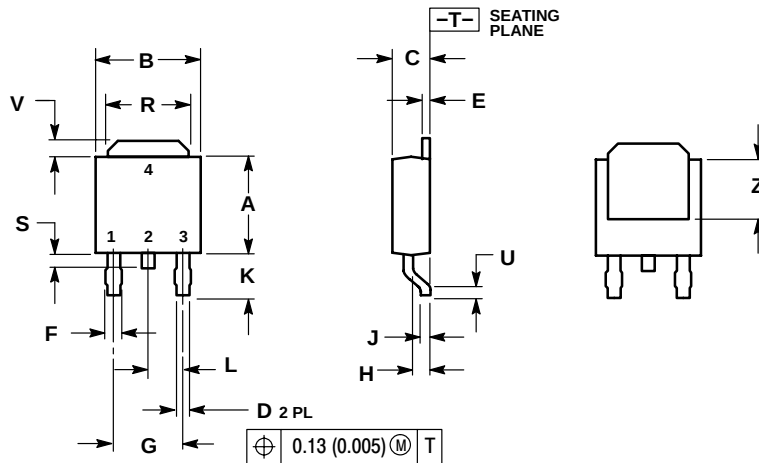
SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}} \right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD80N02

PACKAGE DIMENSIONS

DPAK
CASE 369C-01
ISSUE O

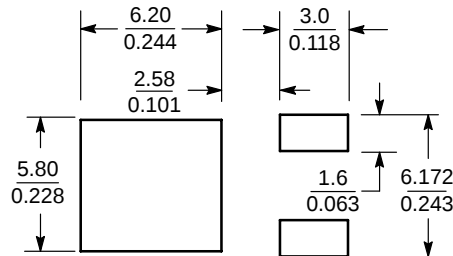


NOTES:
1. DIMENSIONING AND TOLERANCING
PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



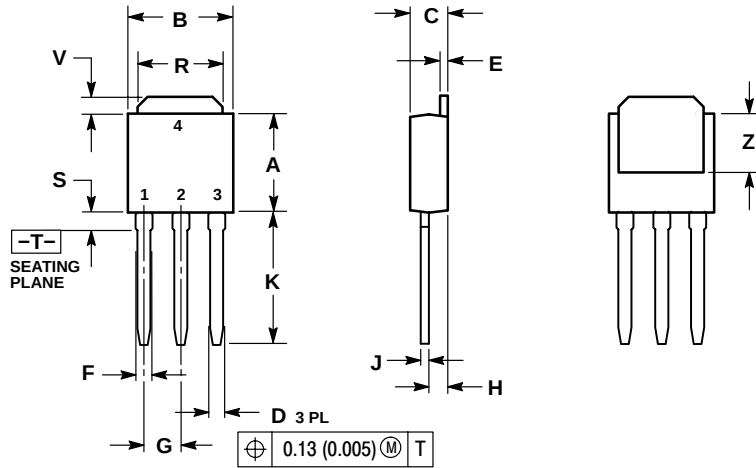
SCALE 3:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD80N02

PACKAGE DIMENSIONS

DPAK CASE 369D-01 ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.