NTP22N06L, NTB22N06L

Power MOSFET
22 Amps, 60 Volts, Logic Level
N–Channel TO–220 and D^{2}PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

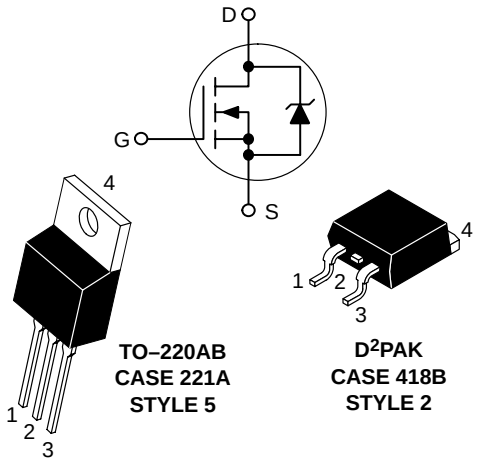
Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 10 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage – Continuous – Non–Repetitive ($t_p \le 10$ ms)	 V_{GS} V_{GS}	 ±10 ±20	Vdc
Drain Current – Continuous @ T_A = 25°C – Continuous @ T_A = 100°C – Single Pulse ($t_p \le 10$ μs)	 I_D I_D I_{DM}	 22 10 66	 Adc Apk
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	60 0.4	W W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to +175	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 5.0 Vdc, L = 1.0 mH $I_{L(pk)}$ = 12 A, V_{DS} = 60 Vdc, R_G = 25 Ω)	E_{AS}	72	mJ
Thermal Resistance – Junction–to–Case – Junction–to–Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

ON Semiconductor™

http://onsemi.com

22 AMPERES
60 VOLTS
$R_{DS(on)}$ = 65 mΩ

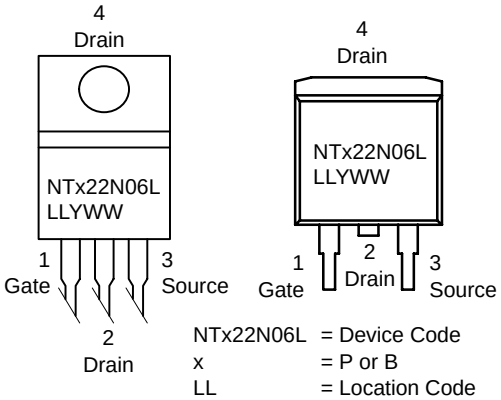
N–Channel



TO–220AB
CASE 221A
STYLE 5

D^{2}PAK
CASE 418B
STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENTS



NTx22N06L	= Device Code
x	= P or B
LL	= Location Code
Y	= Year
WW	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
NTP22N06L	TO–220AB	50 Units/Rail
NTB22N06L	D^{2}PAK	50 Units/Rail
NTB22N06LT4	D^{2}PAK	800/Tape & Reel

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Note 1.) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 60 –	 68.2 81	 – –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	 – –	 – –	 1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	±100	nAdc
ON CHARACTERISTICS (Note 1.)						
Gate Threshold Voltage (Note 1.) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 –	 1.79 5.0	 2.0 –	Vdc mV/°C
Static Drain–to–Source On–Resistance (Note 1.) (V_{GS} = 5.0 Vdc, I_D = 11 Adc)		$R_{DS(on)}$	 –	 57	 65	mΩ
Static Drain–to–Source On–Voltage (Note 1.) (V_{GS} = 5.0 Vdc, I_D = 22 Adc) (V_{GS} = 5.0 Vdc, I_D = 11 Adc, T_J = 150°C)		$V_{DS(on)}$	 – –	 1.4 1.17	 1.7 –	Vdc
Forward Transconductance (Note 1.) (V_{DS} = 7.0 Vdc, I_D = 11 Adc)		g_{FS}	–	14.6	–	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	490	690	pF
Output Capacitance		C_{oss}	–	167	230	
Transfer Capacitance		C_{rss}	–	56	80	
SWITCHING CHARACTERISTICS (Note 2.)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 22 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω) (Note 1.)	$t_{d(on)}$	–	10	20	ns
Rise Time		t_r	–	115	230	
Turn–Off Delay Time		$t_{d(off)}$	–	21	40	
Fall Time		t_f	–	56	120	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 22 Adc, V_{GS} = 5.0 Vdc) (Note 1.)	Q_T	–	10.4	20	nC
		Q_1	–	2.5	–	
		Q_2	–	7.0	–	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 22 Adc, V_{GS} = 0 Vdc) (Note 1.) (I_S = 22 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	 –	 1.03 0.98	 1.2 –	Vdc
Reverse Recovery Time	(I_S = 22 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 1.)	t_{rr}	–	42	–	ns
		t_a	–	26	–	
		t_b	–	16	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.060	–	μC

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperatures.

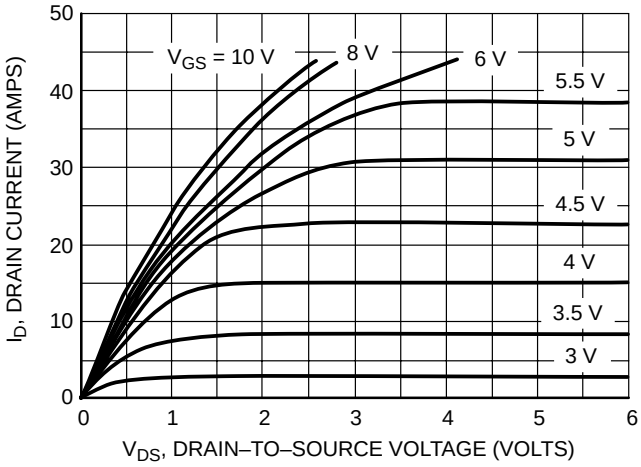


Figure 1. On–Region Characteristics

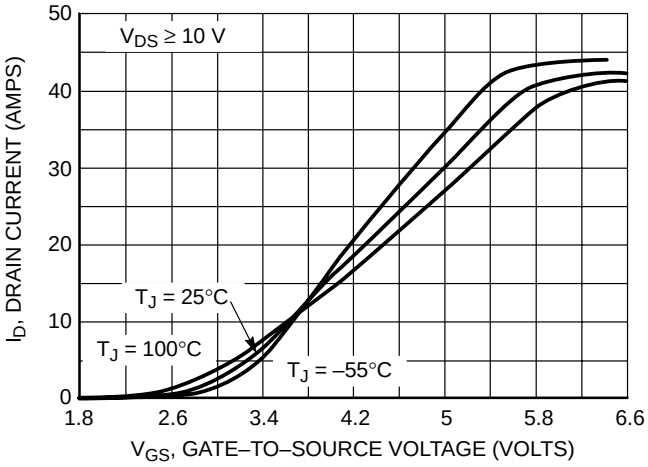


Figure 2. Transfer Characteristics

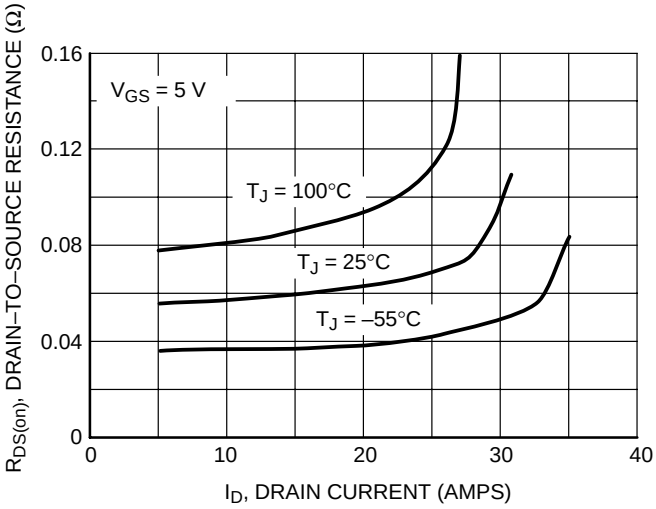


Figure 3. On–Resistance versus Gate–to–Source Voltage

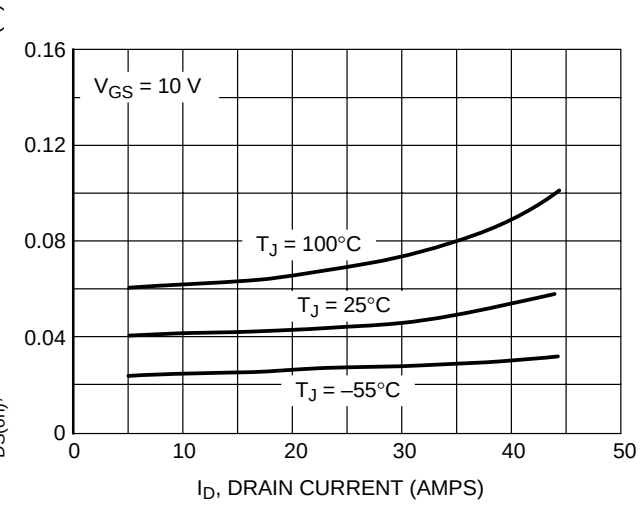


Figure 4. On–Resistance versus Drain Current and Gate Voltage

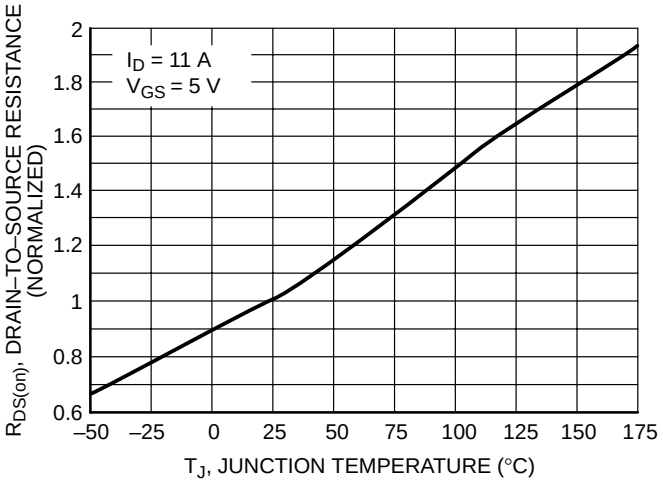


Figure 5. On–Resistance Variation with Temperature

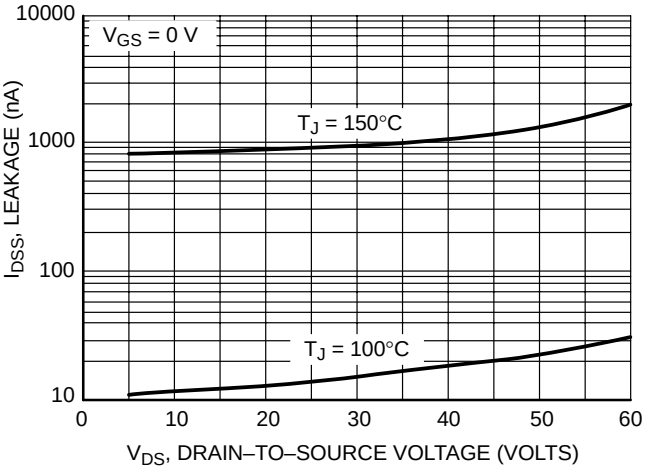


Figure 6. Drain–to–Source Leakage Current versus Voltage

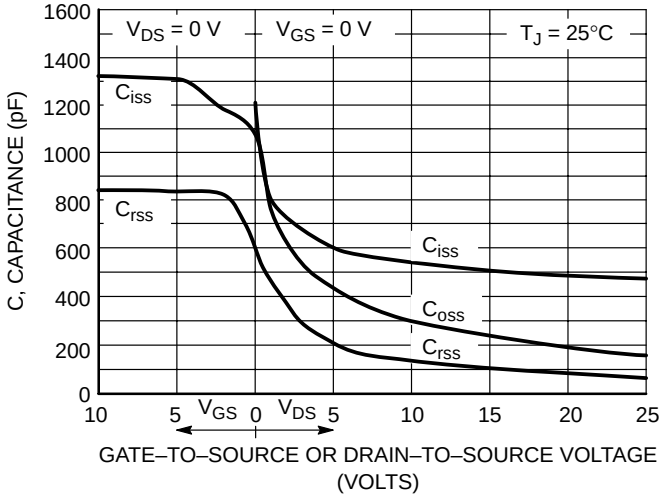


Figure 7. Capacitance Variation

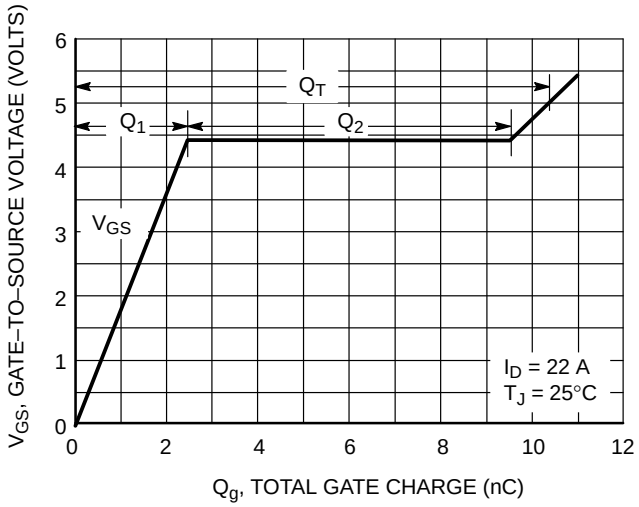


Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

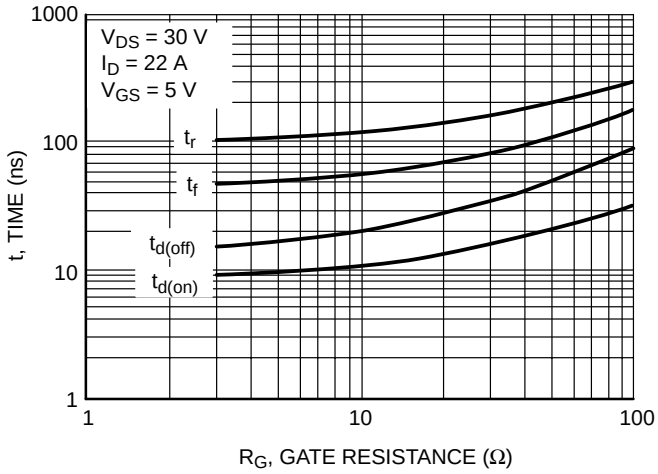


Figure 9. Resistive Switching Time Variation versus Gate Resistance

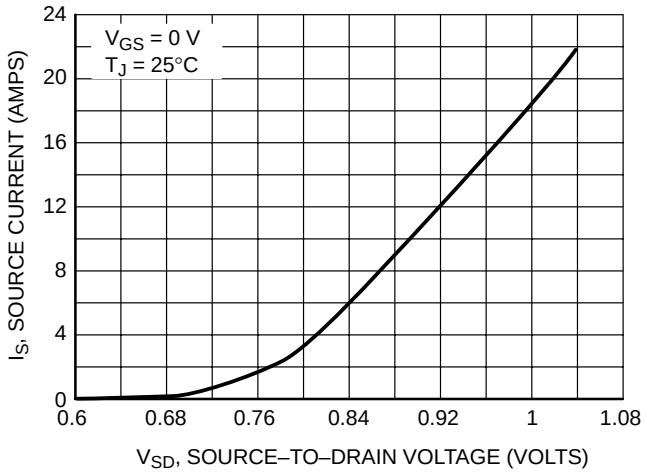


Figure 10. Diode Forward Voltage versus Current

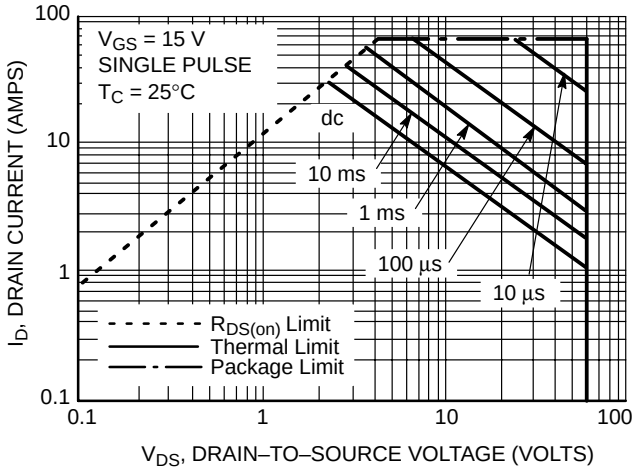


Figure 11. Maximum Rated Forward Biased Safe Operating Area

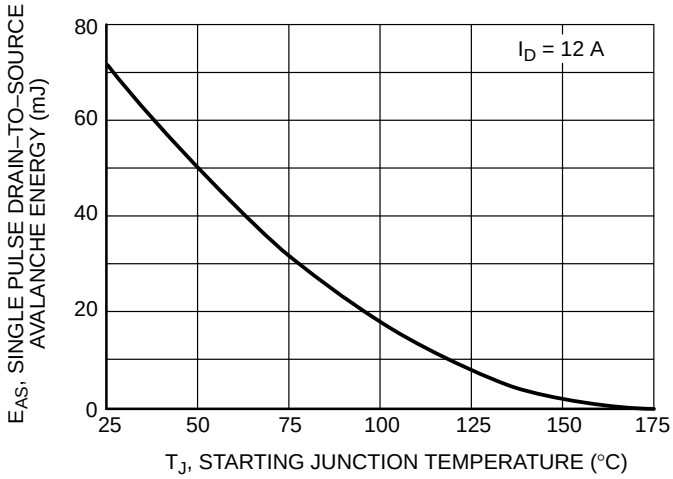


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

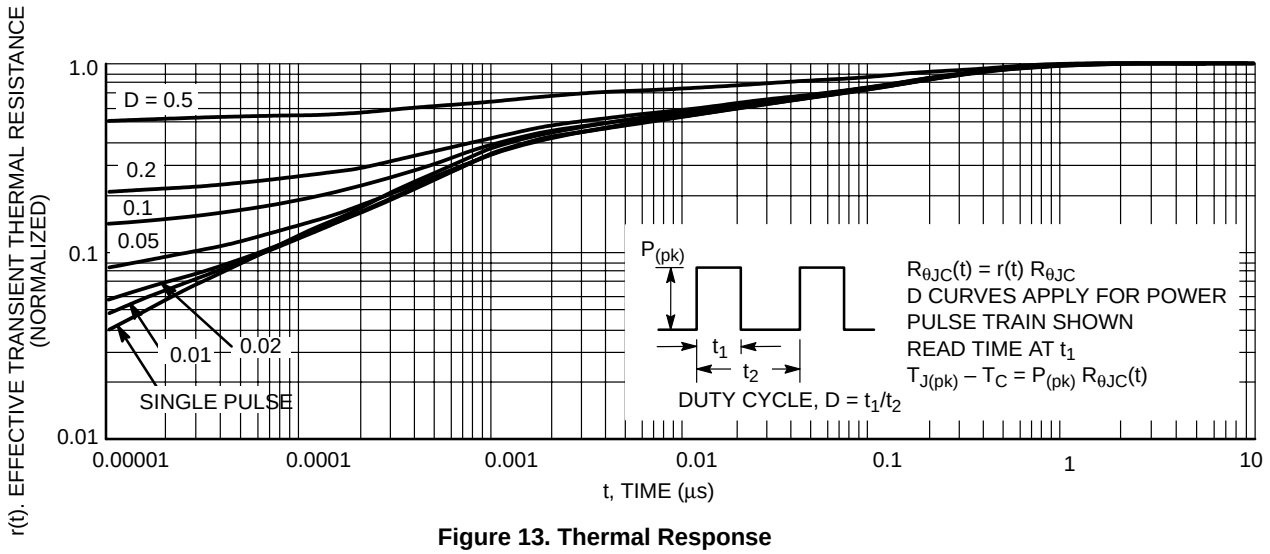


Figure 13. Thermal Response

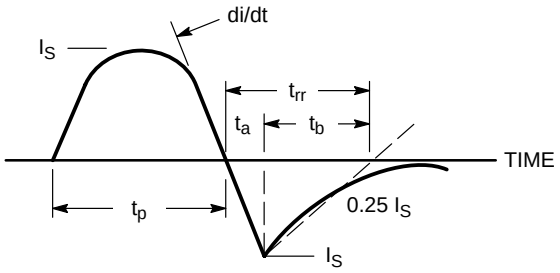
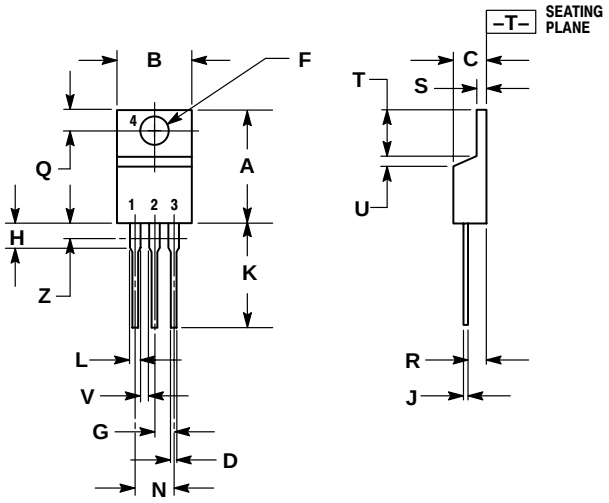


Figure 14. Diode Reverse Recovery Waveform

PACKAGE DIMENSIONS

TO–220 THREE–LEAD
TO–220AB
CASE 221A–09
ISSUE AA



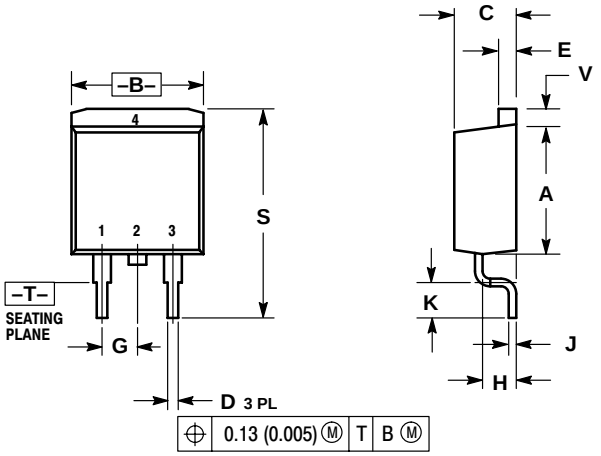
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN

PACKAGE DIMENSIONS

D²PAK
CASE 418B–03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

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