Complementary Silicon High-Power Transistors

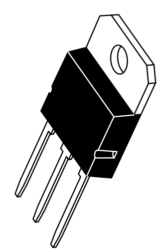
. . . for general–purpose power amplifier and switching applications.

- 25 A Collector Current
- Low Leakage Current —
  I_{CEO} = 1.0 mA @ 30 and 60 V
- Excellent DC Gain —
  h_{FE} = 40 Typ @ 15 A
- High Current Gain Bandwidth Product —
  $|h_{fe}|$ = 3.0 min @ I_C
  = 1.0 A, f = 1.0 MHz

NPN
TIP35A
TIP35B*
TIP35C*
PNP
TIP36A
TIP36B*
TIP36C*

***ON Semiconductor Preferred Device**

25 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60–100 VOLTS 125 WATTS



CASE 340D–02
TO–218AC

MAXIMUM RATINGS

Rating	Symbol	TIP35A TIP36A	TIP35B TIP36B	TIP35C TIP36C	Unit
Collector–Emitter Voltage	V_{CEO}	60 V	80 V	100 V	Vdc
Collector–Base Voltage	V_{CB}	60 V	80 V	100 V	Vdc
Emitter–Base Voltage	V_{EB}		5.0		Vdc
Collector Current — Continuous Peak (1)	I_C		25 40		Adc
Base Current — Continuous	I_B		5.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D		125 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		–65 to +150		°C
Unclamped Inductive Load	E_{SB}		90		mJ

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Junction–To–Free–Air Thermal Resistance	$R_{\theta JA}$	35.7	°C/W

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle ≤ 10%.

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

January, 2002 – Rev. 4

Publication Order Number:
TIP35A/D

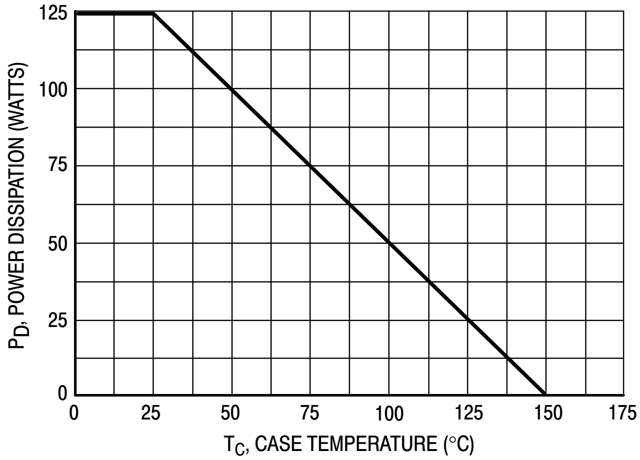


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mA, I_B = 0)	 TIP35A, TIP36A TIP35B, TIP36B TIP35C, TIP36C	$V_{CEO(sus)}$	 60 80 100	 — — —	Vdc
Collector–Emitter Cutoff Current (V_{CE} = 30 V, I_B = 0) (V_{CE} = 60 V, I_B = 0)	 TIP35A, TIP36A TIP35B, TIP35C, TIP36B, TIP36C	I_{CEO}	 — —	 1.0 1.0	mA
Collector–Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)		I_{CES}	—	0.7	mA
Emitter–Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)		I_{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.5 A, V_{CE} = 4.0 V) (I_C = 15 A, V_{CE} = 4.0 V)		h_{FE}	 25 15	 — 75	—
Collector–Emitter Saturation Voltage (I_C = 15 A, I_B = 1.5 A) (I_C = 25 A, I_B = 5.0 A)		$V_{CE(sat)}$	 — —	 1.8 4.0	Vdc
Base–Emitter On Voltage (I_C = 15 A, V_{CE} = 4.0 V) (I_C = 25 A, V_{CE} = 4.0 V)		$V_{BE(on)}$	 — —	 2.0 4.0	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 kHz)		h_{fe}	25	—	—
Current–Gain — Bandwidth Product (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 MHz)		f_T	3.0	—	MHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

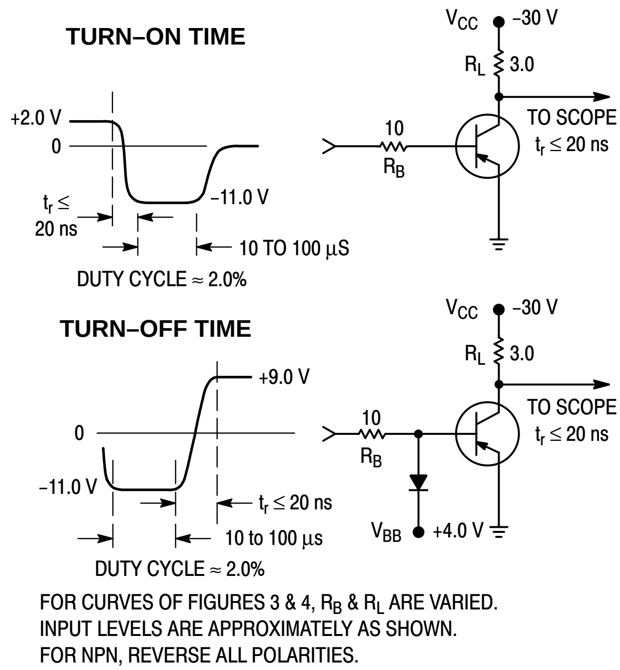


Figure 2. Switching Time Equivalent Test Circuits

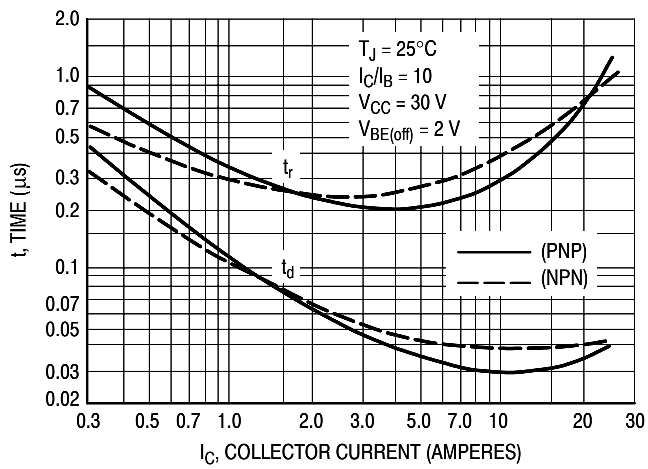


Figure 3. Turn−On Time

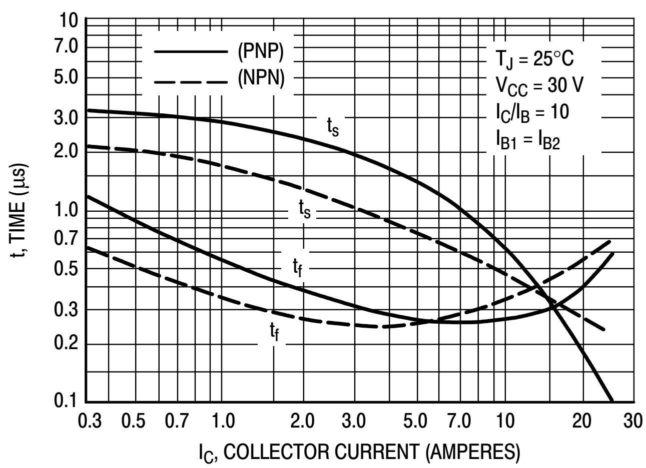


Figure 4. Turn−Off Time

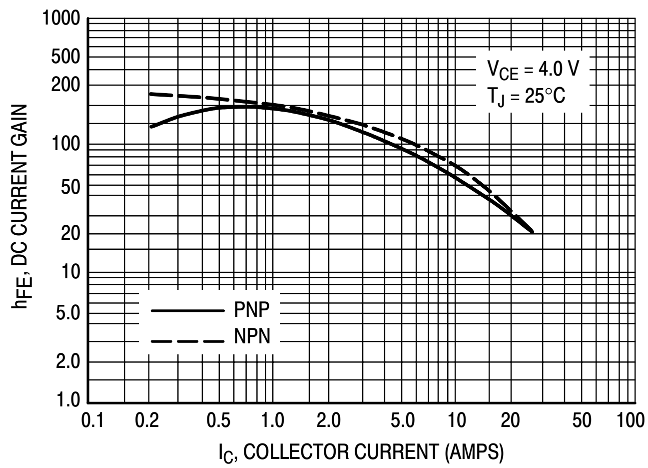


Figure 5. DC Current Gain

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives RBSOA characteristics.

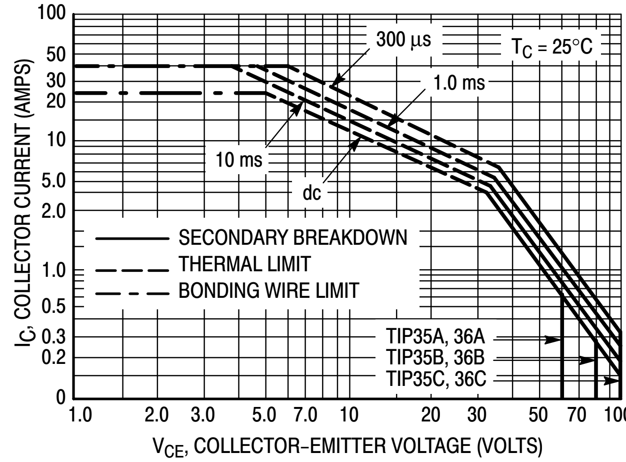


Figure 6. Maximum Rated Forward Bias Safe Operating Area

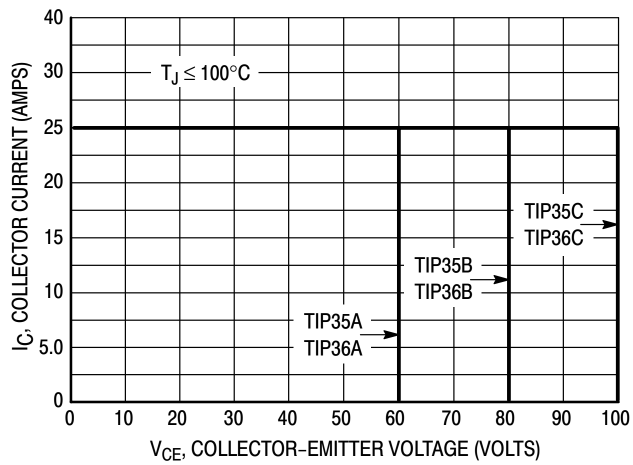
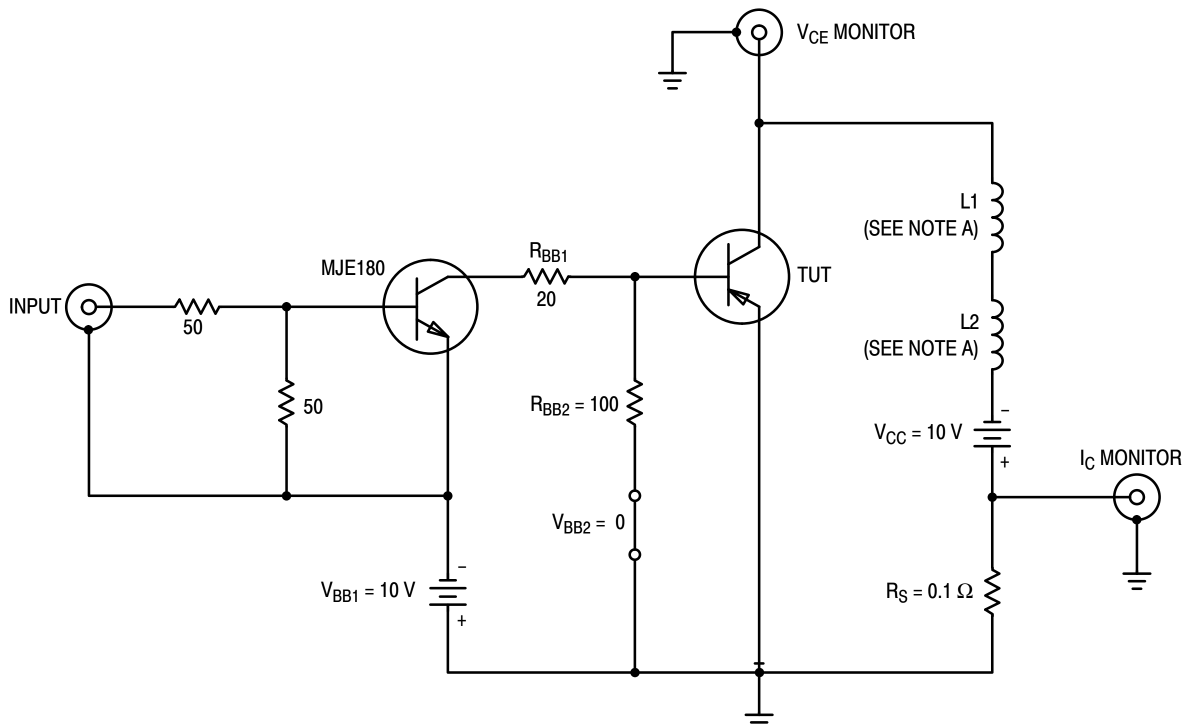
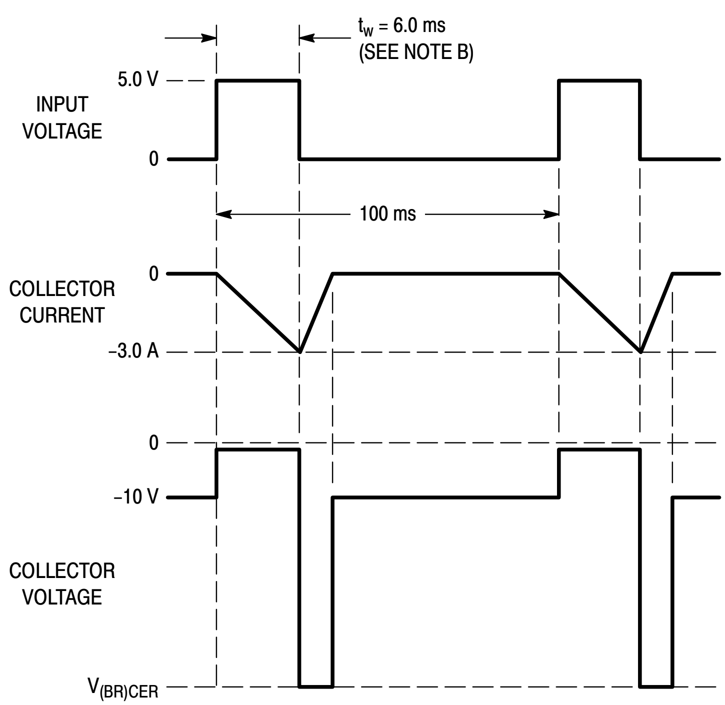


Figure 7. Maximum Rated Forward Bias Safe Operating Area

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



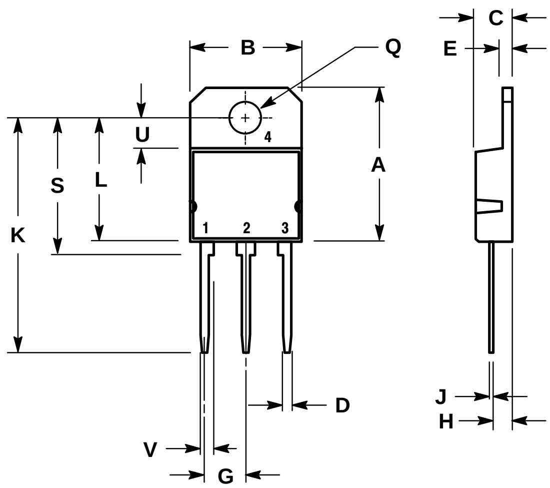
NOTES:

A. L1 and L2 are 10 mH, 0.11 Ω, Chicago Standard Transformer Corporation C–2688, or equivalent.
B. Input pulse width is increased until I_{CM} = –3.0 A.
C. For NPN, reverse all polarities.

Figure 8. Inductive Load Switching

PACKAGE DIMENSIONS

CASE 340D–02
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	---	16.20	---	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

Notes

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