

T-25-17

Triacs

Silicon Bidirectional Triode Thyristors

... designed primarily for industrial and military applications for the control of ac loads in applications such as light dimmers, power supplies, heating controls, motor controls, welding equipment and power switching systems; or wherever full-wave, silicon gate controlled solid-state devices are needed.

- Glass Passivated Junctions and Center Gate Fire
- Isolated Stud for Ease of Assembly
- Gate Triggering Guaranteed In All 4 Quadrants

**2N5441
thru
2N5446**

**TRIACs
40 AMPERES RMS
200 thru 600 VOLTS**



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage ($T_J = -65$ to $+110^\circ\text{C}$) 1/2 Sine Wave 50 to 60 Hz, Gate Open	VDRM		Volts
*Peak Principal Voltage 2N5441, 2N5444 2N5442, 2N5445 2N5443, 2N5446		200 400 600	
*RMS On-State Current (T_C per Figure 2) ($T_C = +100^\circ\text{C}$) Full Sine Wave, 50 to 60 Hz	$I_T(\text{RMS})$	40 20	Amps
*Peak Non-Repetitive Surge Current (One Full Cycle of surge current at 60 Hz, preceded and followed by a 40 A RMS current, $T_J = +110^\circ\text{C}$)	I_{TSM}	300	Amps
*Peak Gate Power (Pulse Width = 10 μs Max)	PGM	40	Watts
*Average Gate Power	$P_{G(\text{AV})}$	0.75	Watt
*Peak Gate Current (10 μs Max)	I_{GM}	4	Amps
*Peak Gate Voltage	VGM	30	Volts
*Operating Junction Temperature Range	T_J	-65 to +110	$^\circ\text{C}$
*Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
*Stud Torque	—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case 2N5441, 2N5442, 2N5443 2N5444, 2N5445, 2N5446	$R_{\theta\text{JC}}$	0.8 0.9 1	$^\circ\text{C/W}$

*Indicates JEDEC Registered Data



**CASE 263-04
STYLE 1
2N5444 thru 2N5446**



**CASE 310-02
STYLE 1
2N5441 thru 2N5443**

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2N5441 thru 2N5446

ELECTRICAL CHARACTERISTICS (T_C = 25°C, and either polarity of MT2 to MT1 voltage, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Forward or Reverse Blocking Current (Rated V _{DRM} or V _{RRM}) T _J = 25°C T _J = 110°C	I _{DRM} , I _{RRM}	—	— 0.5	10 4	μA mA
*Peak On-State Voltage (I _{TM} = 56 A Peak, Pulse Width ≤ 1 ms, Duty Cycle ≤ 2%)	V _{TM}	—	1.65	1.85	Volts
Gate Trigger Current (Continuous dc), Note 1 (Main Terminal Voltage = 12 Vdc, R _L = 50 Ohms)	I _{GT}	—	—	70	mA
MT2(+), G(+)	—	—	70		
MT2(+), G(-)	—	—	70		
MT2(-), G(-)	—	—	100		
MT2(-), G(+)	—	—	125		
*MT2(+), G(+); MT2(-), G(-) T _C = -65°C *MT2(+), G(-); MT2(-), G(+) T _C = -65°C	—	—	240		
*Gate Trigger Voltage (Continuous dc) (Main Terminal Voltage = 12 Vdc, R _L = 50 Ohms)	V _{GT}	—	—	—	Volts
MT2(+), G(+)	—	—	2		
MT2(+), G(-)	—	—	2		
MT2(-), G(-)	—	—	2		
MT2(-), G(+)	—	—	2.5		
*All Quadrants, T _C = -65°C *Main Terminal Voltage = Rated V _{DRM} = R _L = 10 k ohms, T _J = +110°C	—	0.2	—	3.4	—
*Holding Current (Main Terminal Voltage = 12 Vdc, Gate Open) (Initiating Current = 150 mA)	I _H	—	—	70 100	mA
T _C = 25°C *T _C = -65°C	—	—	—	—	
*Turn-On Time (Main Terminal Voltage = Rated V _{DRM} , I _{TM} = 56 A, Gate Source Voltage = 12 V, R _S = 12 Ohms, Rise Time = 0.1 μs, Pulse Width = 2 μs)	t _{gt}	—	1	2	μs
*Critical Rate-of-Rise of Commutation Voltage (Rated V _{DRM} , I _{TM} = 40 A, Commutating di/dt = 22 A/ms, gate energized)	dv/dt(c)	—	—	—	V/μs
T _C = 70°C 2N5441, 2N5442, 2N5443	5	30	—		
= 65°C 2N5444, 2N5445, 2N5446	5	30	—		
Critical Rate-of-Rise of Off State Voltage (Rated V _{DRM} , Exponential Voltage Rise, Gate Open, T _C = 110°C)	dv/dt	—	—	—	V/μs
2N5441, 2N5444	50	—	—		
2N5442, 2N5445	30	—	—		
2N5443, 2N5446	20	—	—		

*Indicates JEDEC Registered Data for 2N5541 thru 2N5446.
Note 1. All voltage polarities referenced to main terminal 1.

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2N5441 thru 2N5446

FIGURE 1 - ON-STATE POWER DISSIPATION

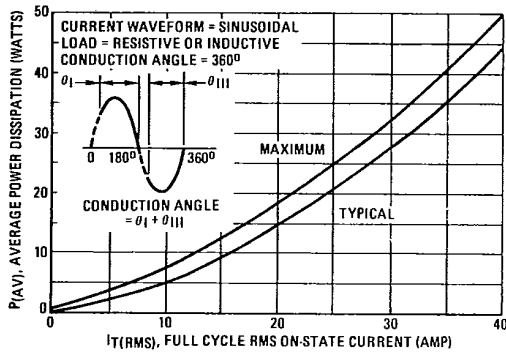


FIGURE 2 - RMS CURRENT DERATING

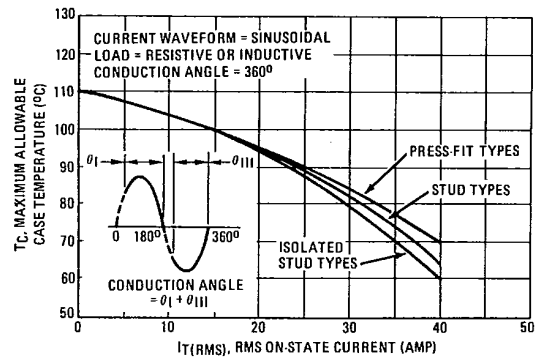


FIGURE 3 - TYPICAL GATE TRIGGER VOLTAGE

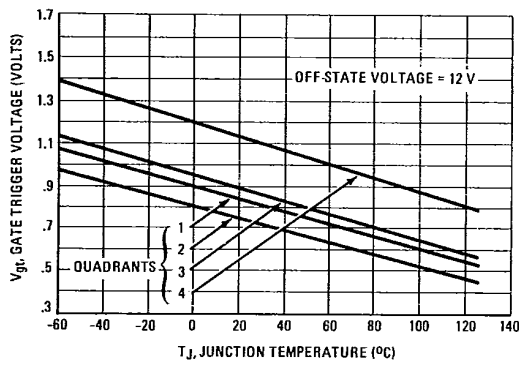


FIGURE 4 - TYPICAL GATE TRIGGER CURRENT

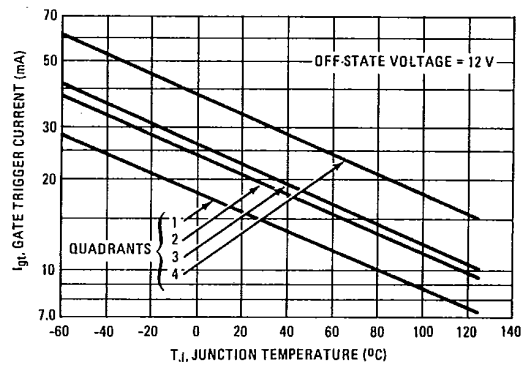
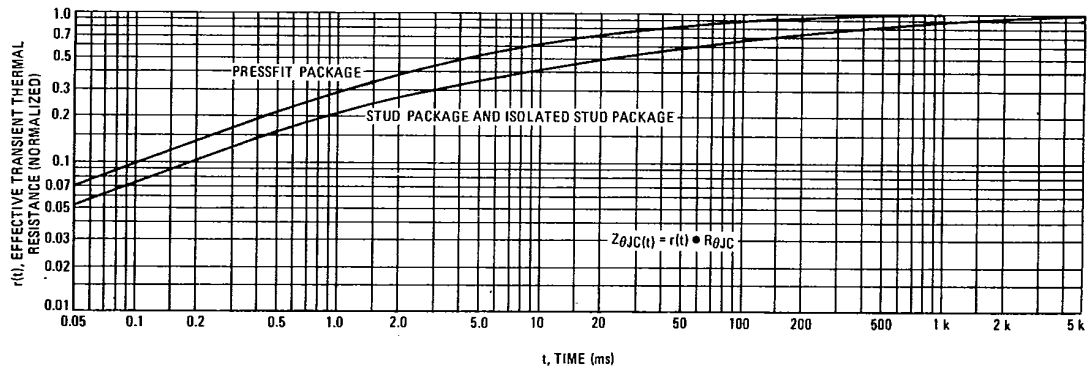


FIGURE 5 - TYPICAL THERMAL RESPONSE



2N5441 thru 2N5446

FIGURE 6 - ON-STATE CHARACTERISTICS

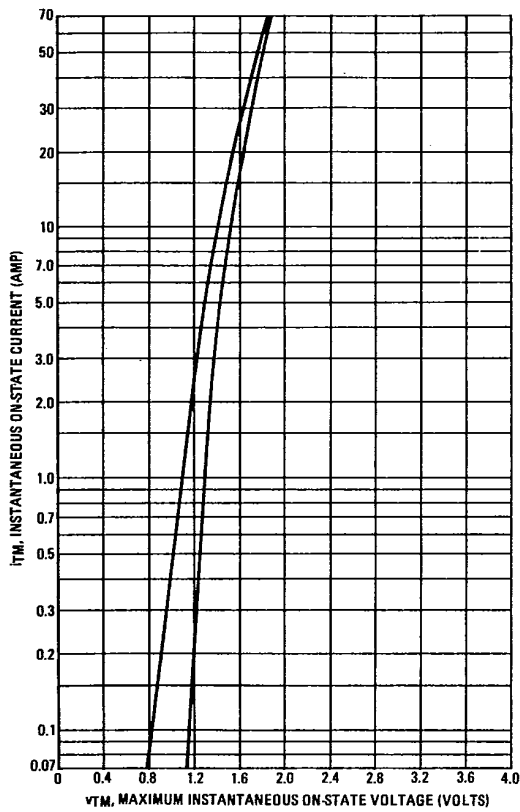


FIGURE 7 - TYPICAL HOLDING CURRENT

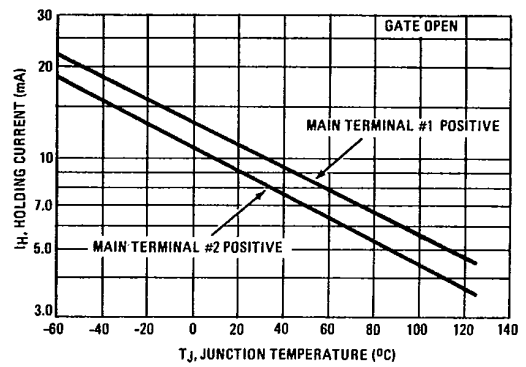
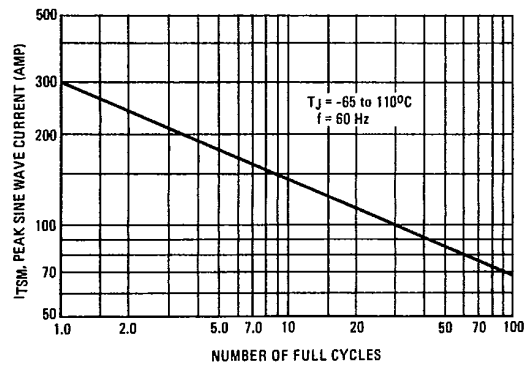


FIGURE 8 - MAXIMUM ALLOWABLE SURGE CURRENT



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