2N6071A,B*
2N6073A,B*
2N6075A,B*

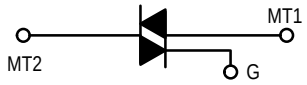
***Motorola preferred devices**

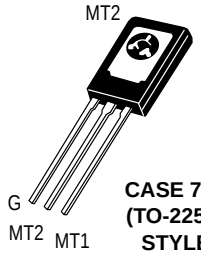
Sensitive Gate Triacs
Silicon Bidirectional Thyristors

. . . designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Sensitive Gate Triggering Uniquely Compatible for Direct Coupling to TTL, HTL, CMOS and Operational Amplifier Integrated Circuit Logic Functions
- Gate Triggering 4 Mode — 2N6071A,B, 2N6073A,B, 2N6075A,B
- Blocking Voltages to 600 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermopad Construction for Low Thermal Resistance, High Heat Dissipation and Durability

TRIACs
4 AMPERES RMS
200 thru 600 VOLTS





CASE 77-08
(TO-225AA)
STYLE 5

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage(1) (Gate Open, T_J = 25 to 110°C) 2N6071A,B 2N6073A,B 2N6075A,B	V_{DRM}	 200 400 600	Volts
*On-State Current RMS (T_C = 85°C)	$I_{T(RMS)}$	4	Amps
*Peak Surge Current (One Full cycle, 60 Hz, T_J = –40 to +110°C)	I_{TSM}	30	Amps
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	3.7	A^2s
*Peak Gate Power	P_{GM}	10	Watts
*Average Gate Power	$P_{G(AV)}$	0.5	Watt
*Peak Gate Voltage	V_{GM}	5	Volts

*Indicates JEDEC Registered Data.

1. V_{DRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
*Operating Junction Temperature Range	T_J	–40 to +110	°C
*Storage Temperature Range	T_{stg}	–40 to +150	°C
Mounting Torque (6-32 Screw)(1)	—	8	in. lb.

*Indicates JEDEC Registered Data.

1. Torque rating applies with use of compression washer (B52200F006). Mounting torque in excess of 6 in. lb. does not appreciably lower case-to-sink thermal resistance. Main terminal 2 and heatsink contact pad are common.
   For soldering purposes (either terminal connection or device mounting), soldering temperatures shall not exceed +200°C, for 10 seconds. Consult factory for lead bending options.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W

*Indicates JEDEC Registered Data.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

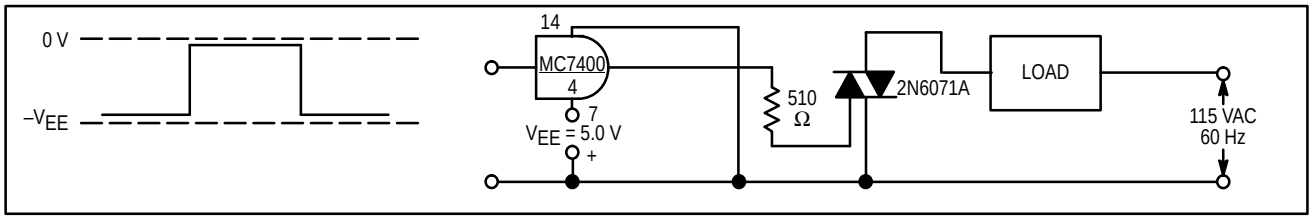
Characteristic	Symbol	Min	Typ	Max	Unit
*Peak Blocking Current	I_{DRM}				
(V_D = Rated V_{DRM}, gate open, T_J = 25°C)		—	—	10	μA
(T_J = 110°C)		—	—	2	mA
*On-State Voltage (Either Direction)	V_{TM}	—	—	2	Volts
(I_{TM} = 6 A Peak)					
*Peak Gate Trigger Voltage (Continuous dc)	V_{GT}				Volts
(Main Terminal Voltage = 12 Vdc, R_L = 100 Ohms, T_J = –40°C)					
MT2(+), G(+); MT2(–), G(–) All Types		—	1.4	2.5	
MT2(+), G(–); MT2(–), G(+)		—	1.4	2.5	
(Main Terminal Voltage = Rated V_{DRM}, R_L = 10 k ohms, T_J = 110°C)					
MT2(+), G(+); MT2(–), G(–) All Types		0.2	—	—	
MT2(+), G(–); MT2(–), G(+)		0.2	—	—	
*Holding Current (Either Direction)	I_H				mA
(Main Terminal Voltage = 12 Vdc, Gate Open, T_J = –40°C)					
(Initiating Current = 1 Adc) 2N6071A,B, 2N6073A,B, 2N6075A,B		—	—	30	
(T_J = 25°C) 2N6071A,B, 2N6073A,B, 2N6075A,B		—	—	15	
Turn-On Time (Either Direction)	t_{on}	—	1.5	—	μs
(I_{TM} = 14 Adc, I_{GT} = 100 mAdc)					
Blocking Voltage Application Rate at Commutation	dv/dt(c)	—	5	—	V/μs
@ V_{DRM}, T_J = 85°C, Gate Open, I_{TM} = 5.7 A, Commutating di/dt = 2.0 A/ms					

*Indicates JEDEC Registered Data.

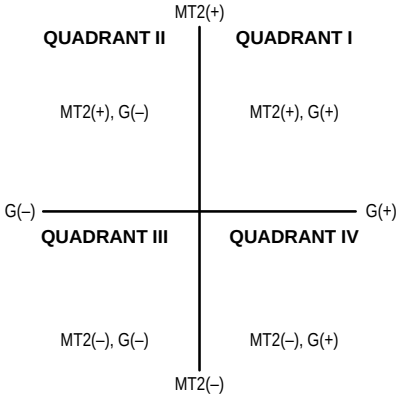
			QUADRANT (See Definition Below)			
	Type	I_{GT} @ T_J	I mA	II mA	III mA	IV mA
Gate Trigger Current (Continuous dc) (Main Terminal Voltage = 12 Vdc, R_L = 100 ohms) Maximum Value	2N6071A 2N6073A 2N6075A	+25°C	5	5	5	10
		–40°C	20	20	20	30
	2N6071B 2N6073B 2N6075B	+25°C	3	3	3	5
		–40°C	15	15	15	20

*Indicates JEDEC Registered Data.

SAMPLE APPLICATION: TTL-SENSITIVE GATE 4 AMPERE TRIAC TRIGGERS IN MODES II AND III



QUADRANT DEFINITIONS



Trigger devices are recommended for gating on Triacs. They provide:

1. Consistent predictable turn-on points.
2. Simplified circuitry.
3. Fast turn-on time for cooler, more efficient and reliable operation.

SENSITIVE GATE LOGIC REFERENCE

IC Logic Functions	Firing Quadrant			
	I	II	III	IV
TTL		2N6071A Series	2N6071A Series	
HTL		2N6071A Series	2N6071A Series	
CMOS (NAND)	2N6071B Series			2N6071B Series
CMOS (Buffer)		2N6071B Series	2N6071B Series	
Operational Amplifier	2N6071A Series			2N6071A Series
Zero Voltage Switch		2N6071A Series	2N6071A Series	

FIGURE 1 – AVERAGE CURRENT DERATING

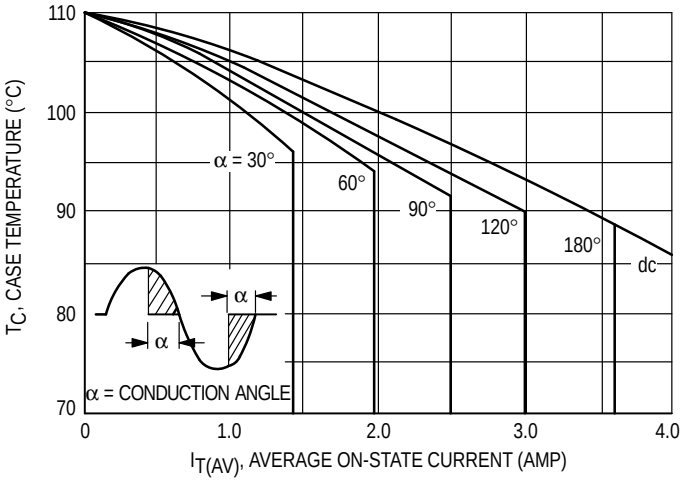


FIGURE 2 – RMS CURRENT DERATING

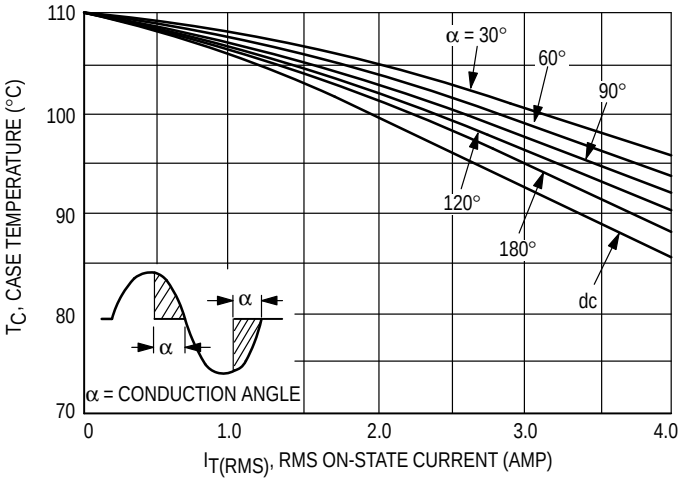


FIGURE 3 – POWER DISSIPATION

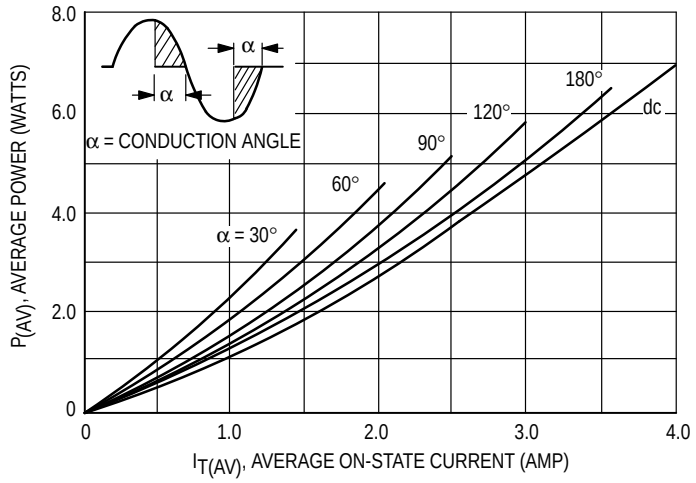


FIGURE 4 – POWER DISSIPATION

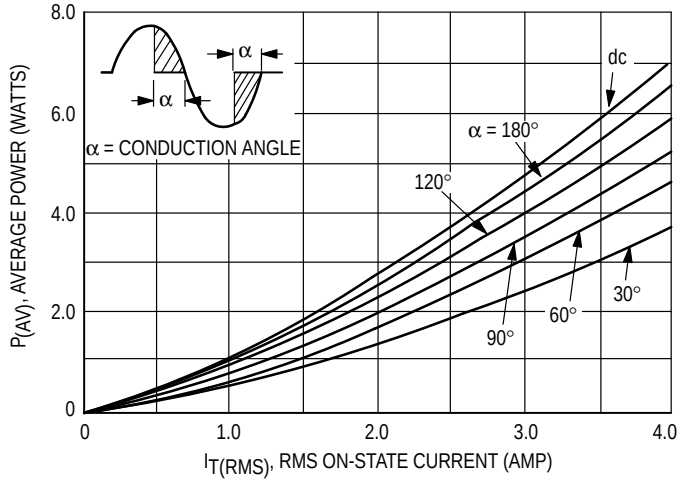


FIGURE 5 – TYPICAL GATE-TRIGGER VOLTAGE

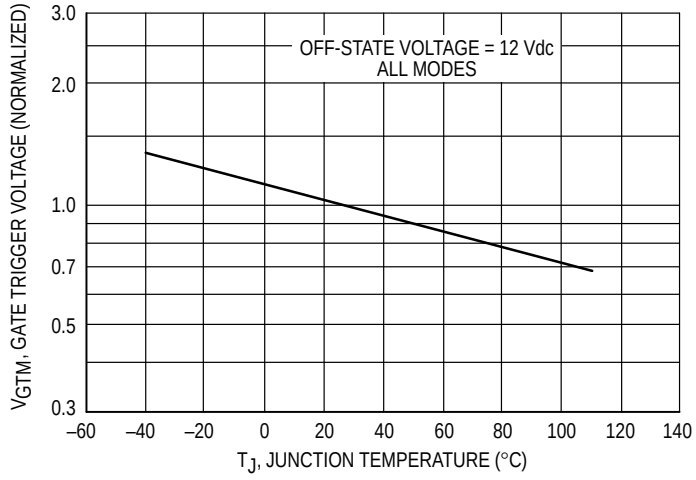


FIGURE 6 – TYPICAL GATE-TRIGGER CURRENT

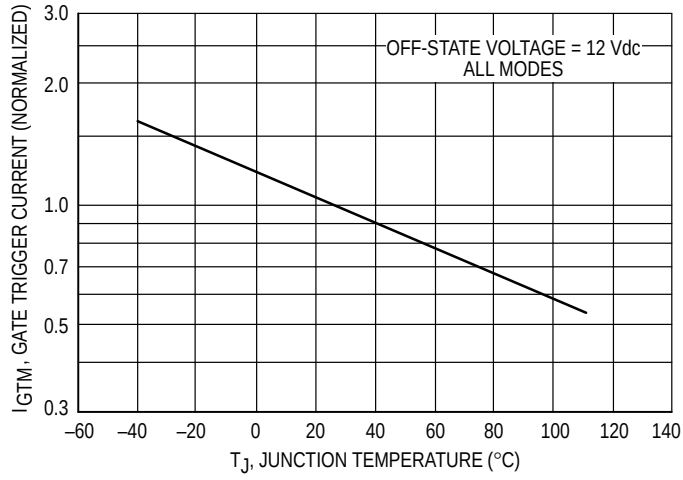


FIGURE 7 – MAXIMUM ON-STATE CHARACTERISTICS

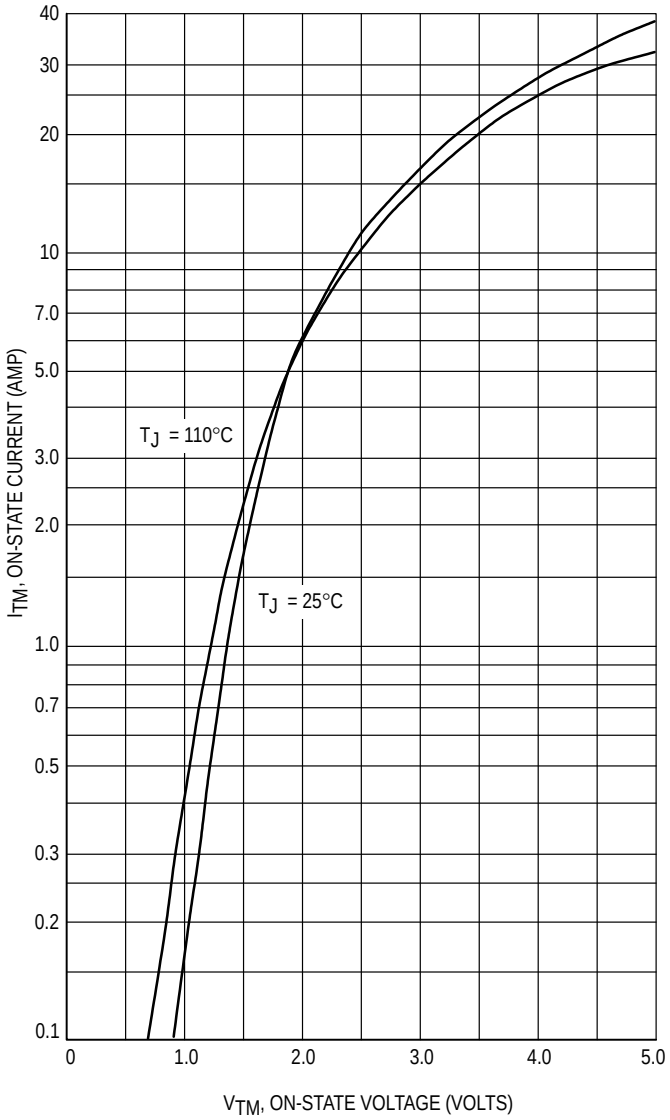


FIGURE 8 – TYPICAL HOLDING CURRENT

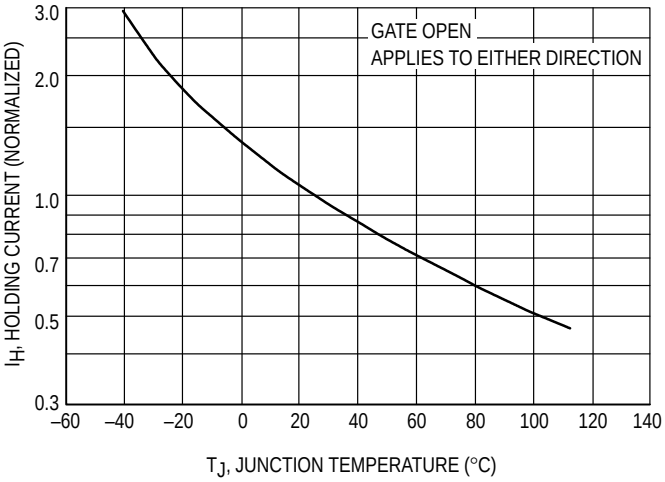


FIGURE 9 – MAXIMUM ALLOWABLE SURGE CURRENT

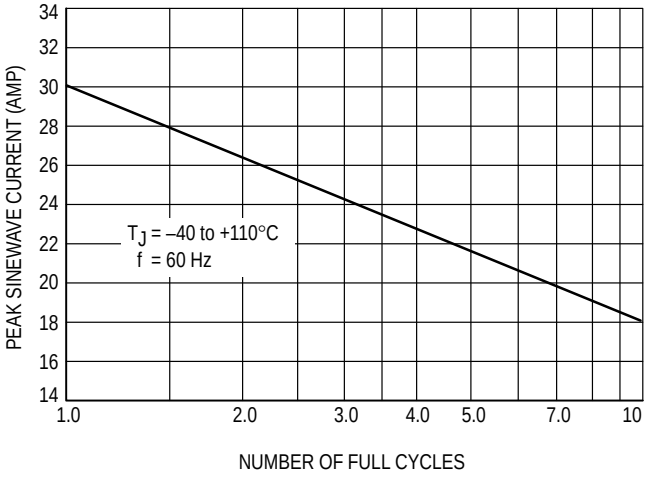
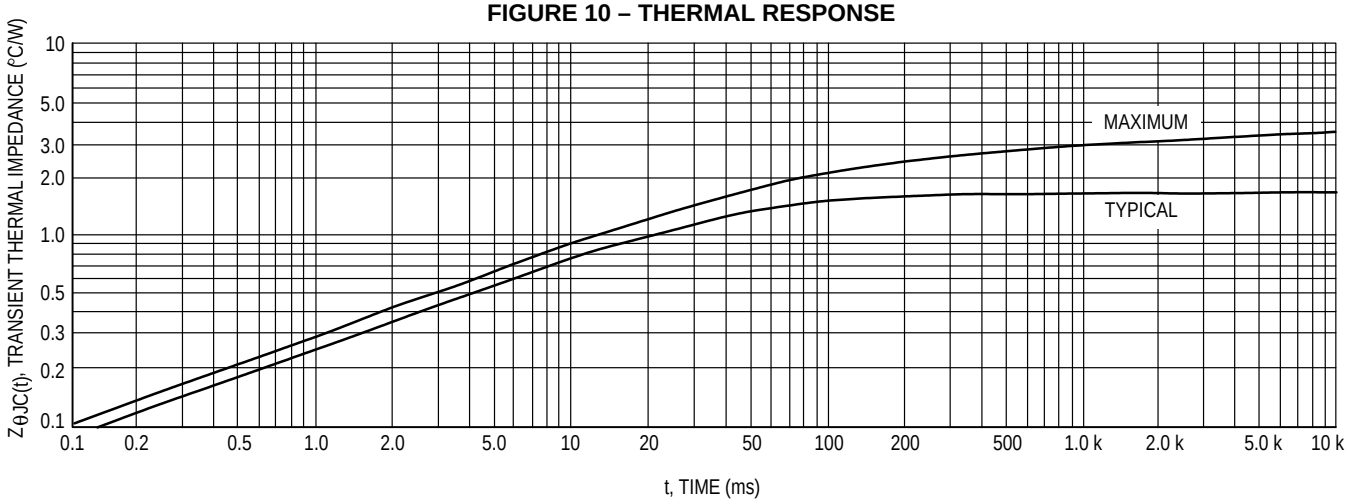
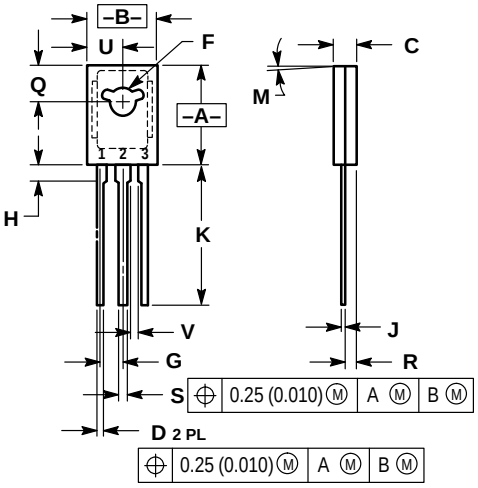


FIGURE 10 – THERMAL RESPONSE



PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	—	1.02	—

STYLE 5:
PIN 1. MT 1
2. MT 2
3. GATE

CASE 77–09
(TO–225AA)
ISSUE W

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