



OCTAL D FLIP-FLOP WITH ENABLE; HEX D FLIP-FLOP WITH ENABLE; 4-BIT D FLIP-FLOP WITH ENABLE

The SN54/74LS377 is an 8-bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

The SN54/74LS378 is a 6-Bit Register with a buffered common enable. This device is similar to the SN54/74LS174, but with common Enable rather than common Master Reset.

The SN54/74LS379 is a 4-Bit Register with buffered common Enable. This device is similar to the SN54/74LS175 but features the common Enable rather than common Master Reset.

- 8-Bit High Speed Parallel Registers
- Positive Edge-Triggered D-Type Flip Flops
- Fully Buffered Common Clock and Enable Inputs
- True and Complement Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

PIN NAMES

| | |
|--------------------------------|--------------------------------------|
| \bar{E} | Enable (Active LOW) Input |
| D ₀ -D ₃ | Data Inputs |
| CP | Clock (Active HIGH Going Edge) Input |
| Q ₀ -Q ₃ | True Outputs (Note b) |
| Q ₀ -Q ₃ | Complemented Outputs (Note b) |

LOADING (Note a)

| | HIGH | LOW |
|--------------------------------|----------|--------------|
| \bar{E} | 0.5 U.L. | 0.25 U.L. |
| D ₀ -D ₃ | 0.5 U.L. | 0.25 U.L. |
| CP | 0.5 U.L. | 0.25 U.L. |
| Q ₀ -Q ₃ | 10 U.L. | 5 (2.5) U.L. |
| Q ₀ -Q ₃ | 10 U.L. | 5 (2.5) U.L. |

NOTES:

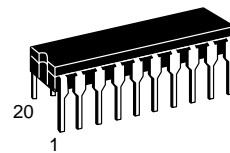
a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

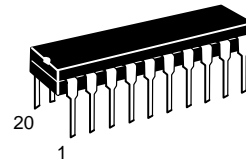
SN54/74LS377
SN54/74LS378
SN54/74LS379

**OCTAL D FLIP-FLOP WITH
ENABLE; HEX D FLIP-FLOP
WITH ENABLE; 4-BIT D FLIP-FLOP
WITH ENABLE**

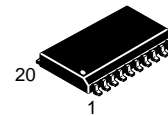
LOW POWER SCHOTTKY



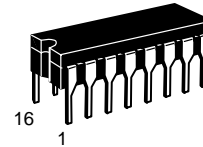
J SUFFIX
CERAMIC
CASE 732-03



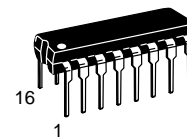
N SUFFIX
PLASTIC
CASE 738-03



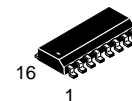
DW SUFFIX
SOIC
CASE 751D-03



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

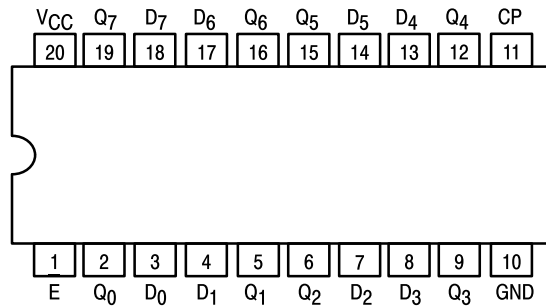
ORDERING INFORMATION

| | |
|-------------|---------|
| SN54LSXXXJ | Ceramic |
| SN74LSXXXN | Plastic |
| SN74LSXXXDW | SOIC |
| SN74LSXXXD | SOIC |

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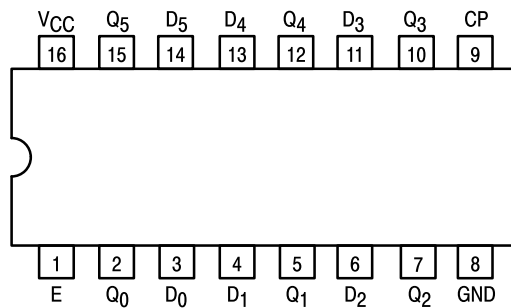
CONNECTION DIAGRAM DIPS (TOP VIEW)

SN54/74LS377



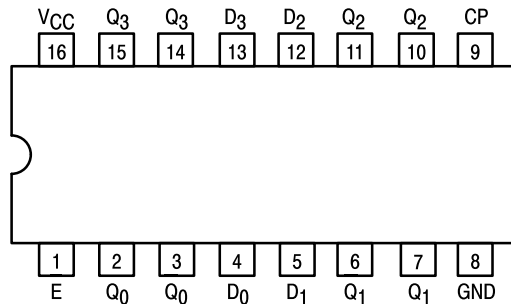
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS378



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS379

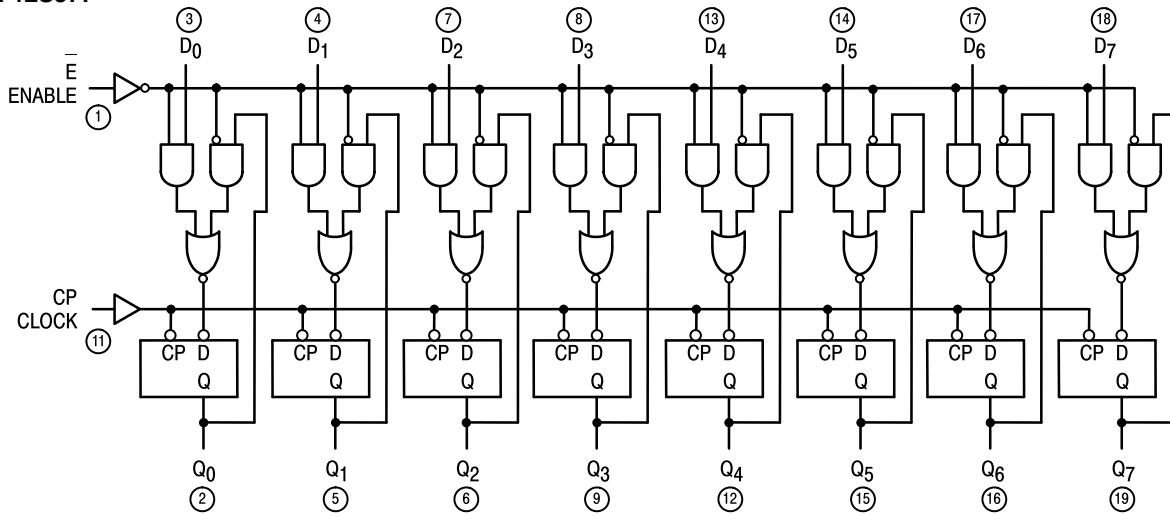


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

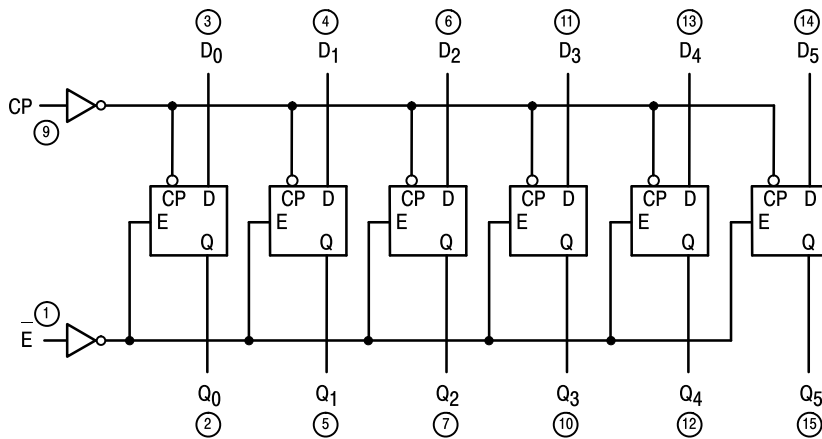
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LOGIC DIAGRAMS

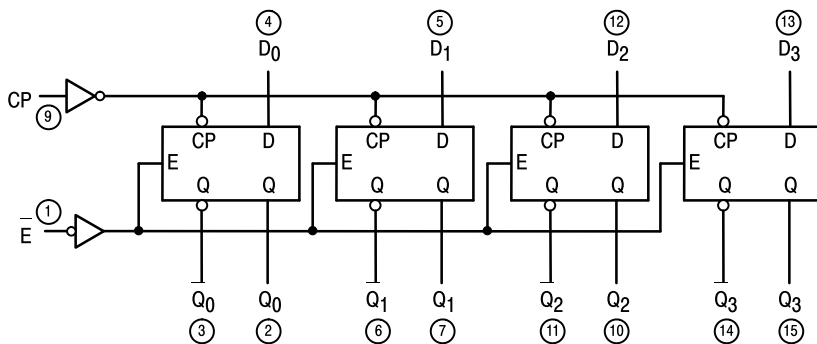
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GUARANTEED OPERATING RANGES

| Symbol | Parameter | | Min | Typ | Max | Unit |
|----------|-------------------------------------|----------|-------------|------------|-------------|------|
| V_{CC} | Supply Voltage | 54 74 | 4.5 4.75 | 5.0 5.0 | 5.5 5.25 | V |
| T_A | Operating Ambient Temperature Range | 54 74 | -55 0 | 25 25 | 125 70 | °C |
| I_{OH} | Output Current — High | 54, 74 | | | -0.4 | mA |
| I_{OL} | Output Current — Low | 54 74 | | | 4.0 8.0 | mA |

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter | Limits | | | Unit | Test Conditions | |
|----------|--------------------------------|--------|-------|------|---------------|---|---|
| | | Min | Typ | Max | | | |
| V_{IH} | Input HIGH Voltage | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| V_{IL} | Input LOW Voltage | 54 | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs | |
| | | 74 | | 0.8 | | | |
| V_{IK} | Input Clamp Diode Voltage | | -0.65 | -1.5 | V | $V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$ | |
| V_{OH} | Output HIGH Voltage | 54 | 2.5 | 3.5 | V | $V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table | |
| | | 74 | 2.7 | 3.5 | V | | |
| V_{OL} | Output LOW Voltage | 54, 74 | | 0.25 | 0.4 | V | $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | |
| I_{IH} | Input HIGH Current | | | 20 | μA | $V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$ | |
| | | | | 0.1 | mA | $V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$ | |
| I_{IL} | Input LOW Current | | | -0.4 | mA | $V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$ | |
| I_{OS} | Short Circuit Current (Note 1) | -20 | | -100 | mA | $V_{CC} = \text{MAX}$ | |
| I_{CC} | Power Supply Current | LS377 | | 28 | mA | $V_{CC} = \text{MAX}$, NOTE 1 | |
| | | LS378 | | 22 | | | |
| | | LS379 | | 15 | | | |

NOTE: With all inputs open and GND applied to all data and enable inputs, I_{CC} is measured after a momentary GND, then 4.5 V is applied to clock.

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|------------------|---------------------------------------|--------|-----|-----|------|---|
| | | Min | Typ | Max | | |
| f_{MAX} | Maximum Clock Frequency | 30 | 40 | | MHz | $V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$ |
| t_{PLH} | Propagation Delay, Clock to Output | | 17 | 27 | ns | |
| t_{PHL} | | | 18 | 27 | | |

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|--------|-------------------|------------------|-----|-----|------|--------------------------|
| | | Min | Typ | Max | | |
| t_W | Any Pulse Width | 20 | | | ns | $V_{CC} = 5.0 \text{ V}$ |
| t_S | Data Setup Time | 20 | | | ns | |
| t_s | Enable Setup Time | Inactive — State | 10 | | ns | |
| | | Active — State | 25 | | ns | |
| t_h | Any Hold Time | 5.0 | | | ns | |

DEFINITION OF TERMS




SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following

the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

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TRUTH TABLE

| \bar{E} | CP | D_n | Q_n | \bar{Q}_n |
|-----------|---|-------|-----------|-------------|
| H |  | X | No Change | No Change |
| L |  | H | H | L |
| L |  | L | L | H |

L = LOW Voltage Level
 H = HIGH Voltage Level
 X = Immaterial

AC WAVEFORMS

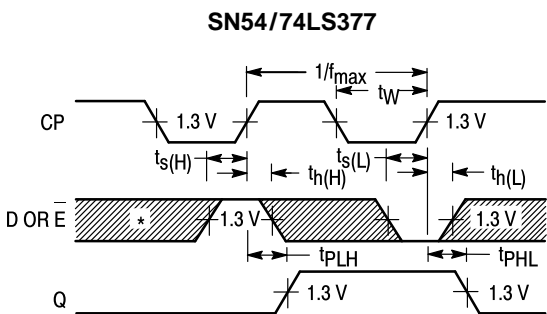


Figure 1. Clock to Output Delays Clock Pulse Width, Frequency, Setup and Hold Times Data or Enable to Clock

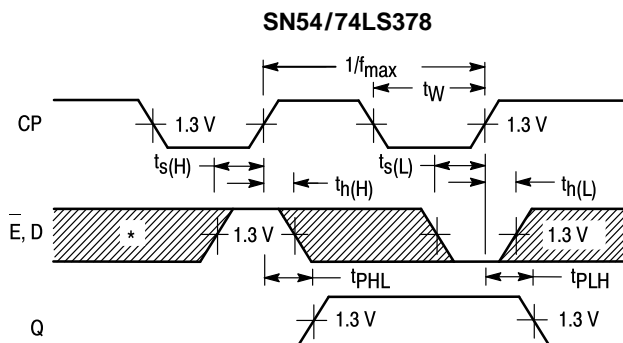
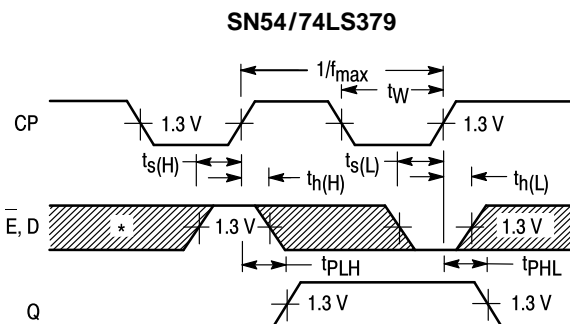


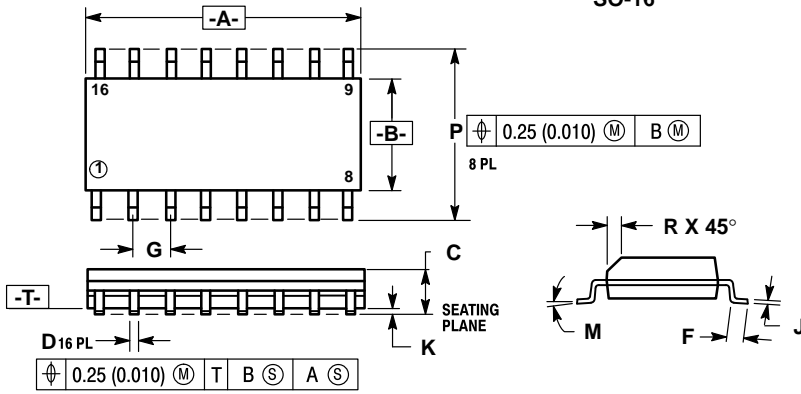
Figure 2. Clock to Output Delays Clock Pulse Width, Frequency, Setup and Hold Times Data or Enable to Clock



*The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 3. Clock to Output Delays Clock Pulse Width, Frequency, Setup and Hold Times Data, Enable to Clock

**Case 751B-03 D Suffix
16-Pin Plastic
SO-16**

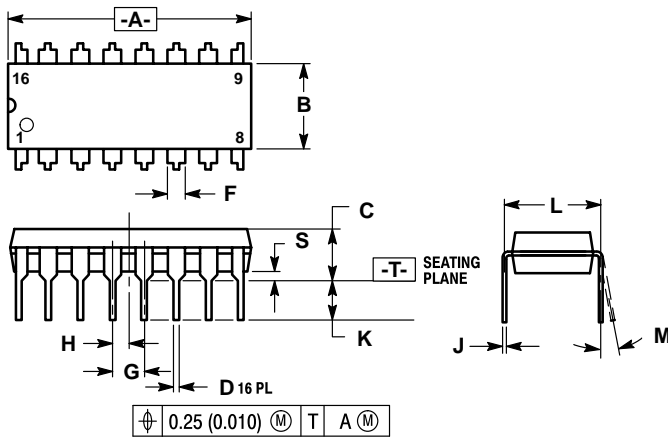


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

**Case 648-08 N Suffix
16-Pin Plastic**

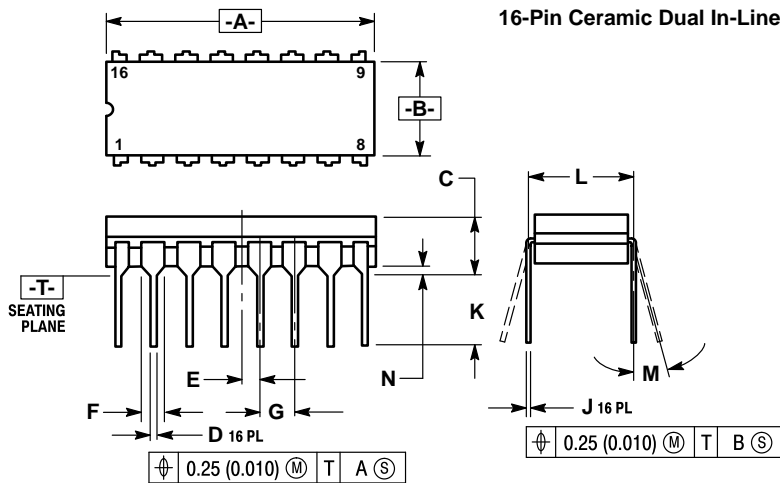


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.
6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 18.80 | 19.55 | 0.740 | 0.770 |
| B | 6.35 | 6.85 | 0.250 | 0.270 |
| C | 3.69 | 4.44 | 0.145 | 0.175 |
| D | 0.39 | 0.53 | 0.015 | 0.021 |
| F | 1.02 | 1.77 | 0.040 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.27 BSC | | 0.050 BSC | |
| J | 0.21 | 0.38 | 0.008 | 0.015 |
| K | 2.80 | 3.30 | 0.110 | 0.130 |
| L | 7.50 | 7.74 | 0.295 | 0.305 |
| M | 0° | 10° | 0° | 10° |
| S | 0.51 | 1.01 | 0.020 | 0.040 |

**Case 620-09 J Suffix
16-Pin Ceramic Dual In-Line**



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 19.05 | 19.55 | 0.750 | 0.770 |
| B | 6.10 | 7.36 | 0.240 | 0.290 |
| C | — | 4.19 | — | 0.165 |
| D | 0.39 | 0.53 | 0.015 | 0.021 |
| E | 1.27 BSC | | 0.050 BSC | |
| F | 1.40 | 1.77 | 0.055 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.23 | 0.27 | 0.009 | 0.011 |
| K | — | 5.08 | — | 0.200 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.39 | 0.88 | 0.015 | 0.035 |

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