

Application Note

AN2533/D  
Rev. 0, 5/2003

Standard Space Vector  
Modulation – 3 outputs  
version – XOR version TPU  
Function Set (svmStd3Xor)



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Functional Overview

Standard Space Vector Modulation – 3 outputs version – XOR version (svmStd3Xor) is a version of the Standard Space Vector Modulation – 3 output version (svmStd3) function that uses two TPU channels to generate one PWM output channel. The TPU channel outputs are connected to an XOR gate whose output is the required PWM signal. See Figure 1. An advantage of this solution is the full range 0% to 100% of PWM duty-cycle ratios. There is no MPW (minimum pulse width) parameter to limit the edge duty-cycle ratios in this version, unlike in the svmStd3. A disadvantage is that the number of assigned TPU channels is doubled.

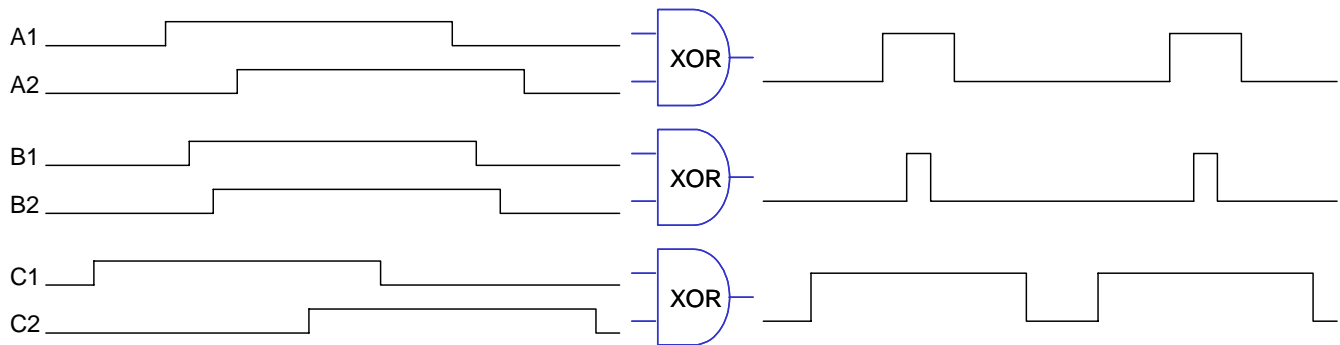


Figure 1. Functionality of XOR version – illustration

The function set consists of 5 TPU functions:

- Standard Space Vector Modulation – 3 outputs version – XOR version – R channels (svmStd3Xor\_R)
- Standard Space Vector Modulation – 3 outputs version – XOR version – T channels (svmStd3Xor\_T)

- Synchronization Signal for Standard Space Vector Modulation – 3 outputs version – XOR version (svmStd3Xor\_sync)
- Resolver Reference Signal for Standard Space Vector Modulation – 3 outputs version – XOR version (svmStd3Xor\_res)
- Fault Input for Standard Space Vector Modulation – 3 outputs version – XOR version (svmStd3Xor\_fault)

The svmStd3Xor function generates 3 pairs of XOR gate input signals. The XOR gate outputs then produce a 3-channel 3-phase center-aligned PWM signal. The generated signals control external hardware, which outputs pair of transistor signals (top and bottom) with dead-time inserted. The Synchronization Signal for the svmStd3Xor function can be used to generate one or more adjustable signals for a wide range of uses, that are synchronized to the PWM, and track changes in the PWM period. The Resolver Reference Signal for the svmStd3Xor function can be used to generate one or more 50% duty-cycle adjustable signals that are also synchronized to the PWM. The Fault Input for the svmStd3Xor function is a TPU input function that sets all XOR gate outputs low when the input signal goes low.

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## Function Set Configuration

None of the TPU functions in the Standard Space Vector Modulation – 3 outputs version – XOR version TPU function set can be used separately. The svmStd3Xor\_R and svmStd3Xor\_T functions have to be used together. The svmStd3Xor\_R runs on pins A1, B1, C1, and the svmStd3Xor\_T runs on pins A2, B2, C2 – see [Figure 1](#). One or more channels running Synchronization Signal for svmStd3Xor as well as Resolver Reference Signals for svmStd3Xor functions can be added to the svmStd3Xor\_R and svmStd3Xor\_T functions. They can run with different settings on each channel. The function Fault Input for svmStd3Xor can also be added to the svmStd3Xor\_R and svmStd3Xor\_T functions. It is recommended to use it on channel 15, and to set the hardware option that disables all TPU output pins when the channel 15 input signal is low (DTPU bit = 1). This ensures that the hardware reacts quickly to a pin fault state. Note that it is not only the svmStd3Xor\_R and svmStd3Xor\_T channels, but all TPU output channels, including the synchronization signals, that are disabled in this configuration.

[Table 1](#) shows the configuration options and restrictions.

**Table 1. svmStd3Xor TPU function set configuration options and restrictions**

TPU function	Optional/Mandatory	How many channels	Assignable channels
svmStd3Xor_R	mandatory	3	any 3 channels
svmStd3Xor_T	mandatory	3	any 3 channels
svmStd3Xor_sync	optional	1 or more	any channels
svmStd3Xor_res	optional	1 or more	any channels
svmStd3Xor_fault	optional	1	any, recommended is 15 and DTPU bit set

**Table 2** shows an example of configuration.

**Table 2. Example of configuration**

Channel	TPU function	Priority
0	svmStd3Xor_R	middle
1	svmStd3Xor_T	middle
2	svmStd3Xor_R	middle
3	svmStd3Xor_T	middle
4	svmStd3Xor_R	middle
5	svmStd3Xor_T	middle
13	svmStd3Xor_sync	low
14	svmStd3Xor_res	low
15	svmStd3Xor_fault	high

**Table 3** shows the TPU function code sizes.

**Table 3. TPU function code sizes.**

TPU function	Code size
svmStd3Xor_R	216 $\mu$ instructions + 8 entries = 224 long words
svmStd3Xor_T	3 $\mu$ instructions + 8 entries = 11 long words
svmStd3Xor_sync	26 $\mu$ instructions + 8 entries = 34 long words
svmStd3Xor_res	38 $\mu$ instructions + 8 entries = 46 long words
svmStd3Xor_fault	9 $\mu$ instructions + 8 entries = 17 long words

**Configuration Order** The CPU configures the TPU as follows.

1. Disables the channels by clearing the two channel priority bits on each channel used (not necessary after reset).
2. Selects the channel functions on all used channels by writing the function numbers to the channel function select bits.

3. Initializes function parameters. The parameters  $T$ ,  $prescaler$ ,  $SQRT3$ ,  $CPU14$  and  $sync\_presc\_addr$  must be set before initialization. If an  $svmStd3Xor\_sync$  channel or an  $svmStd3Xor\_res$  channel is used, then its parameters must also be set before initialization.
4. Issues an HSR (Host Service Request) type %10 to one of the  $svmStd3Xor\_R$  channels to initialize all  $svmStd3Xor\_R$  and  $svmStd3Xor\_T$  channels. Issues an HSR type %10 to the  $svmStd3Xor\_sync$  channels,  $svmStd3Xor\_res$  channels and  $svmStd3Xor\_fault$  channel, if used.
5. Enables servicing by assigning high, middle or low priority to the channel priority bits. All  $svmStd3Xor\_R$  and  $svmStd3Xor\_T$  channels must be assigned the same priority to ensure correct operation. The CPU must ensure that the  $svmStd3Xor\_sync$  or  $svmStd3Xor\_res$  channels are initialized after the initialization of the  $svmStd3Xor\_R$  and  $svmStd3Xor\_T$  channels:
  - assign a priority to the  $svmStd3Xor\_R$  and  $svmStd3Xor\_T$  channels to enable their initialization
  - if a Synchronization Signal or a Resolver Reference Signal channel is used, wait until the HSR bits are cleared to indicate that initialization of the  $svmStd3Xor\_R$  and  $svmStd3Xor\_T$  channels has completed and
  - assign a priority to the  $svmStd3Xor\_sync$  or  $svmStd3Xor\_res$  channels to enable their initialization

**NOTE:** A CPU routine that configures the TPU can be generated automatically using the MPC500\_Quick\_Start Graphical Configuration Tool.

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## Detailed Function Description

**Standard Space Vector Modulation – 3 outputs version – XOR version – R channels (svmStd3Xor\_R) and Standard Space Vector Modulation – 3 outputs version – XOR version – T channels (svmStd3Xor\_T)**

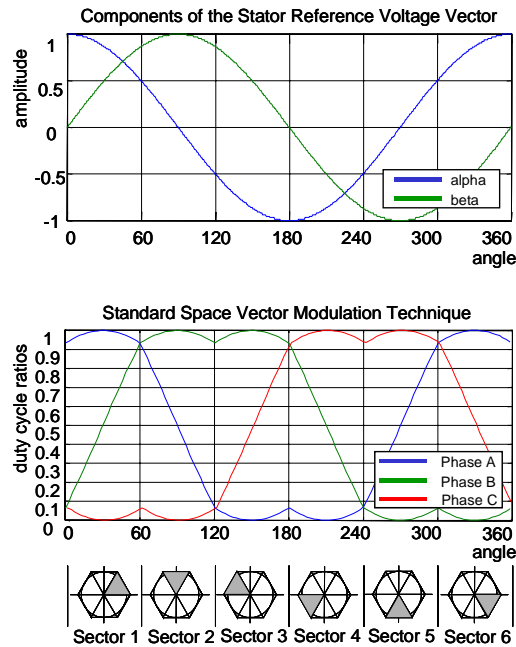
The  $svmStd3Xor\_R$  and  $svmStd3Xor\_T$  TPU functions work together to generate 3 pairs of XOR gate inputs. The XOR gate outputs then produce a 3-channel 3-phase center-aligned PWM signal. Unlike the  $svmStd$ , the generated signals are not top-bottom pairs with dead-times but only top-like signals without dead-times. In order to charge the bootstrap transistors, the PWM signals start to run 1.6ms after their initialization (at 20MHz TCR1 clock). The functions generate signals corresponding to Reference Voltage Vector Amplitude of 0 (50% duty-cycle) until the first reloaded values are processed.

The CPU controls the PWM output by setting the TPU parameters. The Stator Reference Voltage Vector components  $u_a$  and  $u_b$  have to be adjusted during run time. The PWM period  $T$  and the  $prescaler$  – the number of PWM periods per reload of new values – are also read at each reload, so these parameters can be changed during run time. The CPU notifies the TPU that the new reload

values are prepared by setting the LD\_OK parameter. The TPU notifies the CPU that the reload values have been read and new values can be written by clearing the LD\_OK parameter.

The TPU writes the parameter Sector that indicates the current Stator Reference Voltage Vector position in sector 1 to 6.

The following figures show the input Stator Reference Voltage Vector components  $u_{\hat{a}}$  and  $u_{\hat{\beta}}$ , corresponding sectors and output PWM signal duty cycle ratios:



**Figure 2. Standard Space Vector Modulation Technique**

The following equations describe how the Space Vector Modulation PWM signal high-times  $ht_A$ ,  $ht_B$ ,  $ht_C$  and transition times  $t_{trans}$  of each channel are calculated:

$$U_{\beta} = T \cdot u_{\beta}$$

$$U_{\alpha} = T \cdot u_{\alpha}$$





$$X = U_{\beta}$$

$$Y = \frac{U_{\beta} + U_{\alpha}\sqrt{3}}{2}$$







$$Z = \frac{U_{\beta} - U_{\alpha}\sqrt{3}}{2}$$

	Y < 0		Y >= 0			
	Z < 0	Z >= 0	Z < 0	X <= 0	X > 0	
<b>Sector:</b>	<b>V.</b>	<b>IV.</b>	<b>III.</b>	<b>VI.</b>	<b>I.</b>	<b>II.</b>

Host Interface

 Written By CPU	 Written by both CPU and TPU
 Written By TPU	 Not Used

**Table 4. svmStd3Xor\_T Control Bits**

Name		Options
3 2 1 0 	Channel Function Select	svmStd3Xor_T function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 	Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
1 0 	Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Not used 11 – Not used
1 0 	Host Sequence Bits (HSQ)	xx – Not used
0 	Channel Interrupt Enable	x – Not used
0 	Channel Interrupt Status	x – Not used

**Table 5. svmStd3Xor\_R Control Bits**




Name		Options
3 2 1 0 	Channel Function Select	svmStd3Xor_R function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 	Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
1 0 	Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Stop

Table 5. svmStd3Xor\_R Control Bits

Name	Options
<div style="display: flex; justify-content: space-around; width: 40px;"> <span>1</span> <span>0</span> </div> Host Sequence Bits (HSQ)	xx – Not used
<div style="display: flex; justify-content: space-around; width: 40px;"> <span>0</span> </div> Channel Interrupt Enable	0 – Channel Interrupt Disabled 1 – Channel Interrupt Enabled
<div style="display: flex; justify-content: space-around; width: 40px;"> <span>0</span> </div> Channel Interrupt Status	0 – Interrupt Not Asserted 1 – Interrupt Asserted

TPU function svmStd3Xor\_R generates an interrupt when the current values of *Ualfa*, *Ubeta*, *T* and *prescaler* have been read by TPU and indicates to the CPU that it can write new variables. The CPU program can either wait for this interrupt to occur, or poll the *LD\_OK* bit to check it has cleared. The interrupt is generated at each reload by one of the R channels. The T channels do not generate any interrupts.

Table 6. svmStd3Xor\_T and svmStd3Xor\_R Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Phase A 1 channel	0	htA															
	1	x2_chan_A															
	2	x1a_chan_A															
	3	x1b_chan_A															
	4	Ualfa															
	5	Ubeta															
	6																
Phase A 2 channel	7	fault_pinstat															
	0	Ttime_A2															
	1	T_copy															
	2	prsc_copy															
	3	UA															
	4	LD_OK															
	5	Sector															
	6																
7																	

**Table 6. svmStd3Xor\_T and svmStd3Xor\_R Parameter RAM**

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Phase B 1 channel	0	htB																
	1	x2_chan_B																
	2	x1a_chan_B																
	3	x1b_chan_B																
	4	T																
	5	prescaler																
	6																	
	7																	
Phase B 2 channel	0	Ttime_B2																
	1	dec																
	2	UA3																
	3	UB																
	4	SQRT3																
	5	sync_presc_addr																
	6																	
	7																	
Phase C 1 channel	0	htC																
	1	x2_chan_C																
	2	x1a_chan_C																
	3	x1b_chan_C																
	4	CPU14																
	5																	
	6																	
	7																	
Phase C 2 channel	0	Ttime_C2																
	1	state																
	2	center_time																
	3																	
	4																	
	5																	
	6																	
	7																	

**Table 7. svmStd3Xor\_T and svmStd3Xor\_R parameter description**

Parameter	Format	Description
Parameters written by CPU		
Ualfa, Ubeta	16-bit fractional	Stator Reference Voltage Vector components
T	16-bit unsigned integer	PWM period in number of TCR1 TPU cycles
prescaler	16-bit unsigned integer	The number of PWM periods per reload of new values

Table 7. svmStd3Xor\_T and svmStd3Xor\_R parameter description

Parameter	Format	Description
CPU14	16-bit unsigned integer	Time of 14 IMB clocks in TCR1 clocks.
SQRT3	16-bit fractional	$\sqrt{3}/2 = 0.866 = \$6EDA$ constant
sync_presc_addr	8-bit unsigned integer	address of synchronization channel <i>prescaler</i> parameter: $\$X4$ , where X is synchronization channel number. \$0 if no synchronization channel is used.
Parameters written by both TPU and CPU		
LD_OK	1-bit	0 ... CPU can update variables 1 ... TPU can read variables CPU sets 1, TPU sets 0
Parameters written by TPU		
Sector	16-bit unsigned integer	The position of Stator Reference Voltage Vector in a sector. The Sector can be 1, 2, 3, 4, 5 or 6
fault_pinstate	0 or 1	If fault channel is used, state of fault pin: 0 ... low 1 ... high
Other parameters are just for TPU function inner use.		

Performance

Table 8. svmStd3Xor\_T State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
ST	2	1
SF	2	0

Table 9. svmStd3Xor\_R State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	92	25
STOP	82	4
SFR <sub>0</sub>	6	1
SFR	40	14
C5	16	4
SFC <sub>0</sub>	6	1
SFC	56	11

**NOTE:** Execution times do not include the time slot transition time ( $TST = 10$  or  $14$  IMB clocks)

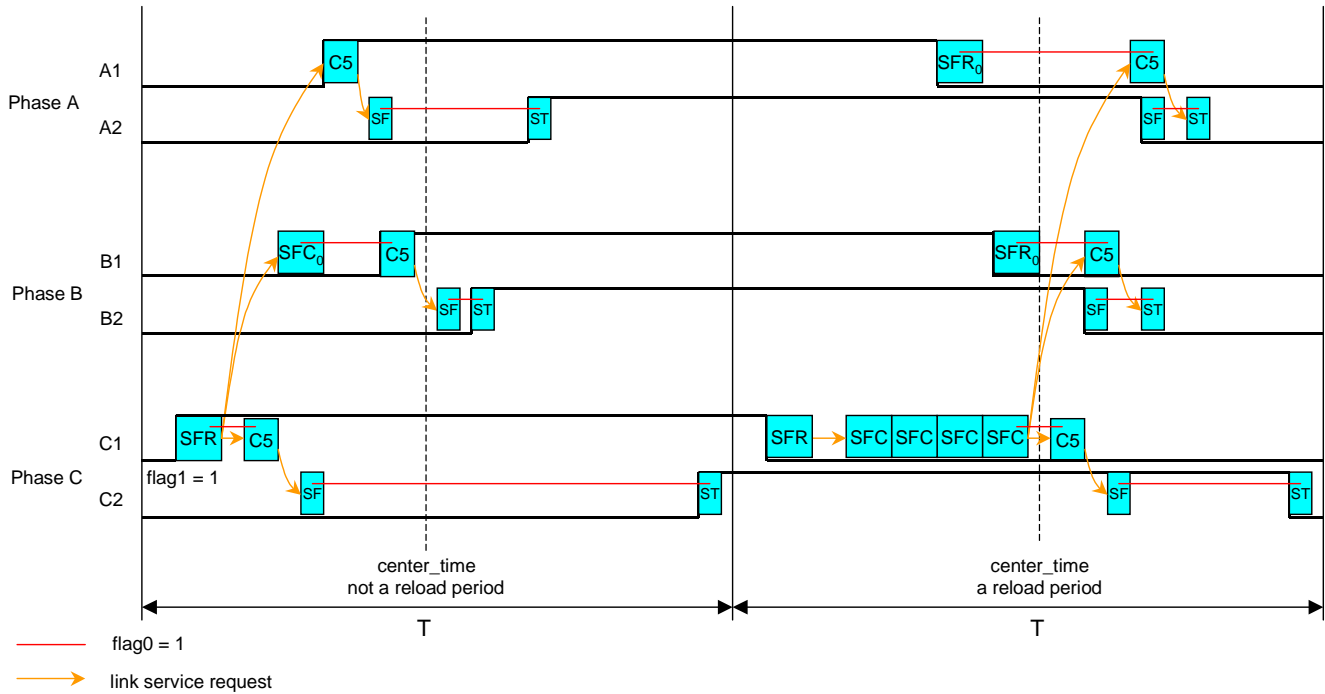


Figure 3. svmStd3Xor\_T and svmStd3Xor\_R timing

**NOTE:** The R channel with the momentary earliest transition within the PWM period is marked by a flag1 and runs the SFR and SFC states.

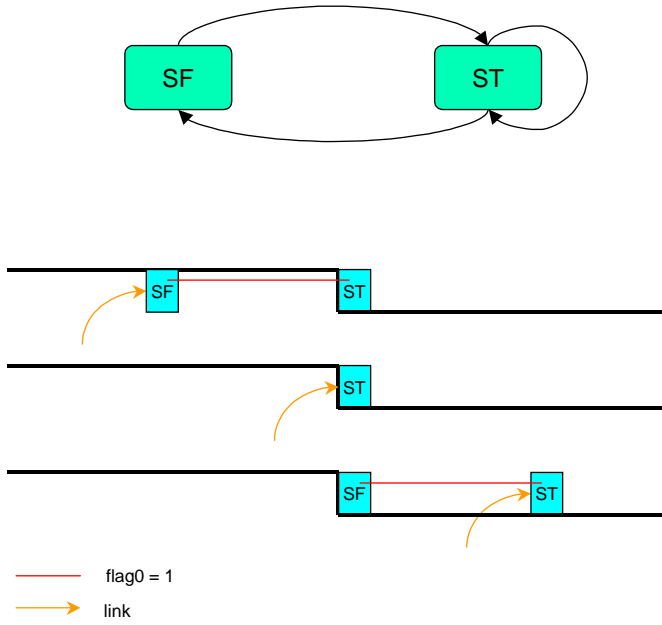


Figure 4. `svmStd3Xor_T` state diagram and 3 cases of timing

**NOTE:** Which case happens is determined by the time when the link comes.

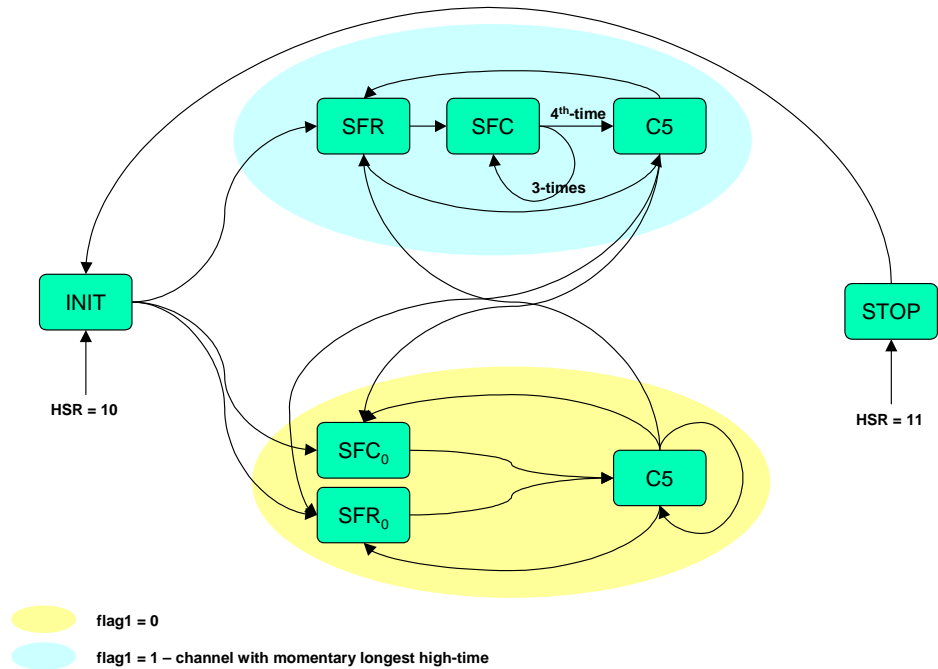


Figure 5. svmStd3Xor\_R state diagram

**Synchronization signal for Standard Space Vector Modulation – 3 outputs version – XOR version (svmStd3Xor\_sync)**

The svmStd3Xor\_sync TPU function uses information obtained from svmStd3Xor\_R and svmStd3Xor\_T functions, the actual PWM center times and the PWM periods. This allows a signal to be generated, which tracks the changes in the PWM period and is always synchronized with the PWM. The synchronization signal is a positive pulse generated repeatedly after the *prescaler* or *presc\_copy* PWM periods (see next paragraph). The low to high transition of the pulse can be adjusted by a parameter, either negative or positive, to go a number of TCR1 TPU cycles before or after the PWM period center time. The pulse width *pw* is another synchronization signal parameter.

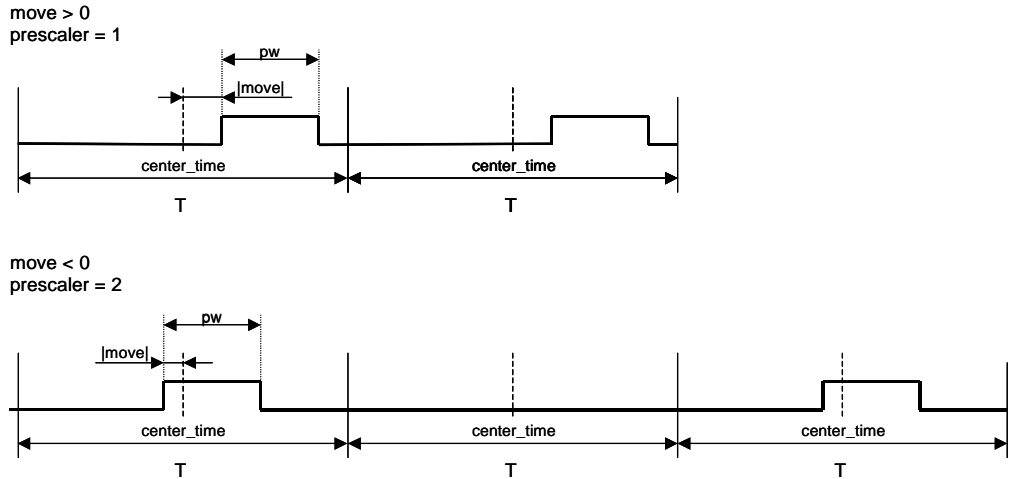


Figure 6. Synchronization signal adjustment examples

*Synchronized Change of PWM Prescaler And Synchronization Signal Prescaler*

The `svmStd3Xor_sync` TPU function actually uses the `presc_copy` parameter instead of the `prescaler` parameter. The `prescaler` parameter holds the prescaler value that is copied to the `presc_copy` by the `svmStd3Xor_bottom` function at the time the PWM parameters are reloaded. This ensures that new prescaler values for the PWM signals, as well as the synchronization signal, are applied at the same time. Write the synchronization signal `prescaler` parameter address to the `sync_presc_addr` parameter to enable this mechanism. Write 0 to disable it, and remember to set the synchronization signal `presc_copy` parameter instead of the `prescaler` parameter in this case.

*Host Interface*

- Written By CPU
- Written by both CPU and TPU
- Written By TPU
- Not Used

Table 10. `svmStd3Xor_sync` Control Bits

Name	Options
<div style="display: flex; justify-content: space-around; width: 100px;"> <span>3</span><span>2</span><span>1</span><span>0</span> </div> <div style="display: flex; align-items: center;"> <div style="border: 1px solid black; width: 20px; height: 20px; margin-right: 5px;"></div> <div style="border: 1px solid black; width: 20px; height: 20px; margin-right: 5px;"></div> <div style="border: 1px solid black; width: 20px; height: 20px; margin-right: 5px;"></div> <div style="border: 1px solid black; width: 20px; height: 20px;"></div> </div>	<code>svmStd3Xor_sync</code> function number (Assigned during assembly the DPTRAM code from library TPU functions)
Channel Function Select	
<div style="display: flex; justify-content: space-around; width: 40px;"> <span>1</span><span>0</span> </div> <div style="display: flex; align-items: center;"> <div style="border: 1px solid black; width: 20px; height: 20px; margin-right: 5px;"></div> <div style="border: 1px solid black; width: 20px; height: 20px;"></div> </div>	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
Channel Priority	

Table 10. svmStd3Xor\_sync Control Bits

Name	Options
<div style="display: flex; align-items: center;"> <div style="margin-right: 10px;"> <div style="display: flex; justify-content: space-around; width: 20px;"> <span>1</span><span>0</span> </div> <div style="border: 1px solid black; width: 15px; height: 15px; display: inline-block;"></div> </div> <div>Host Service Bits (HSR)</div> </div>	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Not used
<div style="display: flex; align-items: center;"> <div style="margin-right: 10px;"> <div style="display: flex; justify-content: space-around; width: 20px;"> <span>1</span><span>0</span> </div> <div style="background-color: green; width: 15px; height: 15px; display: inline-block;"></div> </div> <div>Host Sequence Bits (HSQ)</div> </div>	xx – Not used
<div style="display: flex; align-items: center;"> <div style="margin-right: 10px;"> <div style="display: flex; justify-content: space-around; width: 20px;"> <span>0</span> </div> <div style="border: 1px solid black; width: 15px; height: 15px; display: inline-block;"></div> </div> <div>Channel Interrupt Enable</div> </div>	0 – Channel Interrupt Disabled 1 – Channel Interrupt Enabled
<div style="display: flex; align-items: center;"> <div style="margin-right: 10px;"> <div style="display: flex; justify-content: space-around; width: 20px;"> <span>0</span> </div> <div style="background-color: blue; width: 15px; height: 15px; display: inline-block;"></div> </div> <div>Channel Interrupt Status</div> </div>	0 – Interrupt Not Asserted 1 – Interrupt Asserted

TPU function svmStd3Xor\_sync generates an interrupt after each low to high transition.

Table 11. svmStd3Xor\_sync Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Synchronization channel	0	move															
	1	pw															
	2	prescaler															
	3	presc_copy															
	4	time															
	5	dec															
	6	T_copy															
	7																

Table 12. svmStd3Xor\_sync parameter description

Parameter	Format	Description
Parameters written by CPU		
move	16-bit signed integer	The number of TCR1 TPU cycles to forego (negative) or come after (positive) the PWM period center time
pw	16-bit unsigned integer	Synchronization pulse width in number of TCR1 TPU cycles.

Table 12. svmStd3Xor\_sync parameter description

Parameter	Format	Description
prescaler	16-bit unsigned integer	The number of PWM periods per synchronization pulse – use in case of synchronized prescalers change
presc_copy	16-bit unsigned integer	The number of PWM periods per synchronization pulse – use in case of asynchronized prescalers change
Parameters written by TPU		
Other parameters are just for TPU function inner use.		

Performance

There is one limitation. The absolute value of parameter *move* has to be less than a quarter of the PWM period *T*.

$$|move| < \frac{T}{4}$$

Table 13. svmStd3Xor\_sync State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	12	5
S1	12	6
S2	8	3
S3	16	7

**NOTE:** Execution times do not include the time slot transition time ( $TST = 10$  or  $14$  IMB clocks)

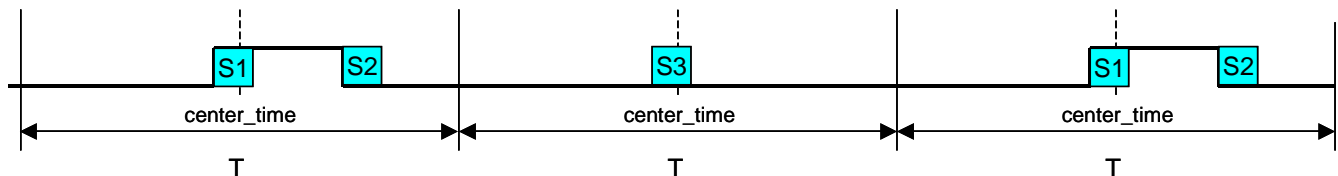


Figure 7. svmStd3Xor\_sync timing

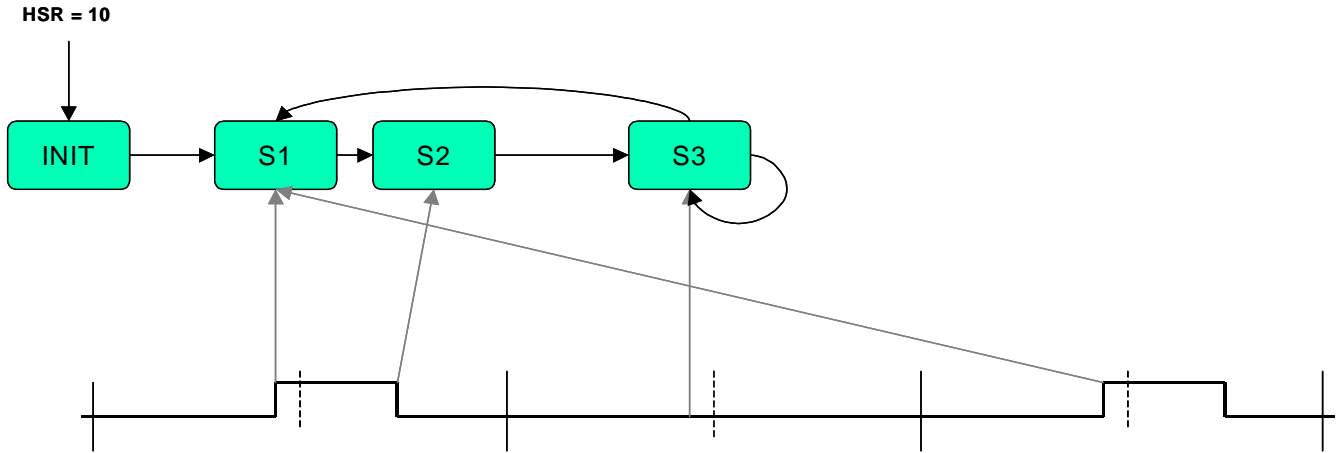
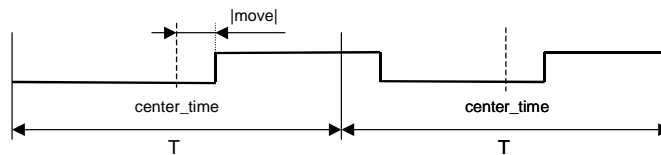


Figure 8. svmStd3Xor\_sync state diagram

**Resolver Reference Signal for Standard Space Vector Modulation – 3 outputs version – XOR version (svmStd3Xor\_res)**

The svmStd3Xor\_res TPU function uses information read from the svmStd3Xor\_R and svmStd3Xor\_T functions, the actual PWM center times and the PWM periods. This allows a signal to be generated, which tracks the changes of the PWM period and is always synchronized with the PWM. The resolver reference signal is a 50% duty-cycle signal with a period equal to *prescaler* or synchronization channel *presc\_copy* PWM periods (see next paragraph). The low to high transition of the pulse can be adjusted by a parameter, either negative or positive, to go a number of TCR1 TPU cycles before or after the PWM period center time.

move > 0  
prescaler = 1



move < 0  
prescaler = 2

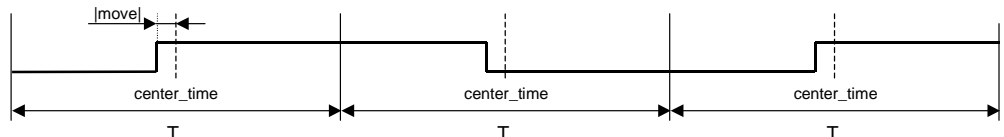






Figure 9. Resolver reference signal adjustment examples

*Synchronized Change of PWM Prescaler And Resolver Reference Signals Prescaler*

The svmStd3Xor\_res TPU function can inherit the Synchronization Signal prescaler that is synchronously changed with the PWM prescaler. Write the synchronization signals *presc\_copy* parameter address to the *presc\_addr* parameter to enable this mechanism. Write 0 to disable it, and in this case set the *prescaler* parameter to directly specify prescaler value.

*Host Interface*

 Written By CPU	 Written by both CPU and TPU
 Written By TPU	 Not Used

**Table 14. svmStd3Xor\_res Control Bits**







Name	Options
<div style="display: flex; justify-content: space-around; width: 100px;"> <span>3</span><span>2</span><span>1</span><span>0</span> </div>  Channel Function Select	svmStd3Xor_res function number (Assigned during assembly the DPTRAM code from library TPU functions)
<div style="display: flex; justify-content: space-around; width: 40px;"> <span>1</span><span>0</span> </div>  Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
<div style="display: flex; justify-content: space-around; width: 40px;"> <span>1</span><span>0</span> </div>  Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Not used
<div style="display: flex; justify-content: space-around; width: 40px;"> <span>1</span><span>0</span> </div>  Host Sequence Bits (HSQ)	xx – Not used
<div style="display: flex; justify-content: space-around; width: 40px;"> <span>0</span> </div>  Channel Interrupt Enable	x – Not used
<div style="display: flex; justify-content: space-around; width: 40px;"> <span>0</span> </div>  Channel Interrupt Status	x – Not used

Table 15. svmStd3Xor\_res Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Resolver	0	move															
	1																
	2	presc_addr															
	3	prescaler															
	4	time															
	5	dec															
	6	T_copy															
	7																

Table 16. svmStd3Xor\_res parameter description

Parameter	Format	Description
Parameters written by CPU		
move	16-bit signed integer	The number of TCR1 TPU cycles to forego (negative) or come after (positive) the PWM period center time
presc_addr	16-bit unsigned integer	\$00X6, where X is a number of Synchronization Signal channel, to inherit Sync. channel prescaler or \$0000 to enable direct specification of prescaler value in prescaler parameter
prescaler	1, 2, 4, 6, 8, 10, 12, 14, ...	The number of PWM periods per synchronization pulse – use when apresc_addr = 0
Parameters written by TPU		
Other parameters are just for TPU function inner use.		

Performance

There is one limitation. The absolute value of parameter *move* has to be less than a quarter of the PWM period *T*.

$$|move| < \frac{T}{4}$$

Table 17. svmStd3Xor\_res State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	12	5
S1	26	9
S3	18	7

**NOTE:** Execution times do not include the time slot transition time ( $TST = 10$  or  $14$  IMB clocks)

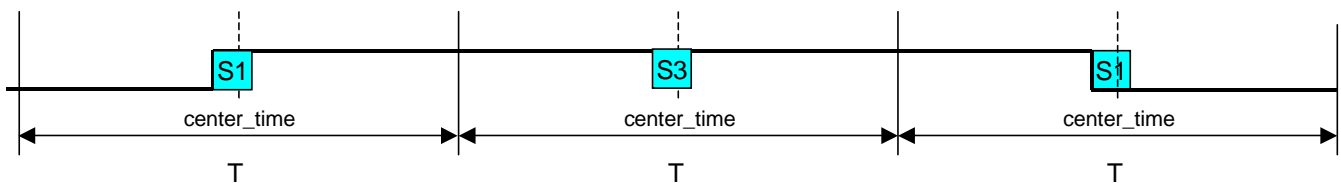


Figure 10. svmStd3Xor\_res timing

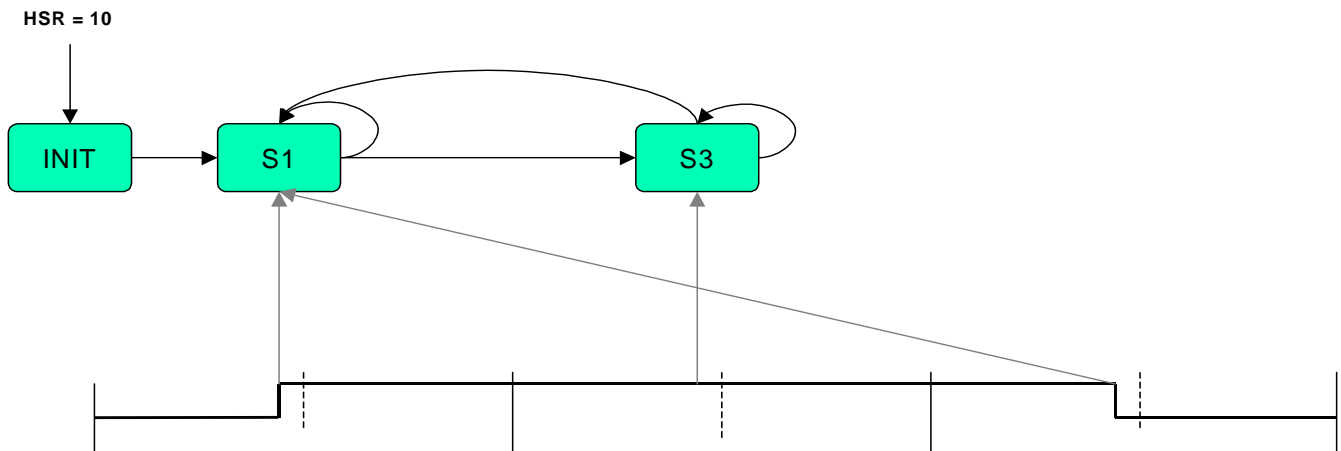


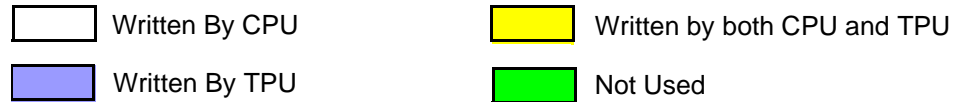
Figure 11. svmStd3Xor\_res state diagram

**Fault Input for Standard Space Vector Modulation – 3 outputs version – XOR version (svmStd3Xor\_fault)**

The svmStd3Xor\_fault is an input TPU function that monitors the pin, and if a high to low transition occurs, immediately sets all PWM channels low and cancels all further transitions on them. The PWM channels, as well as the synchronization and resolver reference signal channels (if used), have to be initialized again to start them running.

The function returns the actual pinstate as a value of 0 (low) or 1 (high) in the parameter *fault\_pinstate*. The parameter is placed on the A1 channel to keep the fault channel parameter space free.

*Host Interface*



**Table 18. svmStd3Xor\_fault Control Bits**

Name	Options
<div style="display: flex; justify-content: space-around; font-size: small;"> <span>3</span><span>2</span><span>1</span><span>0</span> </div> <div style="display: flex; align-items: center;"> <div style="display: flex; gap: 5px;"> <div style="width: 15px; height: 15px; border: 1px solid black;"></div> <div style="width: 15px; height: 15px; border: 1px solid black;"></div> <div style="width: 15px; height: 15px; border: 1px solid black;"></div> <div style="width: 15px; height: 15px; border: 1px solid black;"></div> </div> <div style="margin-left: 10px;">Channel Function Select</div> </div>	svmStd3Xor_fault function number (Assigned during assembly the DPTRAM code from library TPU functions)
<div style="display: flex; justify-content: space-around; font-size: small;"> <span>1</span><span>0</span> </div> <div style="display: flex; align-items: center;"> <div style="display: flex; gap: 5px;"> <div style="width: 15px; height: 15px; border: 1px solid black;"></div> <div style="width: 15px; height: 15px; border: 1px solid black;"></div> </div> <div style="margin-left: 10px;">Channel Priority</div> </div>	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
<div style="display: flex; justify-content: space-around; font-size: small;"> <span>1</span><span>0</span> </div> <div style="display: flex; align-items: center;"> <div style="display: flex; gap: 5px;"> <div style="width: 15px; height: 15px; border: 1px solid black;"></div> <div style="width: 15px; height: 15px; border: 1px solid black;"></div> </div> <div style="margin-left: 10px;">Host Service Bits (HSR)</div> </div>	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Not used
<div style="display: flex; justify-content: space-around; font-size: small;"> <span>1</span><span>0</span> </div> <div style="display: flex; align-items: center;"> <div style="display: flex; gap: 5px;"> <div style="width: 15px; height: 15px; border: 1px solid black; background-color: lime;"></div> <div style="width: 15px; height: 15px; border: 1px solid black; background-color: lime;"></div> </div> <div style="margin-left: 10px;">Host Sequence Bits (HSQ)</div> </div>	xx – Not used
<div style="display: flex; justify-content: space-around; font-size: small;"> <span>0</span> </div> <div style="display: flex; align-items: center;"> <div style="width: 15px; height: 15px; border: 1px solid black;"></div> <div style="margin-left: 10px;">Channel Interrupt Enable</div> </div>	0 – Channel Interrupt Disabled 1 – Channel Interrupt Enabled
<div style="display: flex; justify-content: space-around; font-size: small;"> <span>0</span> </div> <div style="display: flex; align-items: center;"> <div style="width: 15px; height: 15px; border: 1px solid black; background-color: lightblue;"></div> <div style="margin-left: 10px;">Channel Interrupt Status</div> </div>	0 – Interrupt Not Asserted 1 – Interrupt Asserted

TPU function svmStd3Xor\_fault generates an interrupt when a high to low transition appears.

Table 19. svmStd3Xor\_fault Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fault input	0	[Redacted]															
	1	[Redacted]															
	2	[Redacted]															
	3	[Redacted]															
	4	[Redacted]															
	5	[Redacted]															
	6	[Redacted]															
	7	[Redacted]															

Table 20. svmStd3Xor\_fault parameter description

Parameter	Format	Description
Parameters written by TPU		
fault_pinstate	0 or 1	State of fault pin: 0 ... low 1 ... high

Performance

Table 21. svmStd3Xor\_fault State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	8	2
FAULT	88	5
NO_FAULT	4	1

**NOTE:** Execution times do not include the time slot transition time (TST = 10 or 14 IMB clocks)

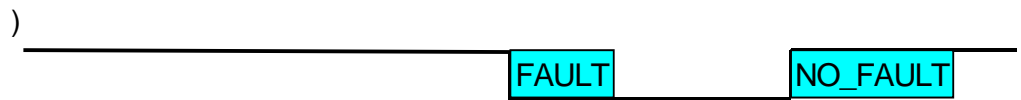


Figure 12. svmStd3Xor\_fault timing.

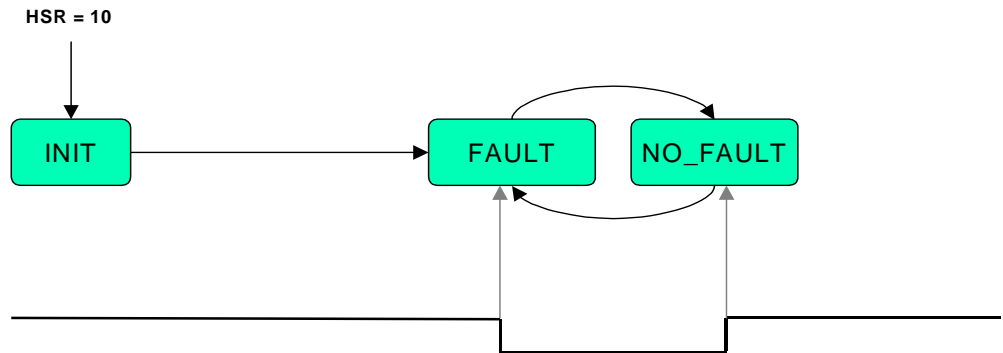


Figure 13. svmStd3Xor\_fault state diagram

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