

Silicon Controlled Rectifier

Reverse Blocking Triode Thyristor

... designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Economical for a Wide Range of Uses
- High Surge Current — $I_{TSM} = 300$ Amps
- Low Forward "On" Voltage — 1.2 V (Typ) @ $I_{TM} = 25$ Amps
- Practical Level Triggering and Holding Characteristics — 10 mA (Typ) @ $T_C = 25^\circ\text{C}$
- Rugged Construction in Either Pressfit, Stud, or Isolated Stud
- Glass Passivated Junctions for Maximum Reliability

MAXIMUM RATINGS

Rating	Suffix	Symbol	Value	Unit
Peak Repetitive Off-State Voltage, Note 1 ($T_C = -40$ to $+100^\circ\text{C}$) All Types	F	V_{DRM}	50	Volts
	A	and	100	
	B	V_{RRM}	200	
	D		400	
	M		600	
Non-Repetitive Reverse Voltage ($T_C = -40$ to 100°C) All Types	F	V_{RSM}	75	Volts
	A		150	
	B		300	
	D		500	
	M		720	
Forward Current RMS		$I_T(\text{RMS})$	25	Amps
Peak Surge Current (One Cycle, 60 Hz, $T_C = -40$ to 100°C)		I_{TSM}	250	Amps
Circuit Fusing ($T_C = -40$ to 100°C , $t = 1$ to 8.3 ms)		I^2t	260	A^2s
Peak Gate Power		P_{GM}	5	Watts
Average Gate Power		$P_{G(AV)}$	0.5	Watt
Peak Forward Gate Current		I_{GM}	2	Amps
Operating Junction Temperature Range		T_J	-40 to $+100$	$^\circ\text{C}$
Storage Temperature Range		T_{stg}	-40 to $+125$	$^\circ\text{C}$
Stud Torque		—	30	in. lb.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Pressfit and Stud Isolated Stud	$R_{\theta JC}$	1	$^\circ\text{C/W}$
		1.15	

Note 1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices shall not have a positive bias applied to the gate concurrently with a negative potential on the anode.

C230, 231
C230()3,
231()3
C232, 233
Series

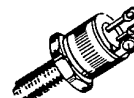
SCRs
25 AMPERES RMS
50 thru 600 VOLTS



CASE 174-04
(TO-203)
STYLE 1
C232 and C233 Series



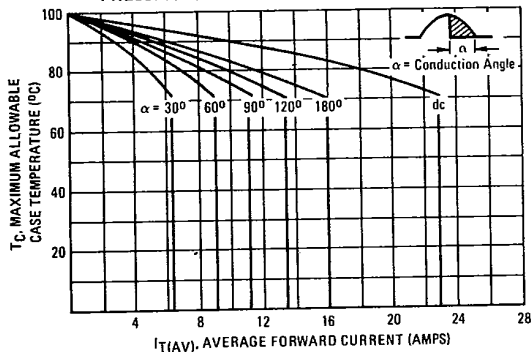
CASE 175-03
STYLE 1
C230 and 231 Series



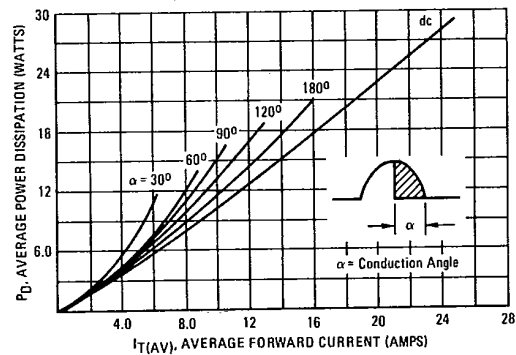
CASE 235-03
STYLE 1
C230()3 and C231()3 Series

C230, 231 • C230()3, 231()3 • C232, 233 Series**ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM} , gate open) $T_C = 25^\circ\text{C}$ $T_C = 100^\circ\text{C}$	I_{DRM} , I_{RRM}	—	—	10 1	μA mA
Forward "On" Voltage ($I_{TM} = 100$ A Peak, Pulse Width ≤ 1 ms, Duty Cycle $\leq 2\%$)	V_{TM}	—	—	1.9	Volts
Gate Trigger Current, C230, C230()3, C232 series ($V_D = 12$ Vdc, $R_L = 120$ Ohms) ($V_D = 12$ Vdc, $R_L = 60$ Ohms) $T_C = -40^\circ\text{C}$	I_{GT}	—	—	25 40	mA
Gate Trigger Current, C231, C231()3, C233 (Continuous dc) ($V_D = 12$ Vdc, $R_L = 120$ Ohms) ($V_D = 12$ Vdc, $R_L = 60$ Ohms) $T_C = -40^\circ\text{C}$	I_{GT}	—	—	9 20	mA
Gate Trigger Voltage (Continuous dc) ($V_D = 12$ Vdc, $R_L = 120$ Ohms) ($V_D = 12$ Vdc, $R_L = 60$ Ohms) $T_C = -40^\circ\text{C}$ ($V_D = \text{Rated } V_{DRM}$, $R_L = 1000$ Ohms) $T_C = +100^\circ\text{C}$	V_{GT}	— 0.2	—	1.5 2	Volts
Holding Current ($V_D = 24$ V, gate open, $I_T = 0.5$ A) $T_C = -40^\circ\text{C}$	I_H	—	—	50 100	mA
Turn-On Time ($t_d + t_r$) ($I_{TM} = 25$ Adc, $I_{GT} = 40$ mAdc, $V_D = \text{Rated } V_{DRM}$)	t_{gt}	—	1	—	μs
Turn-Off Time ($I_{TM} = 10$ A, $I_R = 10$ A, Pulse Width = $50 \mu\text{s}$, $dv/dt = 20$ V/ μs , $V_D = \text{Rated } V_{DRM}$) $T_C = 100^\circ\text{C}$	t_q	—	25 35	—	μs
Forward Voltage Application Rate ($V_D = \text{Rated } V_{DRM}$) $T_C = 100^\circ\text{C}$	dv/dt	—	100	—	V/ μs

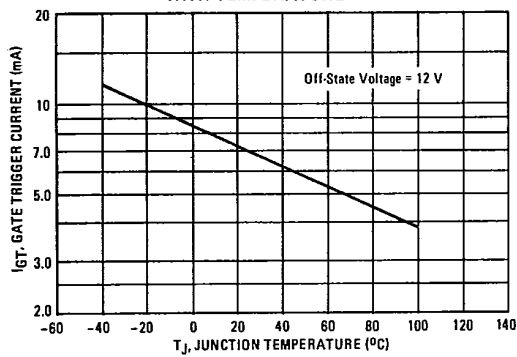
3**FIGURE 1 — CURRENT DERATING FOR PRESSFIT AND NON-ISOLATED STUD**

NOTE: Derating is for Pressfit and Stud Devices. Isolated stud devices must be derated an additional 15%. For example, the max T_C @ 16 A (180° conduction angle) is 70°C, a derating of 30°C. Isolated stud devices must be derated 34.5°C; therefore, the maximum T_C is 65.5°C.

FIGURE 2 — ON-STATE POWER DISSIPATION versus ON-STATE CURRENT

C230, 231 • C230()3, 231()3 • C232, 233 Series

**FIGURE 3 – GATE CURRENT VARIATION
WITH TEMPERATURE**



**FIGURE 4 – GATE VOLTAGE VARIATION
WITH TEMPERATURE**

