

TRIACS

Silicon Bidirectional Thyristors

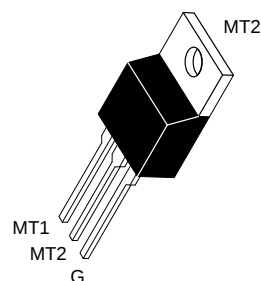
Designed for high performance full-wave ac control applications where high noise immunity and high commutating di/dt are required.

- Blocking Voltage to 800 Volts
- On-State Current Rating of 8.0 Amperes RMS at 100°C
- Uniform Gate Trigger Currents in Three Modes
- High Immunity to dv/dt — 500 V/μs minimum at 125°C
- Minimizes Snubber Networks for Protection
- Industry Standard TO-220AB Package
- High Commutating di/dt — 6.5 A/ms minimum at 125°C

MAC9 SERIES*

*Motorola preferred devices

TRIACS
8.0 AMPERES RMS
400 thru 800
VOLTS



CASE 221A-06
(TO-220AB)
Style 4

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DRM}	Peak Repetitive Off-State Voltage (1) (-40 to 125°C , Sine Wave, 50 to 60 Hz, Gate Open)	MAC9D MAC9M MAC9N 400 600 800	Volts
$I_{\text{T(RMS)}}$	On-State RMS Current (60 Hz, $T_C = 100^\circ\text{C}$)	8.0	A
I_{TSM}	Peak Non-repetitive Surge Current (One Full Cycle, 60 Hz, $T_J = 125^\circ\text{C}$)	80	A
I^2t	Circuit Fusing Consideration ($t = 8.3$ ms)	26	A ² sec
P_{GM}	Peak Gate Power (Pulse Width ≤ 1.0 μs, $T_C = 80^\circ\text{C}$)	16	Watts
$P_{\text{G(AV)}}$	Average Gate Power ($t = 8.3$ ms, $T_C = 80^\circ\text{C}$)	0.35	Watts
T_J	Operating Junction Temperature Range	-40 to $+125$	$^\circ\text{C}$
T_{stg}	Storage Temperature Range	-40 to $+150$	$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta\text{JC}}$ $R_{\theta\text{JA}}$	Thermal Resistance — Junction to Case — Junction to Ambient	2.2 62.5	$^\circ\text{C/W}$
T_L	Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	260	$^\circ\text{C}$

(1) V_{DRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

Preferred devices are Motorola recommended choices for future use and best overall value.

MAC9 SERIES

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
I_{DRM}	Peak Repetitive Blocking Current ($V_D = \text{Rated } V_{\text{DRM}}$, Gate Open)	—	—	0.01	mA
	$T_J = 25^\circ\text{C}$	—	—	2.0	
	$T_J = 125^\circ\text{C}$	—	—		

ON CHARACTERISTICS

V_{TM}	Peak On-State Voltage* ($I_{\text{TM}} = \pm 11 \text{ A Peak}$)	—	1.2	1.6	Volts
I_{GT}	Continuous Gate Trigger Current ($V_D = 12 \text{ V}$, $R_L = 100 \Omega$) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–)	10 10 10	16 18 22	50 50 50	mA
I_{H}	Hold Current ($V_D = 12 \text{ V}$, Gate Open, Initiating Current = $\pm 150 \text{ mA}$)	—	30	50	mA
I_{L}	Latch Current ($V_D = 24 \text{ V}$, $I_{\text{G}} = 50 \text{ mA}$) MT2(+), G(+); MT2(–), G(–) MT2(+), G(–)	— —	20 30	50 80	mA
V_{GT}	Gate Trigger Voltage ($V_D = 12 \text{ V}$, $R_L = 100 \Omega$) MT2(+), G(+) MT2(+), G(–) MT2(–), G(–)	0.5 0.5 0.5	0.69 0.77 0.72	1.5 1.5 1.5	Volts

DYNAMIC CHARACTERISTICS

$(di/dt)_C$	Rate of Change of Commutating Current* See Figure 10. ($V_D = 400 \text{ V}$, $I_{\text{TM}} = 4.4 \text{ A}$, Commutating $dv/dt = 18 \text{ V}/\mu\text{s}$, Gate Open, $T_J = 125^\circ\text{C}$, $f = 250 \text{ Hz}$, No Snubber)	6.5	—	—	A/ms
dv/dt	Critical Rate of Rise of Off-State Voltage ($V_D = \text{Rated } V_{\text{DRM}}$, Exponential Waveform, Gate Open, $T_J = 125^\circ\text{C}$)	500	—	—	V/ μs

*Indicates Pulse Test: Pulse Width $\leq 2.0 \text{ ms}$, Duty Cycle $\leq 2\%$.

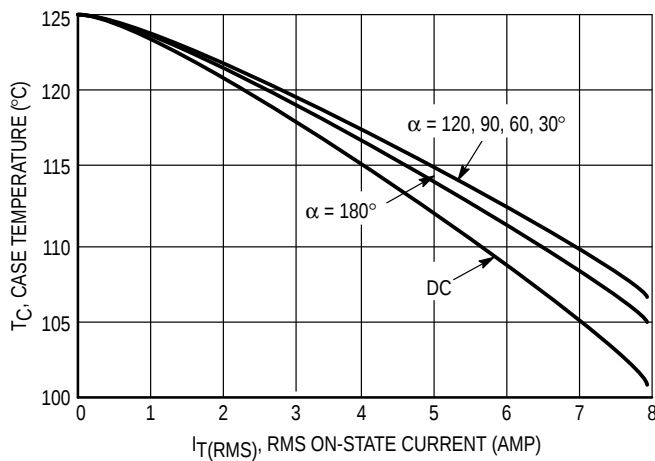


Figure 1. RMS Current Derating

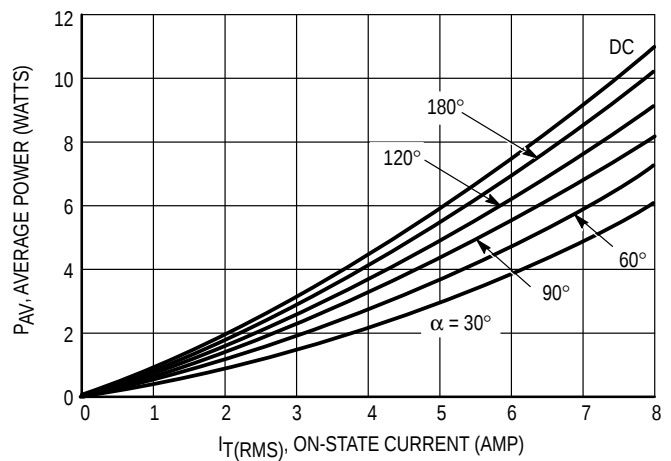


Figure 2. On-State Power Dissipation

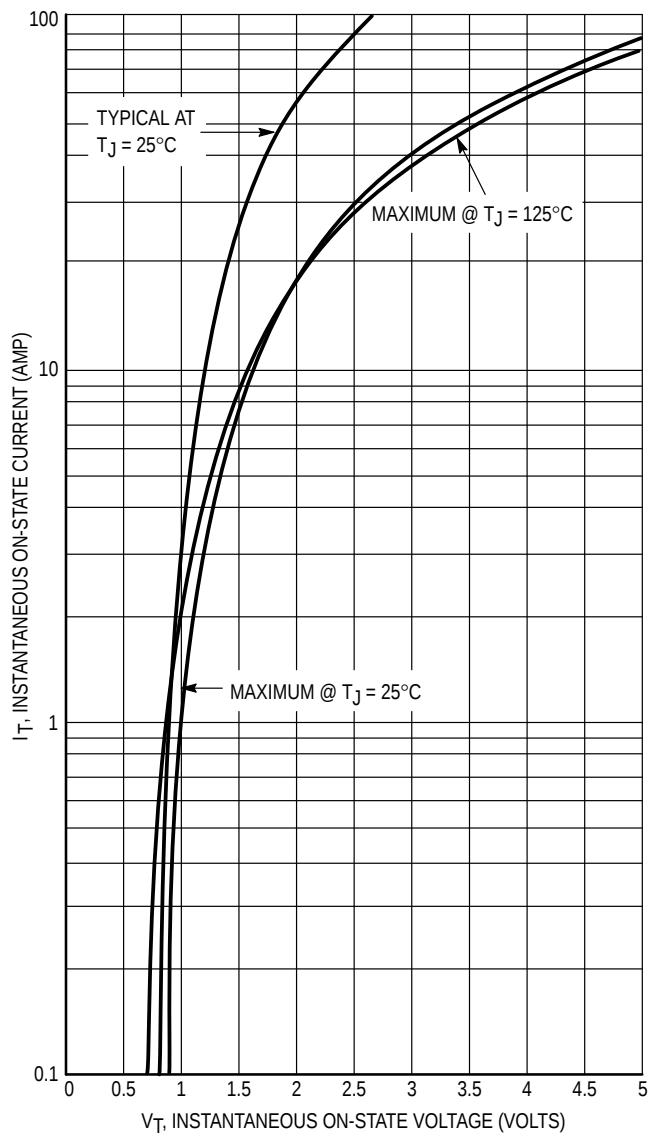


Figure 3. On-State Characteristics

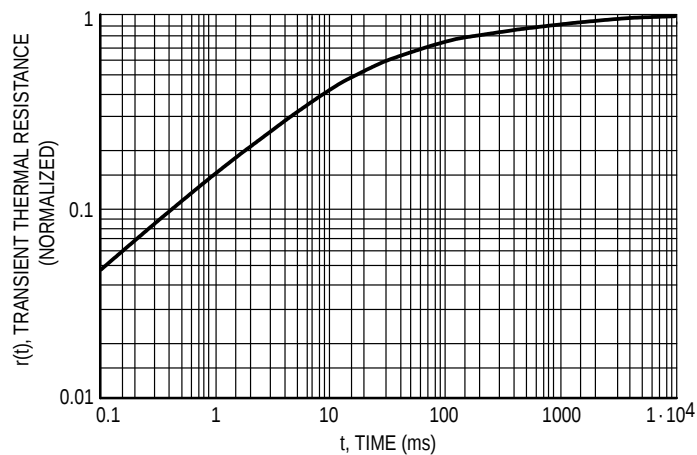


Figure 4. Thermal Response

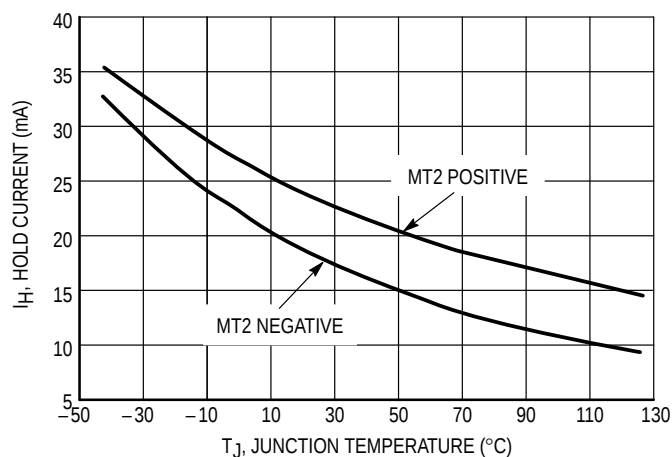


Figure 5. Hold Current Variation

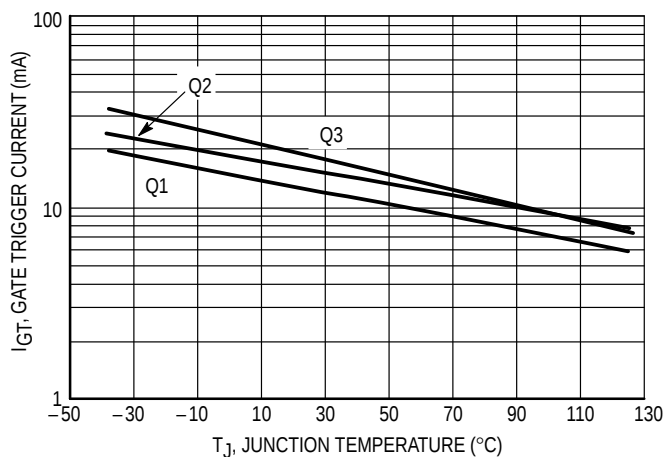


Figure 6. Gate Trigger Current Variation

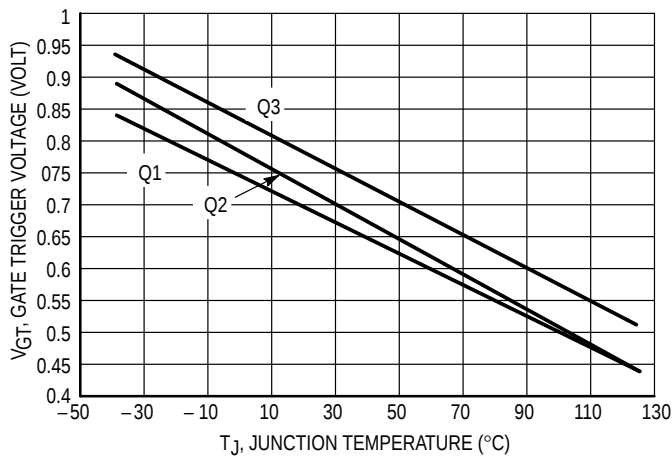


Figure 7. Gate Trigger Voltage Variation

MAC9 SERIES

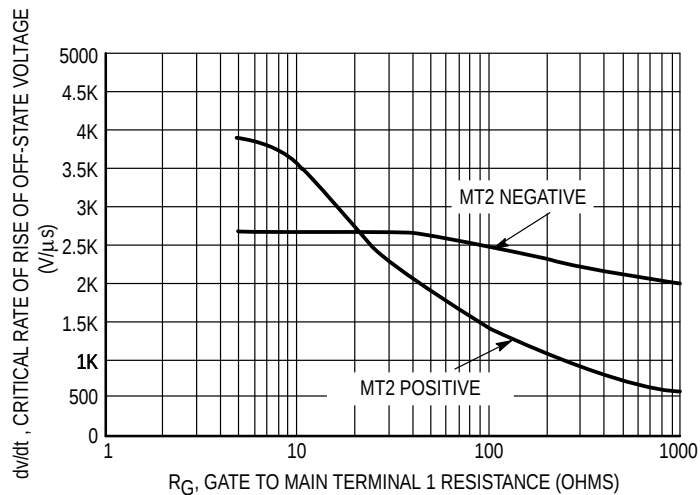


Figure 8. Critical Rate of Rise of Off-State Voltage (Exponential)

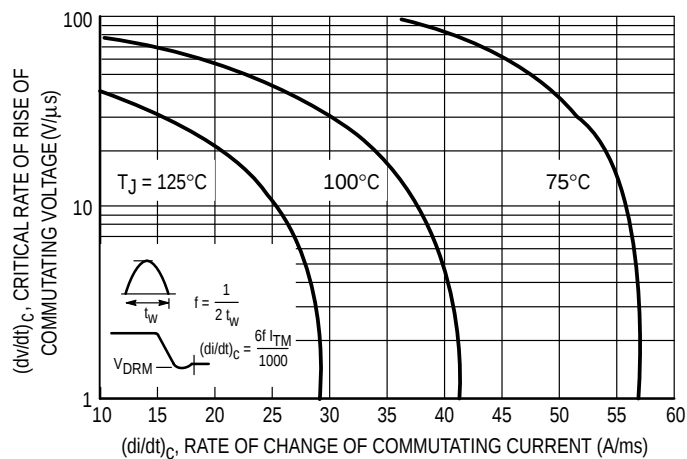
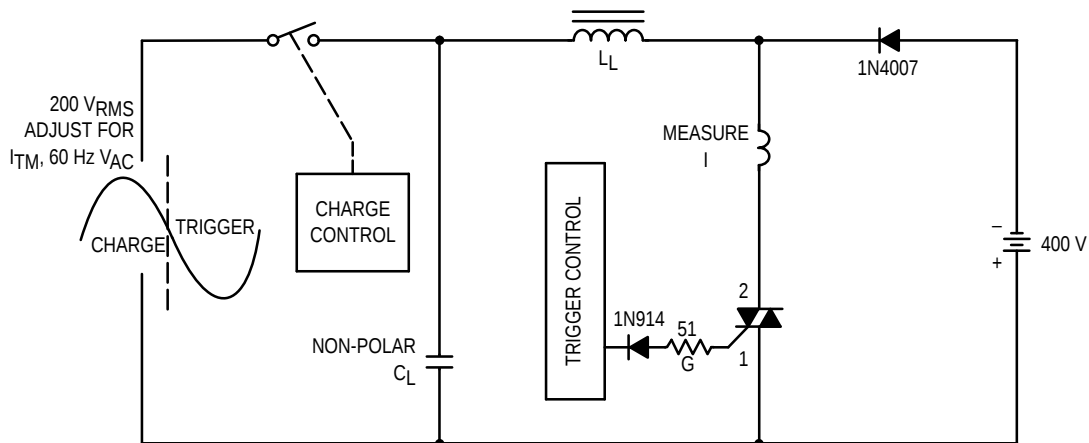


Figure 9. Critical Rate of Rise of Commutating Voltage



Note: Component values are for verification of rated $(dv/dt)_C$. See AN1048 for additional information.

Figure 10. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Voltage