

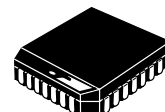
3-Bit Scannable Registered Bus Transceiver

The MC10E/100E337 is a 3-bit registered bus transceiver with scan. The bus outputs (BUS0–BUS2) are specified for driving a 25Ω bus; the receive outputs (Q0 – Q2) are specified for 50Ω. The bus outputs feature a normal HIGH level (V_{OH}) and a cutoff LOW level — when LOW, the outputs go to – 2.0V and the output emitter-follower is “off”, presenting a high impedance to the bus. The bus outputs also feature edge slow-down capacitors.

- Scannable Version of E336
- 25Ω Cutoff Bus Outputs
- 50Ω Receiver Outputs
- Scannable Registers
- Sync. and Async. Bus Enables
- Non-inverting Data Path
- 1500ps Max. Clock to Bus (Data Transmit)
- 1000ps Max. Clock to Q (Data Receive)
- Bus Outputs Feature Internal Edge Slow-Down Capacitors
- Additional Package Ground Pins
- Extended 100E V_{EE} Range of – 4.2V to – 5.46V
- 75kΩ Input Pulldown Resistors

MC10E337
MC100E337

**3-BIT SCANNABLE
REGISTERED
BUS TRANSCEIVER**



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

Both drive and receive sides feature the same logic, including a loopback path to hold data. The HOLD/LOAD function is controlled by Transmit Enable (TEN) and Receive Enable (REN) on the transmit and receive sides respectively, with a HIGH selecting LOAD. Note that the implementation of the E337 Receive Enable differs from that of the E336.

A synchronous bus enable (SBUSEN) is provided for normal, non-scan operation. The asynchronous bus disable (ABUSDIS) disables the bus immediately for scan mode.

The SYNCEN input is provided for flexibility when re-enabling the bus after disabling with ABUSDIS, allowing either synchronous or asynchronous re-enabling. An alternative use is asynchronous-only operation with ABUSDIS, in which case SYNCEN is tied LOW, or left open. SYNCEN is implemented as an overriding SET control (active-LOW) to the enable flip-flop.

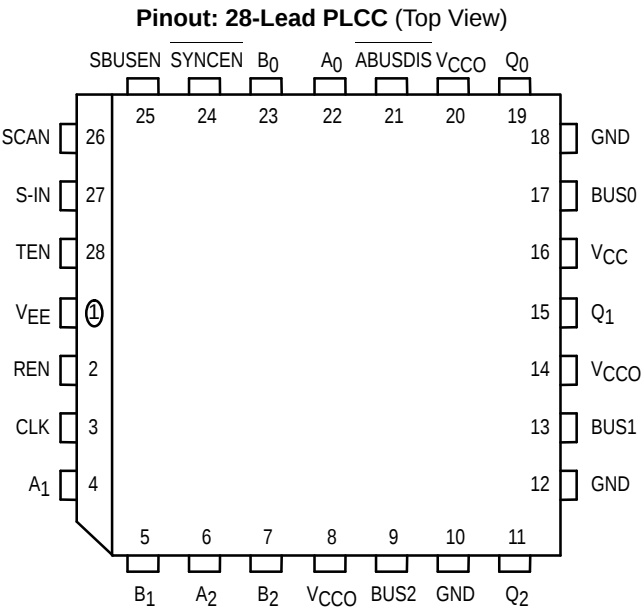
Scan mode is selected by a HIGH at the SCAN input. Scan input data is shifted in through S_IN and output data appears at the Q2 output.

All registers are clocked on the positive transition of CLK. Additional lead-frame grounding is provided through the Ground pins (GND) which should be connected to 0V. The GND pins are not electrically connected to the chip.

PIN NAMES

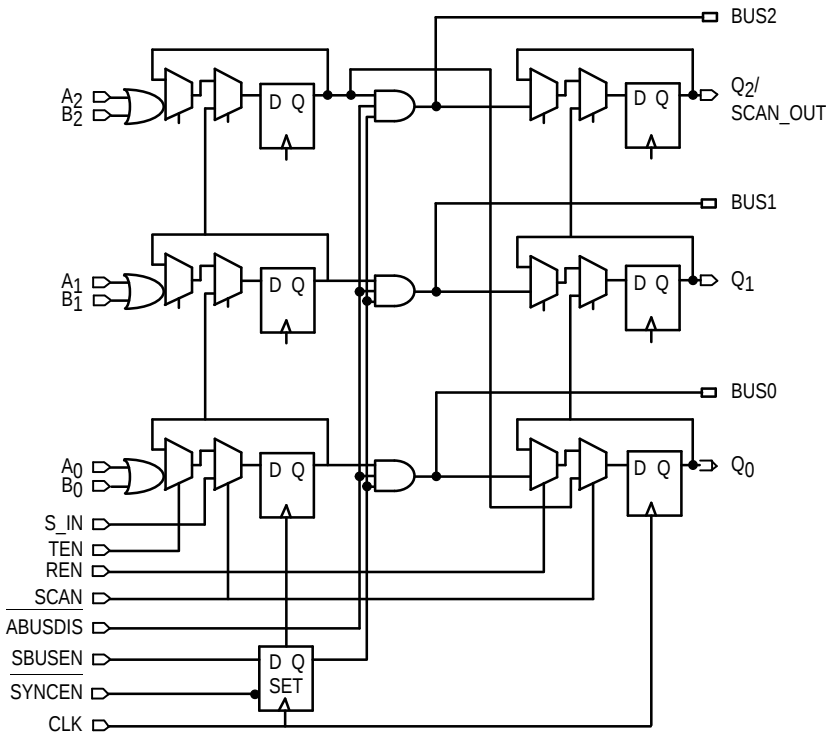
Pin	Function
A ₀ – A ₂	Data Inputs A
B ₀ – B ₂	Data Inputs B
S-IN	Serial (Scan) Data Input
TEN, REN	HOLD/LOAD Controls
SCAN	Scan Control
ABUSDIS	Asynchronous Bus Disable
SBUSEN	Synchronous Bus Enable
SYNCEN	Synchronous Enable Control
CLK	Clock
BUS0 – BUS2	25Ω Cutoff Bus Outputs
Q ₀ – Q ₂	Receive Data Outputs (Q2 serves as SCAN_OUT in scan mode)





* All VCC and VCCO pins are tied together on the die.

LOGIC DIAGRAM



DC CHARACTERISTICS ($V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$; $V_{CC} = V_{CCO} = \text{GND}$)

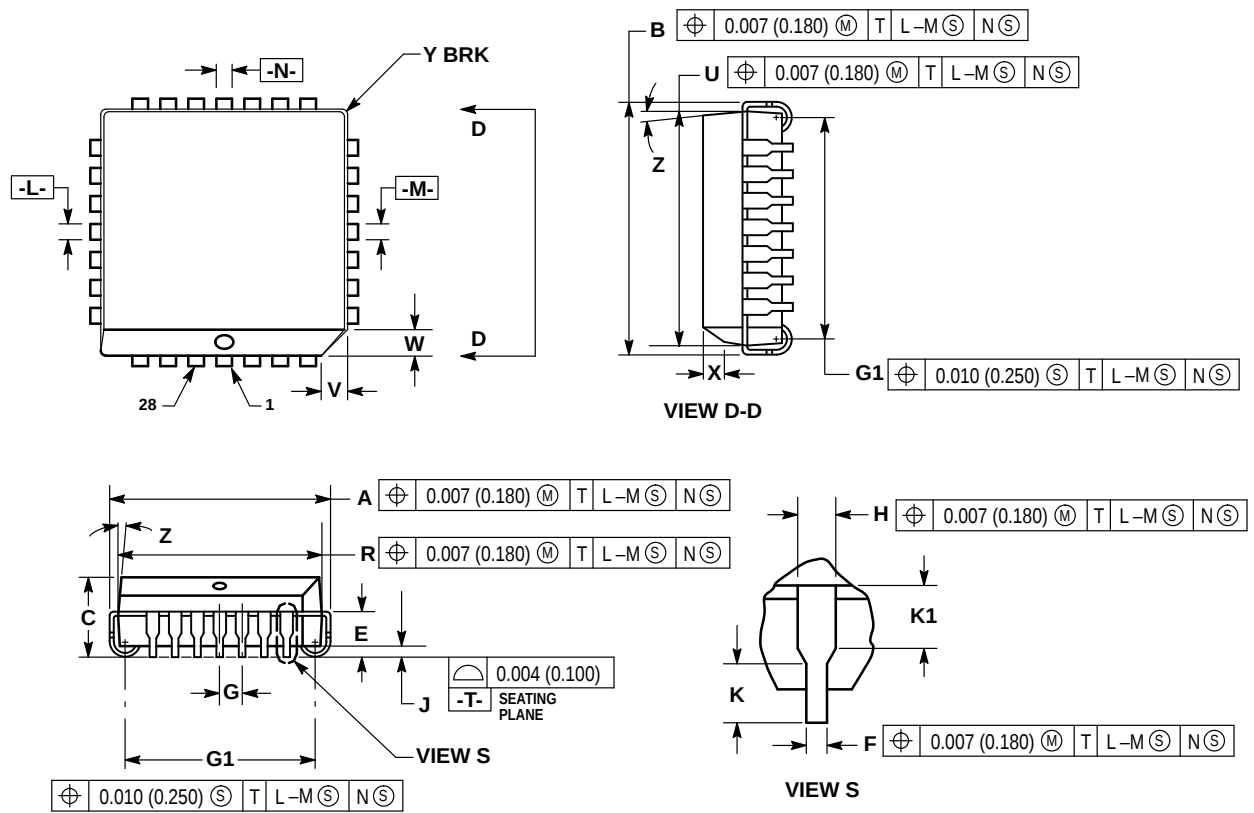
Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
V_{CUT}	Cut-off Output Voltage ¹	- 2.10		- 2.03	- 2.10		- 2.03	- 2.10		- 2.03	V	
I_{IH}	Input HIGH Current All Other Inputs			150			150			150	μA	
I_{EE}	Power Supply Current										mA	
	10E		145	174		145	174		145	174		
	100E		145	174		145	174		167	200		

1. measured with $V_{\text{TT}} = -2.10\text{V}$ **AC CHARACTERISTICS** ($V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$; $V_{CC} = V_{CCO} = \text{GND}$)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
t_{PLH} t_{PHL}	Propagation Delay to Output Clk to Q Clk to BUS <u>ABUSDIS</u> SYNCEN	450		1000	450		1000	450		1000	ps	
		800		1800	800		1800	800		1800		
		500		1500	500		1500	500		1500		
		800		1800	800		1800	800		1800		
t_{s}	Setup Time BUS SBUSEN Data, S-IN TEN, REN, SCAN	350			350			350			ps	
		100			100			100				
		400			400			400				
		550			550			550				
t_{h}	Hold Time BUS SBUSEN Data, S-IN TEN, REN, SCAN	350			350			350			ps	
		500			500			500				
		350			350			350				
		200			200			200				
t_{PW}	Minimum Pulse Width CLK	400			400			400			ps	
t_{r} t_{f}	Rise/Fall Times 20 - 80% (Q_n) 20 - 80% (BUSn Rise) 20 - 80% (BUSn Fall)	300		800	300		800	300		800	ps	
		500		1000	500		1000	500		1000		
		300		800	300		800	300		800		

OUTLINE DIMENSIONS

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PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE D



NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050	BSC	1.27	BSC
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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