

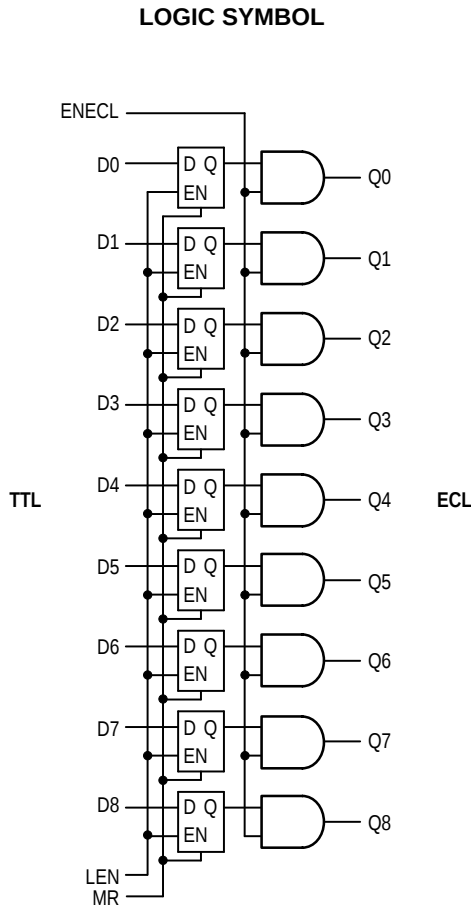
9-Bit Latch TTL/ECL Translator

The MC10H/100H602 is a 9-bit, dual supply TTL to ECL translator with latch. Devices in the Motorola 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

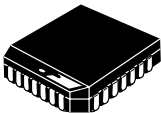
The H602 features D-type latches. Latching is controlled by Latch Enable (LEN), while the Master Reset input resets the latches. A post-latch logic enable is also provided (ENECL), allowing control of the output state without destroying latch data. All control inputs are ECL level.

The 10H version is compatible with MECL 10H ECL logic levels. The 100H version is compatible with 100K levels.

- 9-Bit Ideal for Byte-Parity Applications
- Flow-Through Configuration
- Extra TTL and ECL Power/Ground Pins to Minimize Switching Noise
- Dual Supply
- 3.5 ns Max D to Q
- PNP TTL Inputs for Low Loading



MC10H602 MC100H602



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

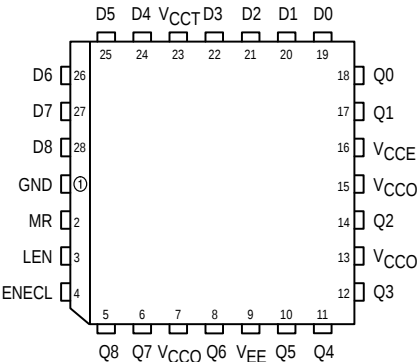
PIN NAMES

PIN	FUNCTION
GND	TTL Ground (0 V)
V _{CCE}	ECL V _{CC} (0 V)
V _{CCO}	ECL V _{CC} (0 V) — Outputs
V _{CCT}	TTL Supply (+5.0 V)
V _{EE}	ECL Supply (–5.2/–4.5 V)
D0–D8	Data Inputs (TTL)
Q0–Q8	Data Outputs (ECL)
ENECL	Enable Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

TRUTH TABLE

D	LEN	MR	ENECL	Q
L	L	L	H	L
H	L	L	H	H
X	H	L	H	Q ₀
X	X	H	H	L
X	X	X	L	L

Pinout: 28-Lead PLCC (Top View)



MC10H602 MC100H602

DC CHARACTERISTICS: $V_{CCT} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -5.2\text{ V} \pm 5\%$ (10H version); $V_{EE} = -4.2\text{ V}$ to -5.5 V (100H version)

Symbol	Parameter		0°C		25°C		75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
	Power Supply Current									
I_{EE}	ECL	10H 100H		-125 -122		-125 -123		-125 -132	mA	
I_{CCH} I_{CCL}	TTL			48 50		48 50		48 50	mA	

AC CHARACTERISTICS: $V_{CCT} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -5.2\text{ V} \pm 5\%$ (10H version); $V_{EE} = -4.2\text{ V}$ to -5.5 V (100H version)

Symbol	Parameter		0°C		25°C		75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output	D LEN MR ENECL	1.4 2.0 2.0 1.6	3.0 3.4 3.4 3.2	1.5 2.1 2.1 1.7	3.2 3.5 3.5 3.3	1.7 2.4 2.5 1.8	3.5 3.7 3.9 3.7	ns	
t_s	Set-Up Time, D to LEN		2.0		2.0		2.0		ns	
t_h	Hold Time, D to LEN		1.0		1.0		1.0		ns	
$t_{w(L)}$	LEN Pulse Width, LOW		2.0		2.0		2.0		ns	
t_R t_F	Output Rise/Fall Time 20%–80%		0.5	1.5	0.5	1.5	0.5	1.5	ns	

10H ECL DC CHARACTERISTICS: $V_{CCT} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -5.2\text{ V} \pm 5\%$

Symbol	Parameter		0°C		25°C		75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current			225		145		145	μA μA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage		-1170 -1950	-840 -1480	-1130 -1950	-810 -1480	-1070 -1950	-735 -1450	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage		-1020 -1950	-840 -1630	-980 -1950	-810 -1630	-920 -1950	-735 -1600	mV	50 Ω to -2.0 V

100H ECL DC CHARACTERISTICS: $V_{CCT} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -4.2\text{ V}$ to -5.5 V

Symbol	Parameter		0°C		25°C		75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
I_{IH} I_{IL}	Input HIGH Current Input LOW Current			225		145		145	μA μA	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage		-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	mV	
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage		-1025 -1810	-880 -1620	-1025 -1810	-880 -1620	-1025 -1810	-880 -1620	mV	50 Ω to -2.0 V

TTL DC CHARACTERISTICS: $V_{CCT} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -5.2\text{ V} \pm 5\%$ (10H version); $V_{EE} = -4.2\text{ V}$ to -5.5 V (100H version)

Symbol	Parameter		0°C		25°C		75°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage		2.0	0.8	2.0	0.8	2.0	0.8	V V	
I_{IH}	Input HIGH Current			20 100		20 100		20 100	μA	$V_{IN} = 2.7\text{ V}$ $V_{IN} = 7.0\text{ V}$
I_{IL}	Input LOW Current			-0.6		-0.6		-0.6	mA	$V_{IN} = 0.5\text{ V}$
V_{IK}	Input Clamp Voltage			-1.2		-1.2		-1.2	V	$I_{IN} = -18\text{ mA}$

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MC10H602/D

