

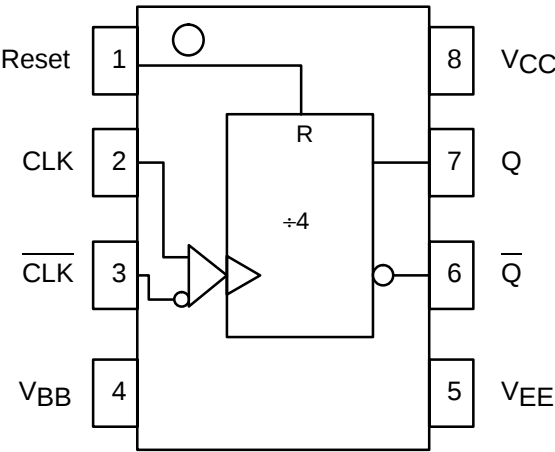
÷4 Divider

The MC100LVEL33 is an integrated ÷4 divider. The differential clock inputs and the V_{BB} allow a differential, single-ended or AC coupled interface to the device. If used, the V_{BB} output should be bypassed to ground with a 0.01μF capacitor. Also note that the V_{BB} is designed to be used as an input bias on the EL33 only, the V_{BB} output has limited current sink and source capability. The LVEL is functionally equivalent to the EL33 and works from a low voltage supply.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple LVEL33's in a system.

- 630ps Propagation Delay
- 4.0GHz Toggle Frequency
- High Bandwidth Output Transitions
- Operates from -3.3V (or 3.3V) Supply
- 75kΩ Internal Input Pulldown Resistors
- >2000V ESD Protection

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



MC100LVEL33



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05

PIN DESCRIPTION

PIN	FUNCTION
CLK	Clock Inputs
Reset	Asynch Reset
V _{BB}	Ref Voltage Output
Q	Data Outputs



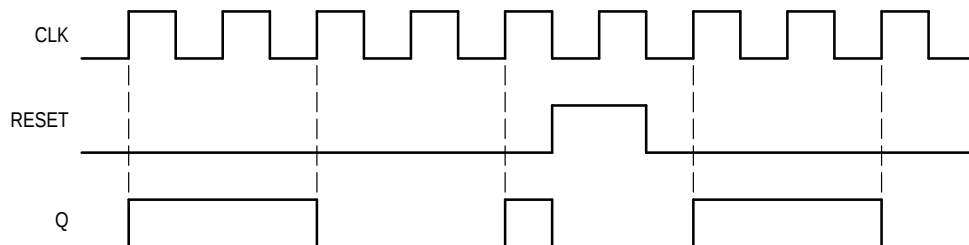
DC CHARACTERISTICS ($V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$; $V_{CC} = \text{GND}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		33	37		33	37		33	37		35	39	mA
V_{EE}	Power Supply Voltage	-3.0		-3.8	-3.0		-3.8	-3.0		-3.8	-3.0		-3.8	V
V_{BB}	Output Reference Voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{IL}	Input LOW Current CLK Other	-600 0.5			-600 0.5			-600 0.5			-600 0.5			μA

AC CHARACTERISTICS ($V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$; $V_{CC} = \text{GND}$)

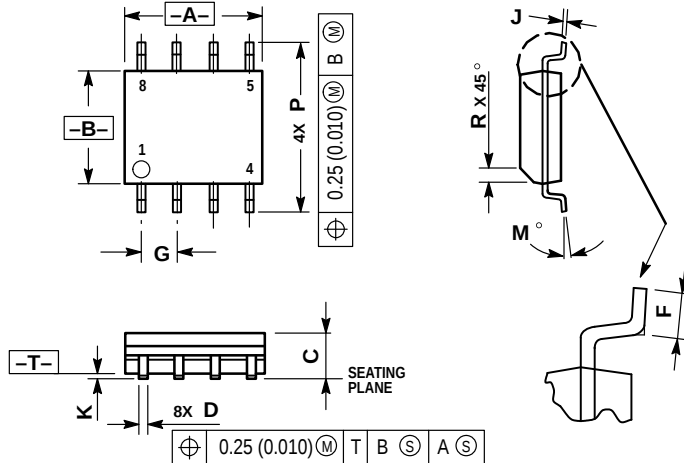
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency	3.4	4.2		3.8	4.2		3.8	4.2		3.8	4.2		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE) Reset to Q	510 460 500		690 740 700	530 480 510		710 760 710	540 490 520		720 770 720	600 550 580		780 830 780	ps
t_{rr}	Reset Recovery	300			300			300			300			ps
t_{skew}	Duty Cycle Skew ²			20			20			20			20	ps
V_{PP}	Minimum Input Swing ¹	150			150			150			150			mV
V_{CMR}	Common Mode Range ³ $V_{\text{PP}} < 500\text{mV}$ $V_{\text{PP}} \geq 500\text{mV}$	-2.0 -1.8		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	V
t_{r} t_{f}	Output Rise/Fall Times Q (20% – 80%)	120		320	120		320	120		320	120		320	ps

1. Minimum input swing for which AC parameters are guaranteed.
2. Duty cycle skew is the difference between T_{PLH} and T_{PLL} .
3. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PPmin} and 1V. The lower end of the CMR range varies 1:1 with V_{EE} . The numbers in the spec table assume a nominal $V_{\text{EE}} = -3.3\text{V}$. Note for PECL operation, the $V_{\text{CMR}}(\text{min})$ will be fixed at $3.3\text{V} - |V_{\text{CMR}}(\text{min})|$.

**Figure 1. Timing Diagram**

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05
ISSUE P



NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DIMENSIONS ARE IN MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.18	0.25
K	0.10	0.25
M	0°	7°
P	5.80	6.20
R	0.25	0.50

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