

4-Bit Parallel-In/Parallel-Out Shift Register

The MC14035B 4-bit shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of a 4-stage clocked serial-shift register with synchronous parallel inputs and buffered parallel outputs. The Parallel/Serial (P/S) input allows serial-right shifting of data or synchronous parallel loading via inputs D_{P0} thru D_{P3} . The True/Complement (T/C) input determines whether the outputs display the Q or $\bar{Q}$ outputs of the flip-flop stages. J-K logic forms the serial input to the first stage. With the J and K inputs connected together they operate as a serial "D" input.

This device may be effectively used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, sample and hold registers, etc . . .

- 4-Stage Clocked Serial-Shift Operation
- Synchronous Parallel Loading of all Four Stages
- J-K Serial Inputs on First Stage
- Asynchronous True/Complement Control of all Outputs
- Fully Static Operation
- Asynchronous Master Reset
- Data Transfer Occurs on the Positive-Going Clock Transition
- No Limit on Clock Rise and Fall Times
- All Inputs are Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	- 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

TRUTH TABLE

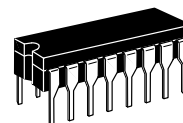
Inputs				t_n Output Q_0
C	J	$\bar{K}$	R	
$\nearrow$	0	0	0	0
$\nearrow$	0	1	0	$Q_0(n-1)$
$\nearrow$	1	0	0	$Q_0(n-1)$
$\nearrow$	1	1	0	1
$\searrow$	X	X	0	$Q_0(n-1)$
X	X	X	1	0

X = Don't Care

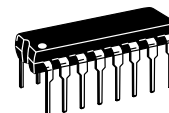
P/S = 0 = Serial Mode

T/C = 1 = True Outputs

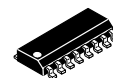
MC14035B



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

$T_A = -55^\circ$ to 125°C for all packages.

PIN ASSIGNMENT

Q0	1	16	V_{DD}
T/C	2	15	Q1
$\bar{K}$	3	14	Q2
J	4	13	Q3
R	5	12	D_{P3}
C	6	11	D_{P2}
P/S	7	10	D_{P1}
V_{SS}	8	9	D_{P0}

[illegible]

** The formulas given are for the typical characteristics only at 25°C.

$$I_T(C_I) = I_T(50 \text{ pF}) + (C_I - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_I in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.001$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$, See Figure 1)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time $T_{TLH}, T_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $T_{TLH}, T_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $T_{TLH}, T_{THL} = (0.55 \text{ ns/pF}) C_L + 12.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time, Clock or Reset to Q $T_{PLH}, T_{PHL} = (1.75 \text{ ns/pF}) C_L + 223 \text{ ns}$ $T_{PLH}, T_{PHL} = (0.70 \text{ ns/pF}) C_L + 89 \text{ ns}$ $T_{PLH}, T_{PHL} = (0.53 \text{ ns/pF}) C_L + 67 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	300 130 95	600 260 190	ns
Clock Pulse Width	t_{WH}	5.0 10 15	335 165 125	135 45 40	— — —	ns
Reset Pulse Width	t_{WH}	5.0 10 15	400 175 130	80 40 35	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	80 30 25	40 15 10	— — —	ns
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	No Limit			—
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	2.5 6.0 10	1.2 2.0 3.0	MHz
J-K to Clock Setup Time	t_{su}	5.0 10 15	500 200 150	120 50 30	— — —	ns
Clock to J-K Hold Time	t_h	5.0 10 15	40 30 25	-40 -5 0	— — —	ns
P/S to Clock Setup Time	t_{su}	5.0 10 15	500 200 150	25 10 7.5	— — —	ns
Clock to P/S Hold Time	t_h	5.0 10 15	30 20 20	-70 -20 -10	— — —	ns
Dp to Clock Setup Time	t_{su}	5.0 10 15	500 200 150	90 20 15	— — —	ns
Clock to Dp Hold Time	t_h	5.0 10 15	90 40 40	-25 0 5	— — —	ns

* The formulas given are for the typical characteristics only at 25°C .

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

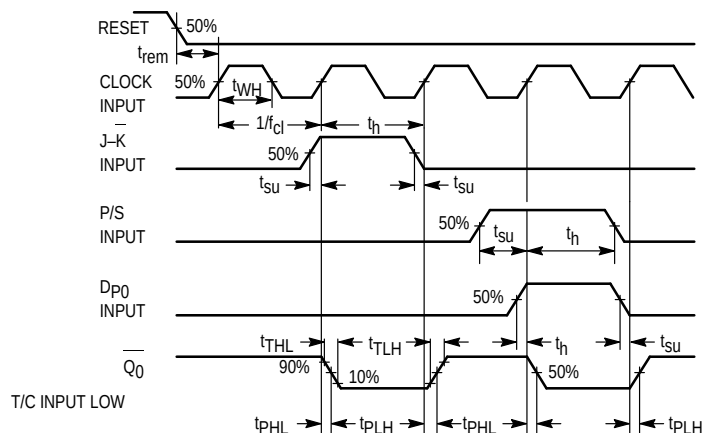
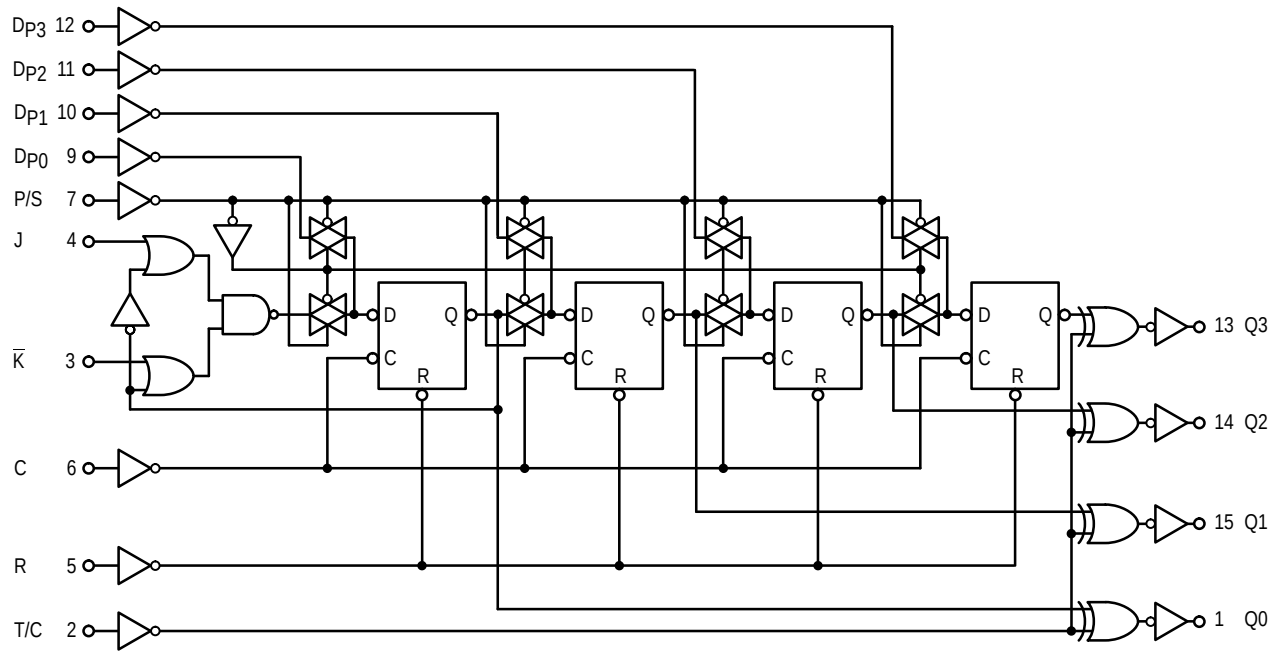
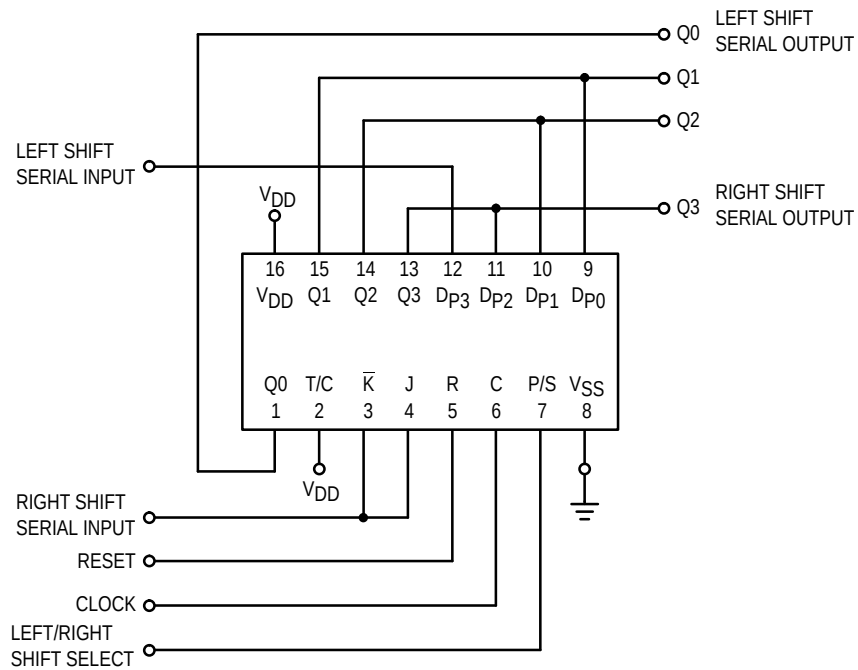


Figure 1. Timing Diagram

LOGIC DIAGRAM

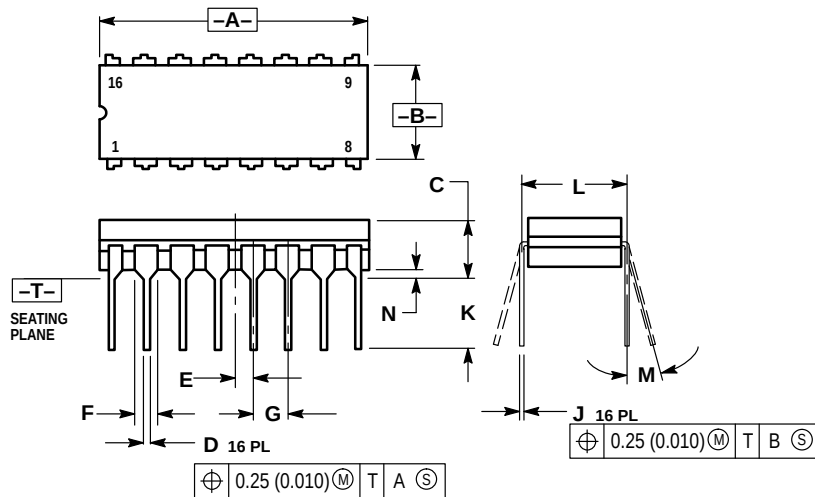


APPLICATION DIAGRAM Shift Left/Shift Right Register



OUTLINE DIMENSIONS

L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

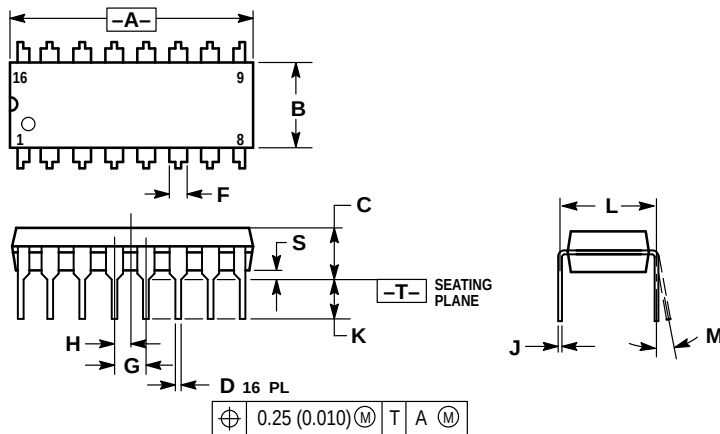


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050	BSC	1.27	BSC
F	0.055	0.065	1.40	1.65
G	0.100	BSC	2.54	BSC
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300	BSC	7.62	BSC
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



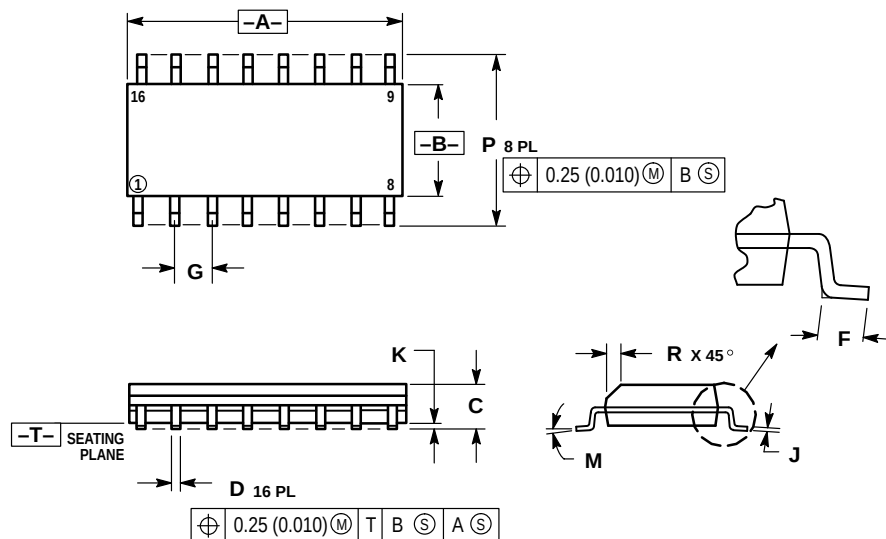
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
H	0.050	BSC	1.27	BSC
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



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MC14035B/D

