

# MC14551B

## Quad 2-Channel Analog Multiplexer/Demultiplexer

The MC14551B is a digitally-controlled analog switch. This device implements a 4PDT solid state switch with low ON impedance and very low OFF Leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ( $V_{DD} - V_{EE}$ ) = 3.0 to 18 V  
Note:  $V_{EE}$  must be  $\leq V_{SS}$
- Linearized Transfer Characteristics
- Low Noise —  $12 \text{ nV}/\sqrt{\text{Cycle}}$ ,  $f \geq 1.0 \text{ kHz}$  typical
- For Low  $R_{ON}$ , Use The HC4051, HC4052, or HC4053 High-Speed CMOS Devices
- Switch Function is Break Before Make

### MAXIMUM RATINGS\*

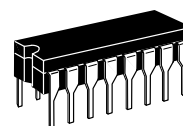
Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage (Referenced to $V_{EE}$ , $V_{SS} \geq V_{EE}$ )	- 0.5 to + 18.0	V
$V_{in}, V_{out}$	Input or Output Voltage (DC or Transient) (Referenced to $V_{SS}$ for Control Input & $V_{EE}$ for Switch I/O)	- 0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient), per Control Pin	$\pm 10$	mA
$I_{sw}$	Switch Through Current	$\pm 25$	mA
$P_D$	Power Dissipation, per Package†	500	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

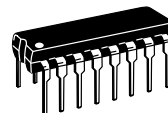
† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages - 12 mW/°C From 100°C To 125°C



**L SUFFIX**  
CERAMIC  
CASE 620



**P SUFFIX**  
PLASTIC  
CASE 648

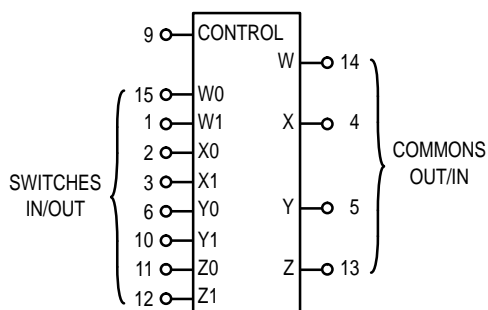


**D SUFFIX**  
SOIC  
CASE 751B

### ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.



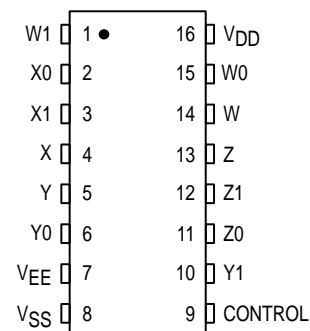
Control	ON
0	W0 X0 Y0 Z0
1	W1 X1 Y1 Z1

$V_{DD}$  = Pin 16

$V_{SS}$  = Pin 8

$V_{EE}$  = Pin 7

### PIN ASSIGNMENT



NOTE: Control Input referenced to  $V_{SS}$ . Analog Inputs and Outputs reference to  $V_{EE}$ .  $V_{EE}$  must be  $\leq V_{SS}$ .

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V <sub>DD</sub>	Test Conditions	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ #	Max	Min	Max	

### SUPPLY REQUIREMENTS (Voltages Referenced to V<sub>EE</sub>)

Power Supply Voltage Range	V <sub>DD</sub>	—	V <sub>DD</sub> - 3.0 ≥ V <sub>SS</sub> ≥ V <sub>EE</sub>	3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I <sub>DD</sub>	5.0 10 15	Control Inputs: V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub> , Switch I/O: V <sub>EE</sub> ≤ V <sub>I/O</sub> ≤ V <sub>DD</sub> , and ΔV <sub>switch</sub> ≤ 500 mV**	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I <sub>D(AV)</sub>	5.0 10 15	T <sub>A</sub> = 25°C only (The channel component, (V <sub>in</sub> - V <sub>out</sub> )/R <sub>on</sub> , is not included.)	Typical (0.07 μA/kHz) f + I <sub>DD</sub> (0.20 μA/kHz) f + I <sub>DD</sub> (0.36 μA/kHz) f + I <sub>DD</sub>							μA

### CONTROL INPUT (Voltages Referenced to V<sub>SS</sub>)

Low-Level Input Voltage	V <sub>IL</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High-Level Input Voltage	V <sub>IH</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I <sub>in</sub>	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C <sub>in</sub>	—		—	—	—	5.0	7.5	—	—	pF

### SWITCHES IN/OUT AND COMMONS OUT/IN — W, X, Y, Z (Voltages Referenced to V<sub>EE</sub>)

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	—	Channel On or Off	0	V <sub>DD</sub>	0	—	V <sub>DD</sub>	0	V <sub>DD</sub>	V <sub>p-p</sub>
Recommended Static or Dynamic Voltage Across the Switch** (Figure 3)	ΔV <sub>switch</sub>	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V <sub>OO</sub>	—	V <sub>in</sub> = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R <sub>on</sub>	5.0 10 15	ΔV <sub>switch</sub> ≤ 500 mV**, V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control), and V <sub>in</sub> = 0 to V <sub>DD</sub> (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR <sub>on</sub>	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off-Channel Leakage Current (Figure 8)	I <sub>off</sub>	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	C <sub>I/O</sub>	—	Switch Off	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	C <sub>O/I</sub>	—		—	—	—	17	—	—	—	pF
Capacitance, Feedthrough (Channel Off)	C <sub>I/O</sub>	— —	Pins Not Adjacent Pins Adjacent	— —	— —	— —	0.15 0.47	— —	— —	— —	pF

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

\*\* For voltage drops across the switch (ΔV<sub>switch</sub>) > 600 mV (> 300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn; i.e. the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

**ELECTRICAL CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{EE} \leq V_{SS}$ )

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Min	Typ #	Max	Unit
Propagation Delay Times Switch Input to Switch Output ( $R_L = 10 \text{ k}\Omega$ ) $t_{PLH}$ , $t_{PHL} = (0.17 \text{ ns/pF}) C_L + 26.5 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.08 \text{ ns/pF}) C_L + 11 \text{ ns}$ $t_{PLH}$ , $t_{PHL} = (0.06 \text{ ns/pF}) C_L + 9.0 \text{ ns}$	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	35 15 12	90 40 30	ns
Control Input to Output ( $R_L = 10 \text{ k}\Omega$ ) $V_{EE} = V_{SS}$ (Figure 4)	$t_{PLH}$ , $t_{PHL}$	5.0 10 15	— — —	350 140 100	875 350 250	ns
Second Harmonic Distortion $R_L = 10 \text{ k}\Omega$ , $f = 1 \text{ kHz}$ , $V_{in} = 5 V_{p-p}$	—	10	—	0.07	—	%
Bandwidth (Figure 5) $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p. $20 \text{ Log} (V_{out}/V_{in}) = -3 \text{ dB}$ , $C_L = 50 \text{ pF}$	BW	10	—	17	—	MHz
Off Channel Feedthrough Attenuation, Figure 5 $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p. $f_{in} = 55 \text{ MHz}$	—	10	—	-50	—	dB
Channel Separation (Figure 6) $R_L = 1 \text{ k}\Omega$ , $V_{in} = 1/2 (V_{DD} - V_{EE})$ p-p. $f_{in} = 3 \text{ MHz}$	—	10	—	-50	—	dB
Crosstalk, Control Input to Common O/I, Figure 7 $R_1 = 1 \text{ k}\Omega$ , $R_L = 10 \text{ k}\Omega$ , Control $t_r = t_f = 20 \text{ ns}$	—	10	—	75	—	mV

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$  for control inputs and  $V_{EE} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$  for Switch I/O.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$ ,  $V_{EE}$ , or  $V_{DD}$ ). Unused outputs must be left open.

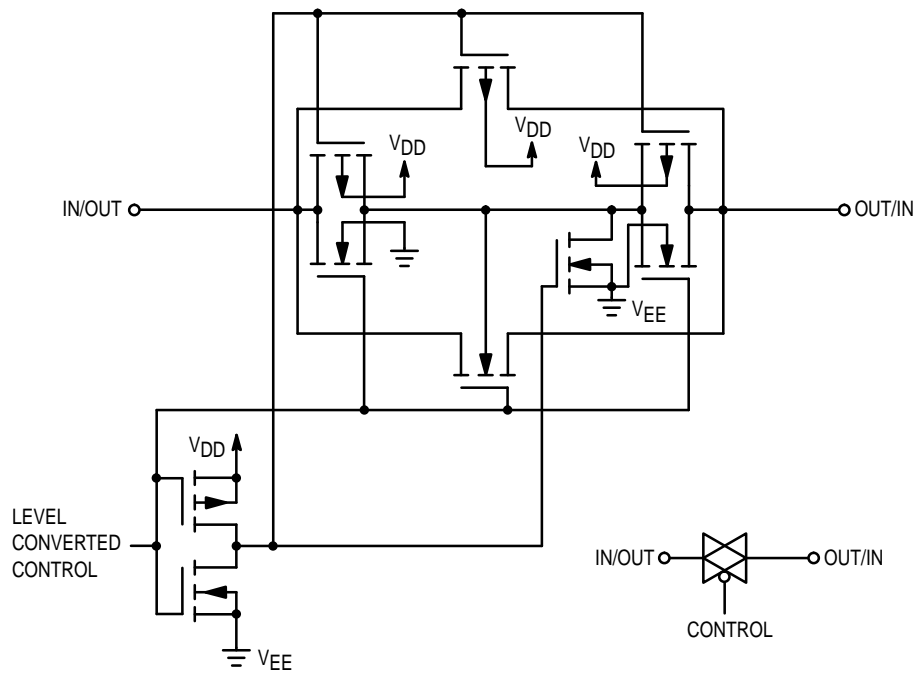


Figure 1. Switch Circuit Schematic

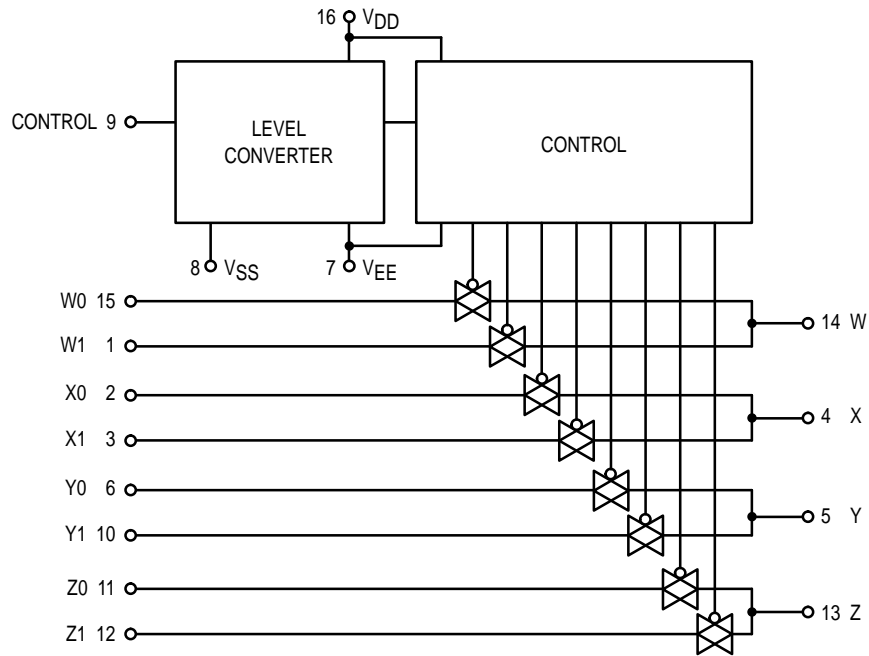
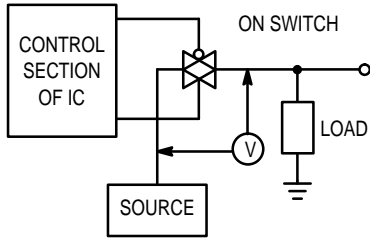
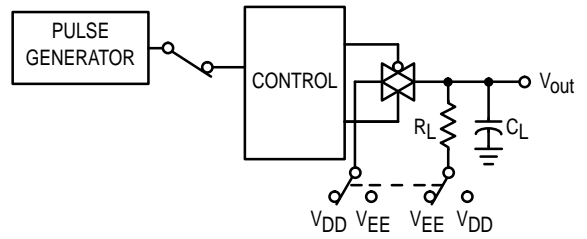


Figure 2. MC14551B Functional Diagram

## TEST CIRCUITS

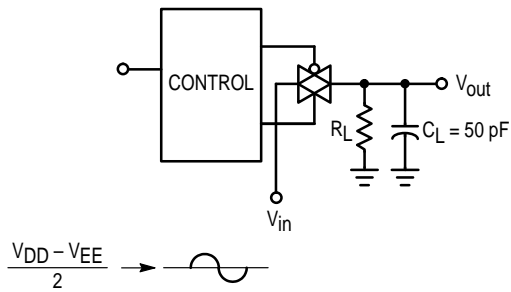


**Figure 3.  $\Delta V$  Across Switch**

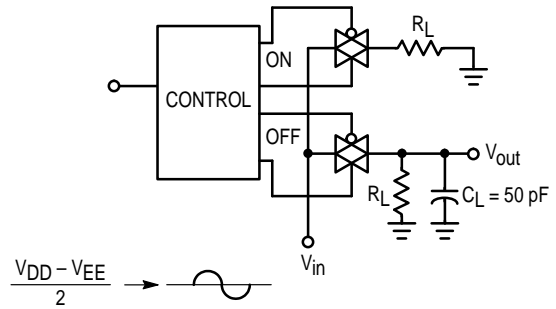


**Figure 4. Propagation Delay Times, Control to Output**

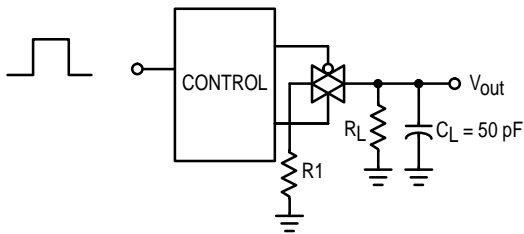
Control input used to turn ON or OFF the switch under test.



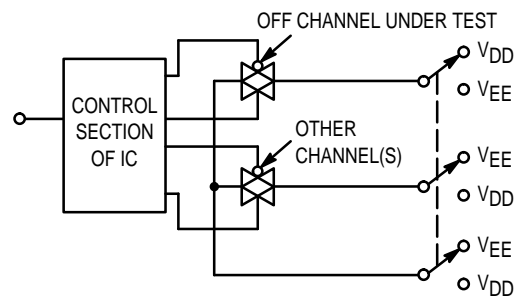
**Figure 5. Bandwidth and Off-Channel Feedthrough Attenuation**



**Figure 6. Channel Separation (Adjacent Channels Used for Setup)**



**Figure 7. Crosstalk, Control Input to Common O/I**



**Figure 8. Off Channel Leakage**

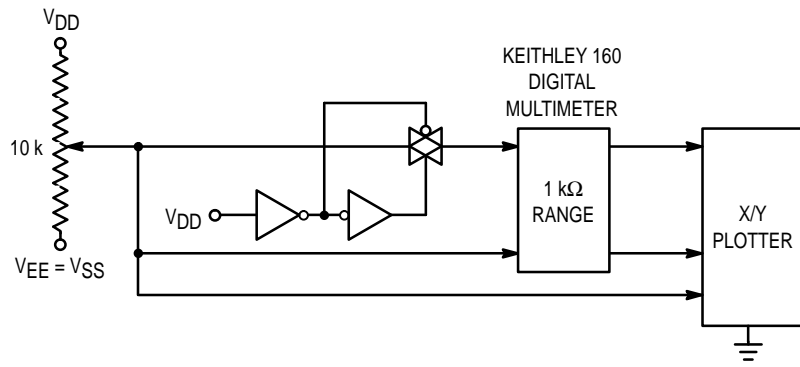


Figure 9. Channel Resistance ( $R_{ON}$ ) Test Circuit

### TYPICAL RESISTANCE CHARACTERISTICS

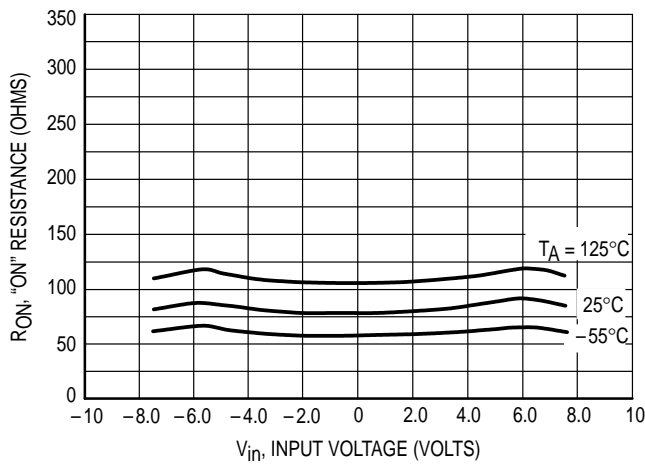


Figure 10.  $V_{DD}$  @ 7.5 V,  $V_{EE}$  @ -7.5 V

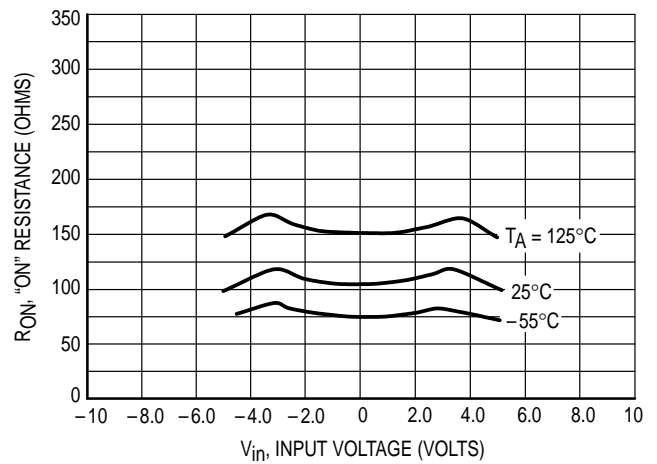


Figure 11.  $V_{DD}$  @ 5.0 V,  $V_{EE}$  @ -5.0 V

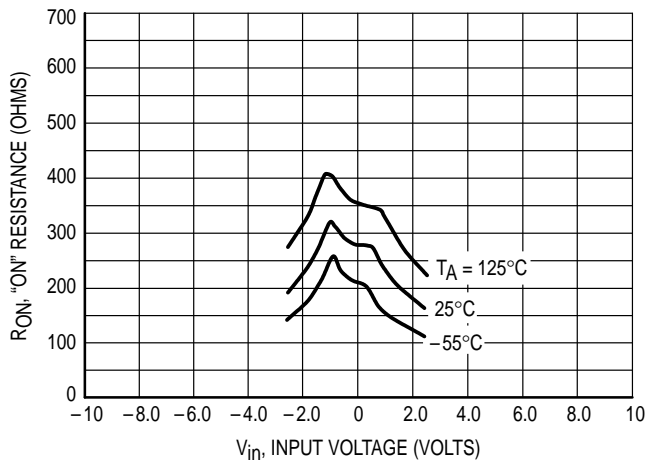


Figure 12.  $V_{DD}$  @ 2.5 V,  $V_{EE}$  @ -2.5 V

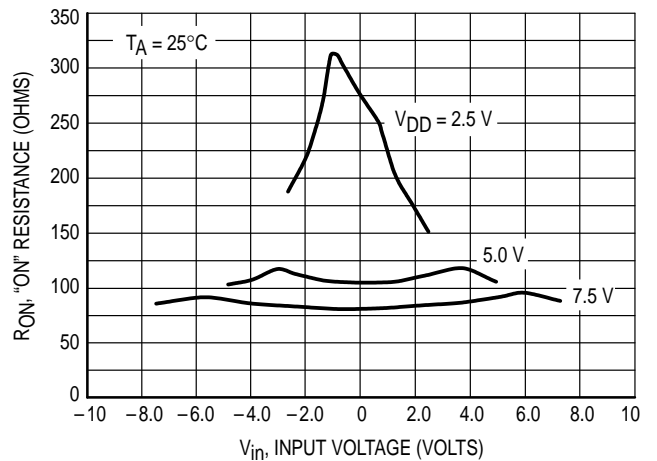


Figure 13. Comparison at 25°C,  $V_{DD}$  @ - $V_{EE}$

## APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figure 2. The 0-to-5 volt Digital Control signal is used to directly control a 9 V<sub>p-p</sub> analog signal.

The digital control logic levels are determined by V<sub>DD</sub> and V<sub>SS</sub>. The V<sub>DD</sub> voltage is the logic high voltage; the V<sub>SS</sub> voltage is logic low. For the example, V<sub>DD</sub> = +5 V = logic high at the control inputs; V<sub>SS</sub> = GND = 0 V = logic low.

The maximum analog signal level is determined by V<sub>DD</sub> and V<sub>EE</sub>. The V<sub>DD</sub> voltage determines the maximum recommended peak above V<sub>SS</sub>. The V<sub>EE</sub> voltage determines the maximum swing below V<sub>SS</sub>. For the example, V<sub>DD</sub> - V<sub>SS</sub> = 5 volt maximum swing above V<sub>SS</sub>; V<sub>SS</sub> - V<sub>EE</sub> = 5 volt maximum swing below V<sub>SS</sub>. The example shows a ± 4.5 volt signal which allows a 1/2 volt margin at each peak. If voltage

transients above V<sub>DD</sub> and/or below V<sub>EE</sub> are anticipated on the analog channels, external diodes (D<sub>x</sub>) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V<sub>DD</sub> and V<sub>EE</sub> is 18.0 volts. Most parameters are specified up to 15 volts which is the recommended maximum difference between V<sub>DD</sub> and V<sub>EE</sub>.

Balanced supplies are not required. However, V<sub>SS</sub> must be greater than or equal to V<sub>EE</sub>. For example, V<sub>DD</sub> = +10 volts, V<sub>SS</sub> = +5 volts, and V<sub>EE</sub> = -3 volts is acceptable. See the table below.

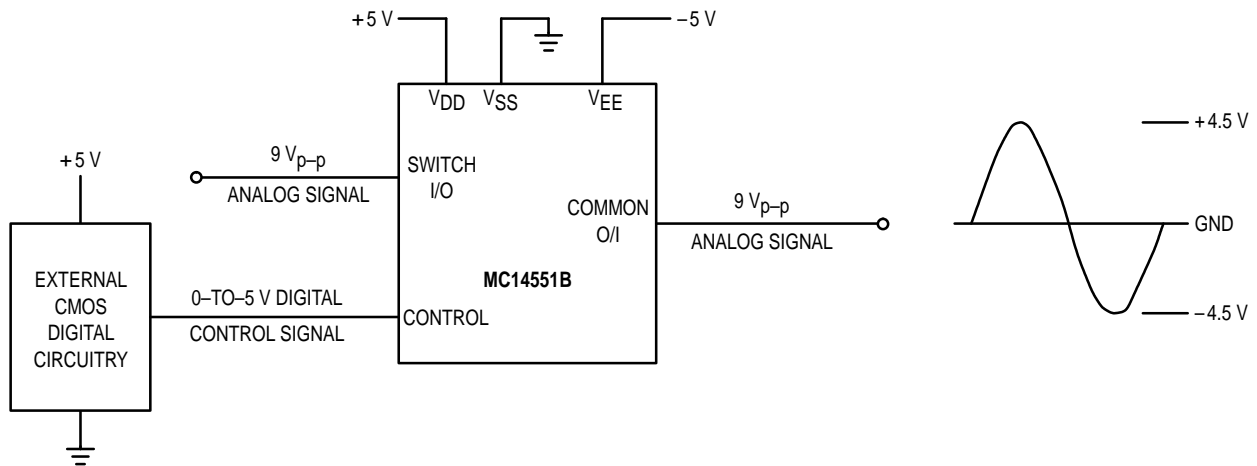


Figure A. Application Example



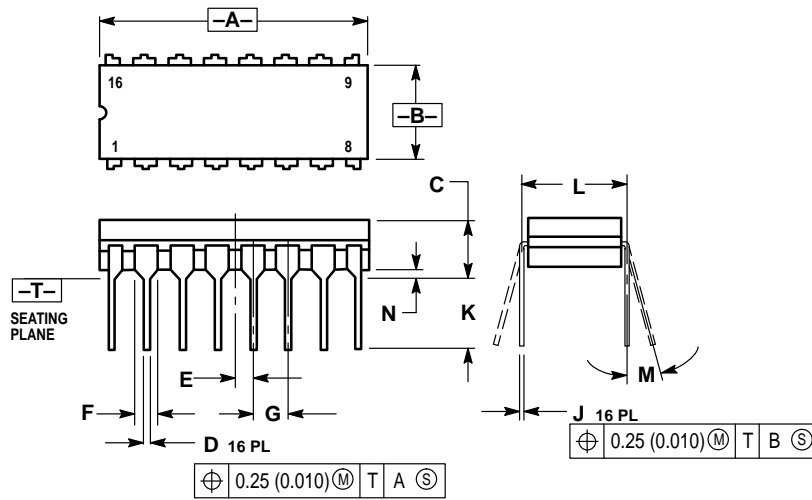
Figure B. External Schottky or Germanium Clipping Diodes

### POSSIBLE SUPPLY CONNECTIONS

V <sub>DD</sub> In Volts	V <sub>SS</sub> In Volts	V <sub>EE</sub> In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+ 8	0	- 8	+ 8/0	+ 8 to - 8 = 16 V <sub>p-p</sub>
+ 5	0	- 12	+ 5/0	+ 5 to - 12 = 17 V <sub>p-p</sub>
+ 5	0	0	+ 5/0	+ 5 to 0 = 5 V <sub>p-p</sub>
+ 5	0	- 5	+ 5/0	+ 5 to - 5 = 10 V <sub>p-p</sub>
+ 10		- 5	+ 10/ + 5	+ 10 to - 5 = 15 V <sub>p-p</sub>

## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

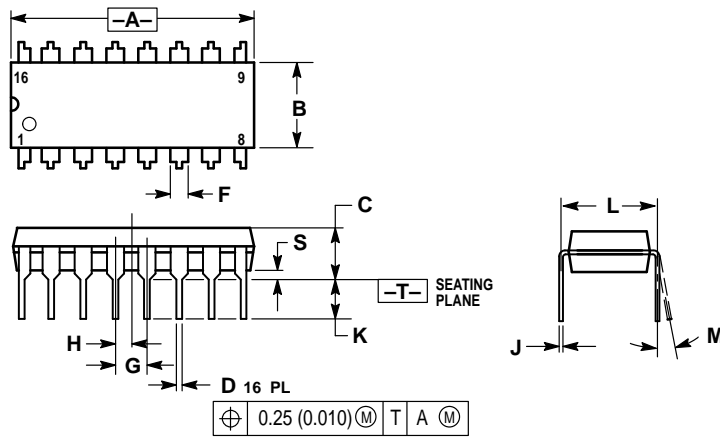


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



**NOTES:**

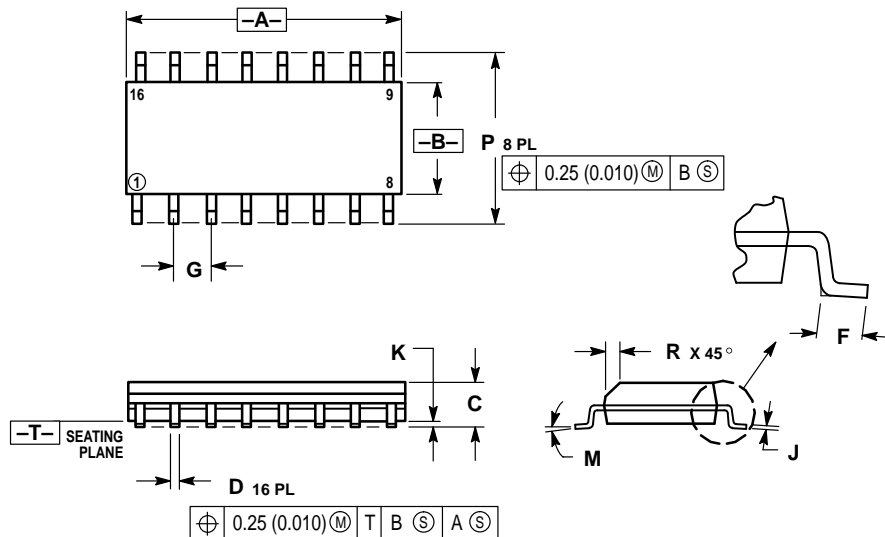
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01



## OUTLINE DIMENSIONS

### D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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MC14551B/D

