MC14559B
See Page 398

MC14560B

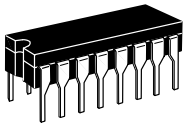
NBCD Adder

The MC14560B adds two 4–bit numbers in NBCD (natural binary coded decimal) format, resulting in sum and carry outputs in NBCD code.

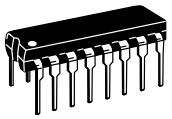
This device can also subtract when one set of inputs is complemented with a 9's Complementer (MC14561B).

All inputs and outputs are active high. The carry input for the least significant digit is connected to V_{SS} for no carry in.

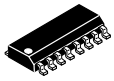
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



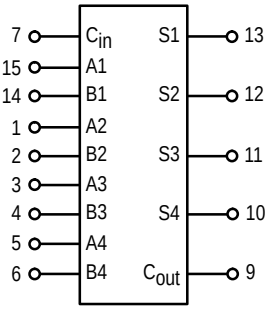
D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = – 55° to 125°C for all packages.

BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

TRUTH TABLE*

Input									Output				
A4	A3	A2	A1	B4	B3	B2	B1	C_{in}	C_{out}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	1	1	1	1	0	0	1

* Partial truth table to show logic operation for representative input values.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

REV 0
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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage “0” Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
“1” Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (1.68 µA/kHz) f + I_{DD} I_T = (3.35 µA/kHz) f + I_{DD} I_T = (5.03 µA/kHz) f + I_{DD}							µAdc

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

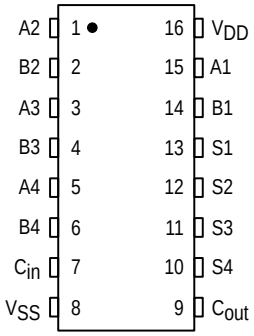
** The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

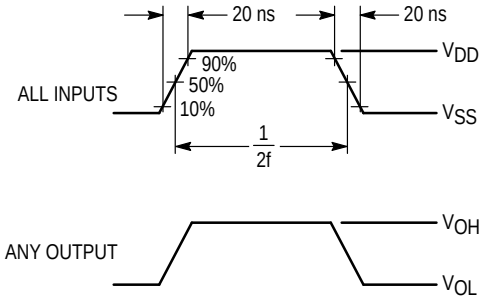
PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
A or B to S						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns		5.0	—	750	2100	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 297 ns		10	—	330	900	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 195 ns		15	—	220	675	
A or B to C_{out}						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	—	650	1800	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	—	230	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	—	170	450	
C_{in} to C_{out}						ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 465 ns		5.0	—	550	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 187 ns		10	—	220	600	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 135 ns		15	—	160	450	
Turn–Off Delay Time	t_{PLH}					ns
C_{in} to S						
t_{PLH} = (1.7 ns/pF) C_L + 715 ns		5.0	—	800	2250	
t_{PLH} = (0.66 ns/pF) C_L + 197 ns		10	—	350	975	
t_{PLH} = (0.5 ns/pF) C_L + 215 ns		15	—	240	750	
Turn–On Delay Time	t_{PHL}					ns
C_{in} to S						
t_{PHL} = (1.7 ns/pF) C_L + 565 ns		5.0	—	650	1800	
t_{PHL} = (0.66 ns/pF) C_L + 197 ns		10	—	230	600	
t_{PHL} = (0.5 ns/pF) C_L + 145 ns		15	—	170	450	

* The formulas given are for the typical characteristics only at 25°C.
#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.



Duty Cycle = 50%

All outputs connected to respective C_L loads

f = System clock frequency

Figure 1. Power Dissipation Waveforms

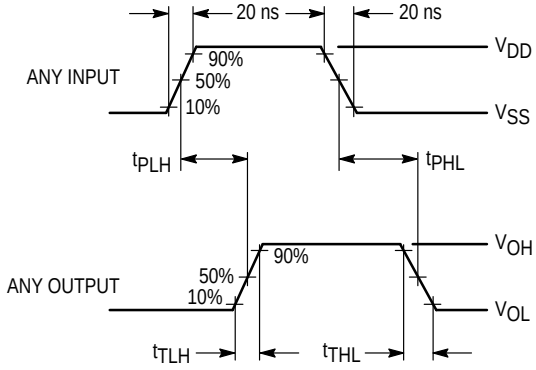
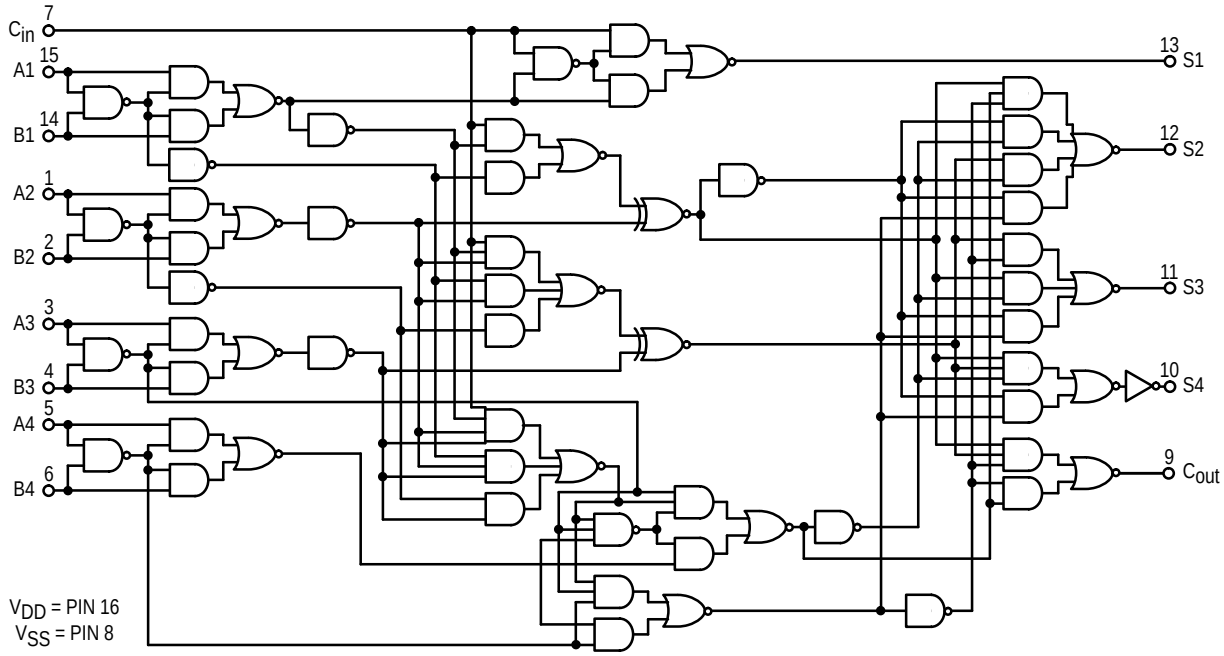


Figure 2. Switching Time Waveforms

FUNCTIONAL EQUIVALENT LOGIC DIAGRAM



One MC14560B and MC14561B permit a BCD digit to be added to or subtracted from a second digit, such as in this typical configuration. A second MC14561B permits either digit to be added to or subtracted from the other, or either word to appear unmodified at the output.

TRUTH TABLE

Zero	Add/Subtract	Result
0	0	B plus A
0	1	B minus A
1	X	B

X = Don't Care

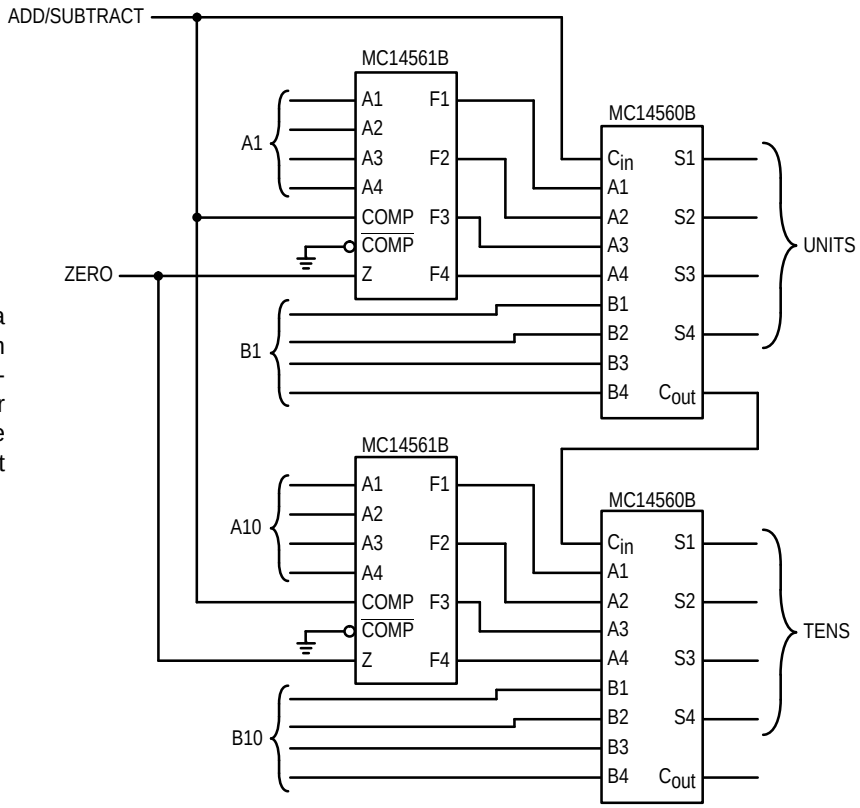


Figure 3. Parallel Add/Subtract Circuit

APPLICATIONS INFORMATION

INTRODUCTION

Frequently in small digital systems, simple decimal arithmetic is performed. Decimal data enters and leaves the system arithmetic unit in a binary coded decimal (BCD) format. The adder/subtracter in the arithmetic unit may be required to accept sign as well as magnitude, and generate sign, magnitude, and overflow. In the past, it has been cumbersome to build sign and magnitude adder/subtracters. Now, using Motorola's MSI CMOS functions, the MC14560 NBCD Adders and MC14561 9's Complementers, NBCD adder/subtracters may be built economically, with surprisingly low package count and moderate speed.

Some background information on BCD arithmetic is presented here, followed by simple circuits for unsigned adder/subtracters. The final circuit discussed is an adder/subtracter for signed numbers with complete overflow and sign correction logic.

DECIMAL NUMBER REPRESENTATION

Because logic elements are binary or two–state devices, decimal digits are generally represented as a group of bits in a weighted format. There are many possible binary codes which can be used to represent a decimal number. One of the most popular codes using 4 binary digits to represent 0 thru 9 is Natural Binary Coded Decimal (NBCD or 8–4–2–1 code).

NBCD is a weighted code. If a value of "0" or "1" is assigned to each of the bit positions, where the rightmost position is 2^0 and the leftmost is 2^3, and the values are summed for a given code, the result is equal to the decimal digit represented by the code. Thus, 0110 equals $0 \cdot 2^3 + 1 \cdot 2^2 + 1 \cdot 2^1 + 0 \cdot 2^0 = 4 + 2 = 6$. The 1010, 1011, 1100, 1101, 1110, and 1111 binary codes are not used. Because of these illegal states, the addition and subtraction of NBCD numbers is more complex than similar calculations on straight binary numbers.

ADDITION OF UNSIGNED NBCD NUMBERS

When 2 NBCD digits, A and B, and a possible carry, C, are added, a total of 20 digit sums (A + B + C) are possible as shown in Table 1.

The binary representations for the digit sums 10 thru 19 are offset by 6, the number of unused binary states, and are not correct. An algorithm for obtaining the correct sum is shown in Figure 1. A conventional method of implementing the BCD addition algorithm is shown in Figure 2(a). The NBCD digits, A and B, are summed by a 4 bit binary full adder. The resultant (sum and carry) is input to a binary/BCD code converter which generates the correct BCD code and carry.

An NBCD adder block which performs the above function is available in a single CMOS package (MC14560). Figure 2(b) shows n decades cascaded for addition of n digit unsigned NBCD numbers. Add time is typically 0.1 + 0.2n μs for n decades. When the carry out of the most significant decade is a logical "1", an overflow is indicated.

COMPLEMENT ARITHMETIC

Complement arithmetic is used in NBCD subtraction. That is, the "complement" of the subtrahend is added to the minuend. The complementing process amounts to biasing the subtrahend such that all possible sums are positive. Consider the subtraction of the NBCD numbers, A and B:

$$R = A - B$$

where R is the result. Now bias both sides of the equation by $10^N - 1$ where N is the number of digits in A and B.

$$R + 10^N - 1\ A - B + 10^N - 1$$

Rearranging,

$$R + 10^N - 1\ A + (10^N - 1 - B)$$

The term $(10^N - 1 - B)$, – B biased by $10^N - 1$, is known as the 9's complement of B. When A > B, $R + 10^N - 1 > 10^N - 1$; thus R is a positive number. To obtain R, 1 is added to $R + 10^N - 1$, and the carry term, 10^N, is dropped. The addition of 1 is called End Around Carry (EAC).

When A < B, $R + 10^N - 1 < 10^N - 1$, no EAC results and R is a negative number biased by $10^N - 1$; thus $R + 10^N - 1$ is the 9's complement of R.

SUBTRACTION OF UNSIGNED NBCD NUMBERS

Nine's complement arithmetic requires an element to perform the complementing function. An NBCD 9's complementer may be implemented using a 4 bit binary adder and 4 inverters, or with combinatorial logic. The Motorola MC14561 9's complementer is available in a single package. It has true and inverted complement disable, which allow straight–through or complement modes of operation. A "zero" line forces the output to "0". Figure 3 shows an NBCD subtracter block using the MC14560 and MC14561. Also shown are n cascaded blocks for subtraction of n digit unsigned numbers. Subtract time is 0.6 + 0.4n μs for n stages. Underflow (borrow) is indicated by a logical "0" on the carry output of the most significant digit. A "0" carry also indicates that the difference is a negative number in 9's complement form. If the result is input to a 9's complementer, as shown, and its mode controlled by the carry out of the most significant digit, the output of the complementer will be the correct negative magnitude. Note that the carry out of the most significant digit (MSD) is the input to carry in of the least significant digit (LSD). This End Around Carry is required because subtraction is done in 9's complement arithmetic.

By controlling the complement and overflow logic with an add/subtract line, both addition and subtraction are performed using the basic subtracter blocks (Figure 4).

Table 1. Sum = A + B + C

Binary Sums	Decimal Numbers	Corrected Binary Sums
0000	0	0000
0001	1	0001
0010	2	0010
0011	3	0011
0100	4	0100
0101	5	0101
0110	6	0110
0111	7	0111
1000	8	1000
1001	9	1001
1010 (Non valid BCD representation)	10	0000 + Carry
1011 (Non valid BCD representation)	11	0001 + Carry
1100 (Non valid BCD representation)	12	0010 + Carry
1101 (Non valid BCD representation)	13	0011 + Carry
1110 (Non valid BCD representation)	14	0100 + Carry
1111 (Non valid BCD representation)	15	0101 + Carry
0000 + Carry	16	0110 + Carry
0001 + Carry	17	0111 + Carry
0010 + Carry	18	1000 + Carry
0011 + Carry	19	1001 + Carry

ADDITION AND SUBTRACTION OF SIGNED NBCD NUMBERS

Using MC14560 NBCD Adders and MC14561 9's Complementers, a sign and magnitude adder/subtracter can be configured (Figure 5). Inputs A and B are signed positive (A_S, B_S = "0") or negative (A_S, B_S = "1"). B is added to or subtracted from A under control of an Add/Sub line (subtraction = "1"). The result, R, of the operation is positive signed, positive signed with overflow, negative signed, or negative signed with overflow. Add/subtract time is typically 0.6 + 0.4n μs for n decades.

An exclusive–OR of Add/Sub line and B_S produces B′, which controls the B complementers. If B_S, the sign of B, is a logical "1" (B is negative) and the Add/Sub line is a "0" (add B to A), then the output of the exclusive–OR (B_S') is a logical "1" and B is complemented. If B_S = "1" and Add/Sub = "1", B is not complemented since subtracting a negative number is the same as adding a positive number. When Add/Sub is a "1" and B_S = "0", B_S' is a "1" and B is complemented. The A complementer is controlled by the A sign bit, A_S. When A_S = "1", A is complemented.

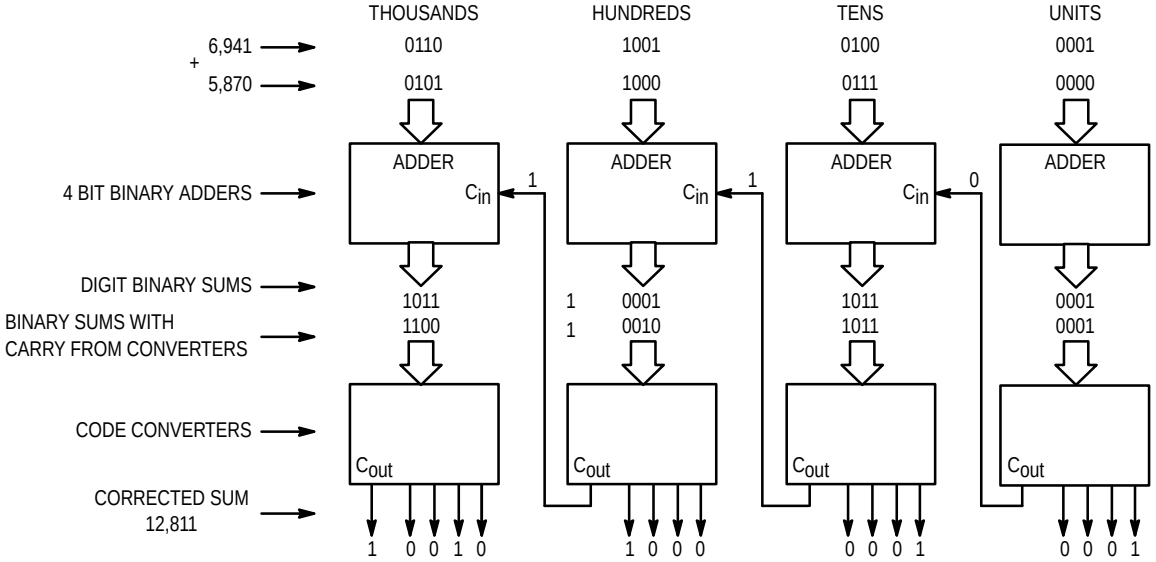
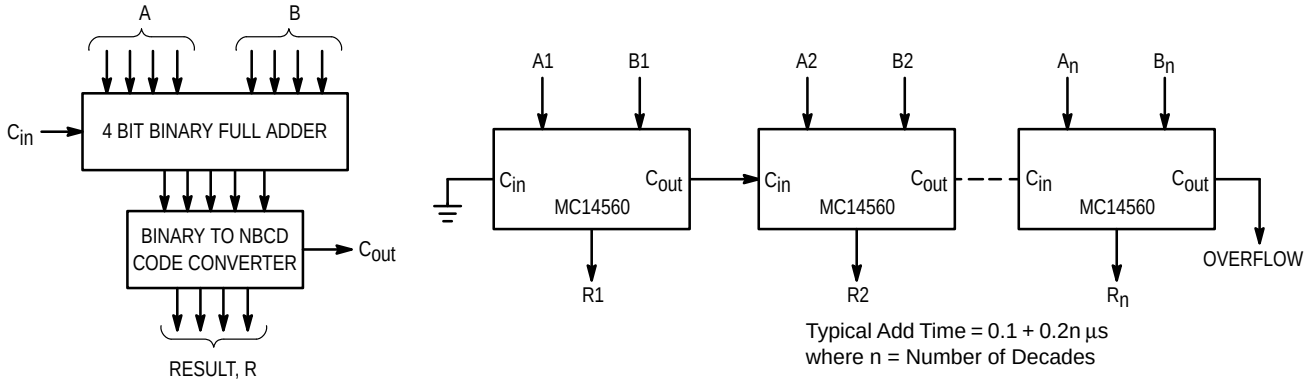


Figure 4. Unsigned NBCD Addition Algorithm



(a) MC14560 Block Diagram

(b) n–Decade Adder

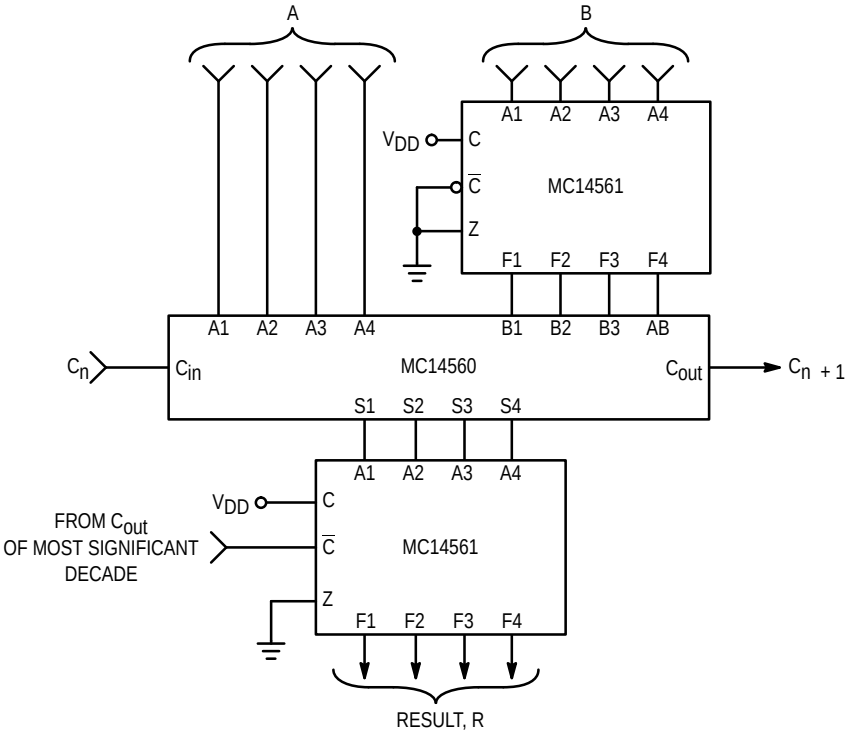
Figure 5. Addition of Unsigned NBCD Numbers

The truth table and Karnaugh maps for sign, overflow, and End Around Carry are shown in Figures 6 and 7. Note the use of B_S' from the exclusive–OR of Add/Sub and B_S. B_S' eliminates Add/Sub as a variable in the truth table. As an example of truth table generation, consider an n decade adder/subtracter where A_S = "0", B_S = "1", and Add/Sub = "0". B is in 9's complement form, $10^N - 1 - B$. Thus $A + (10^N - 1 - B) = 10^N - 1 + (A - B)$. There is no carry when $A \leq B$, and the sign is negative (sign = "1"). When A_S and B_S are opposite states and Add/Sub is a "0" (add mode), no overflow can occur (overflow = "0"). The other output states are determined in a similar manner (see Figure 6).

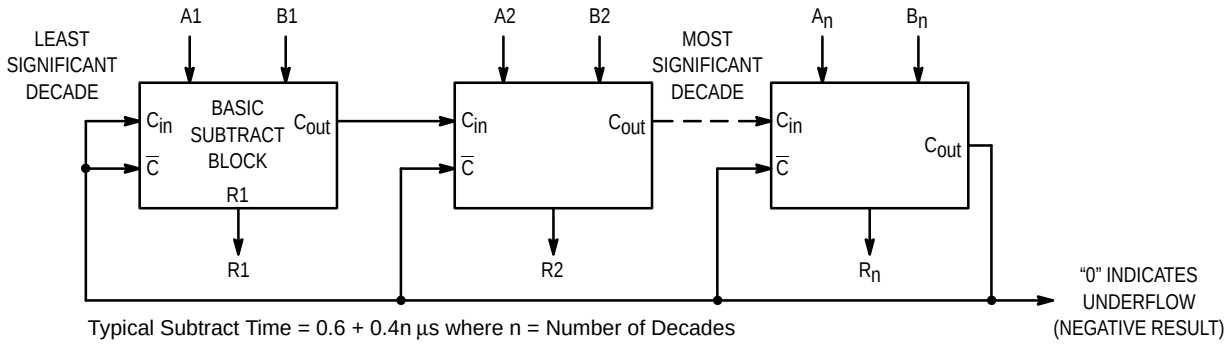
From the Karnaugh maps it is apparent that End Around Carry is composed of the two symmetrical functions S2 and S3 of three variables with $A_S\ B_S'\ C_{out}$ as the center of symmetry. This is the definition of the majority logic function $M_3(ABC)$. Similarly the Sign is composed of the symmetrical functions S2(3) and S3(3) but with the center of symmetry translated to $A_S B_S'\ C_{out}$. This is equivalent to the majority function $M_3(A_S B_S'\ \overline{C}_{out})$. Further evaluation of the maps and truth table reveal that Overflow can be generated by the exclusive–OR function of End Around Carry and Carry Out. This analysis results in a minimum device count consisting of one exclusive–OR package and one dual Majority Logic package to implement B_S', EAC, Sign and Overflow. The logic connections of these devices are shown in Figure 5.

The output sign, R_S, complements the result of the add/subtract operation when R_S = "1". This is required because the adder performs 9's complement arithmetic. Complementing, when R_S indicates the result is negative, restores sign and magnitude convention.

Several variations of the adder/subtracter are possible. For example, 9's complement is available at the output of the NBCD adders, and output complementers are eliminated if sign and magnitude output is not required.



(a) Basic Subtracter Block



(b) n–Decade Subtracter

Figure 6. Subtraction of Unsigned NBCD Numbers

SUMMARY

The concepts of binary code representations for decimal numbers, addition, and complement subtraction were discussed in detail. Using the basic Adder and Complementer MSI blocks, adder/subtracters for both signed and unsigned numbers were illustrated with examples.

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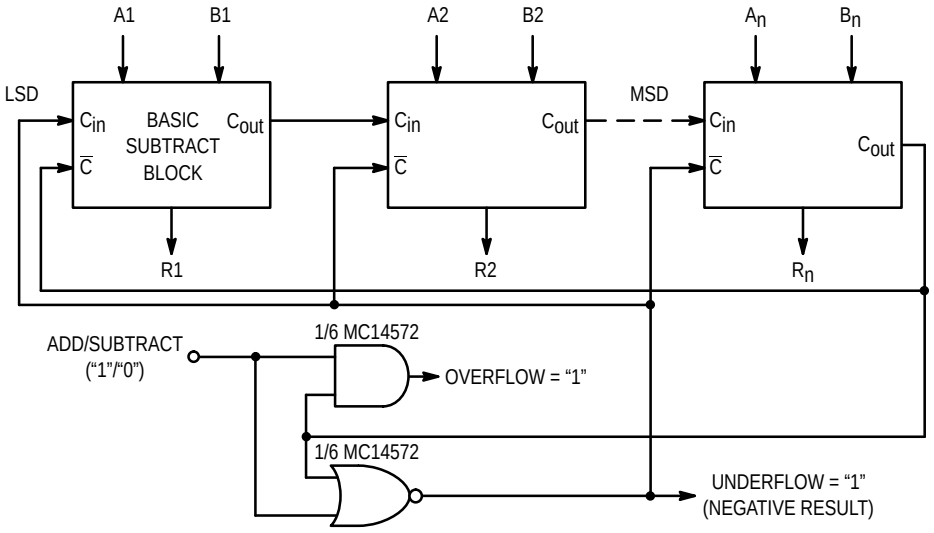


Figure 7. Adder/Subtracter for Unsigned NBCD Numbers

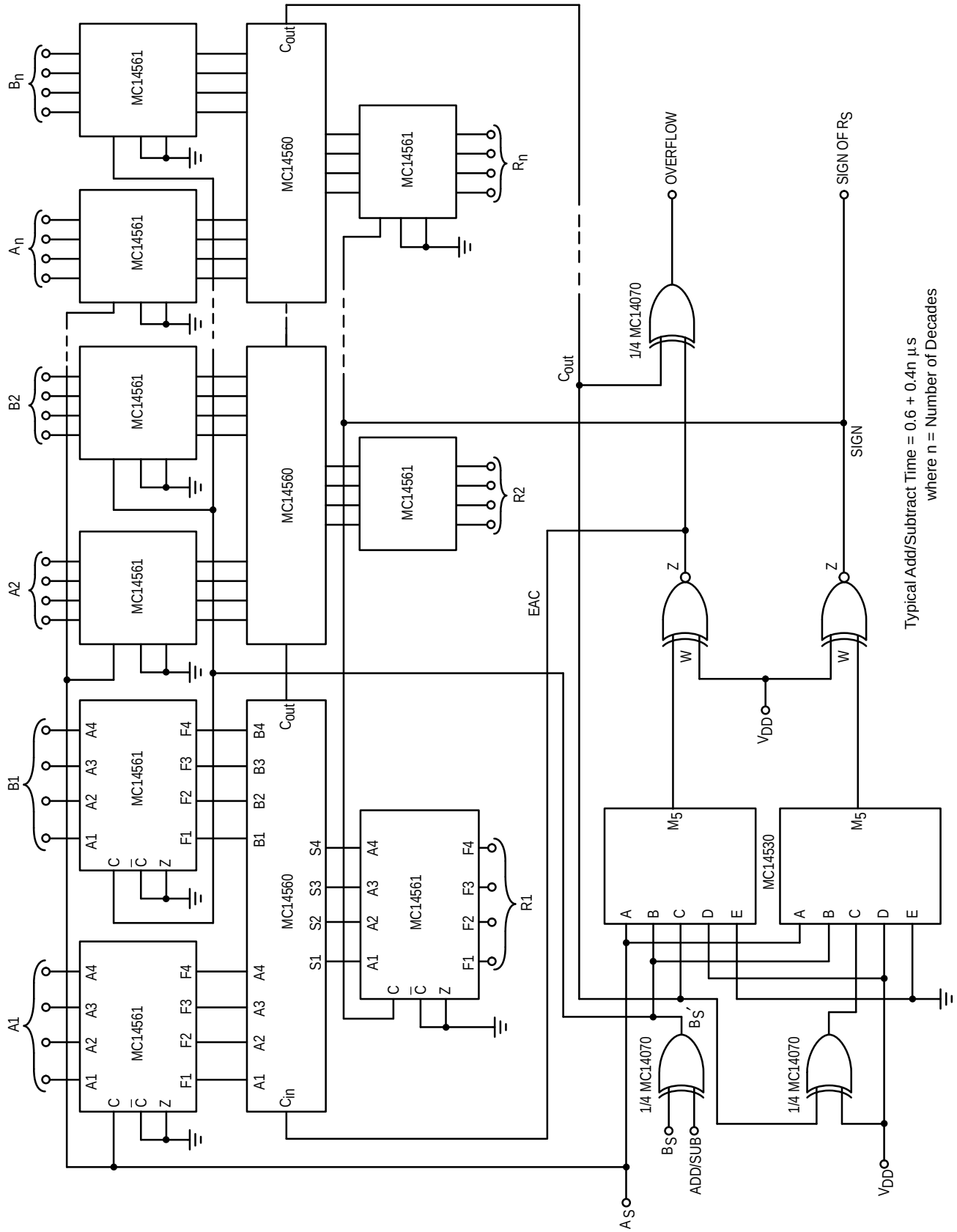


Figure 8. Sign and Magnitude Adder/Subtracter with Overflow

Inputs			Arithmatic Expression for R* (Result) (N = Number of Digits, 10^N = Modulus A, B, R are Positive Magnitudes)	Outputs		
A_S "1" = Neg	$B_{S'}$ "1" = Neg	C_{out} "1" = Carry		End Around Carry (EAC) "1" = EAC	Sign of R "1" = Negative	Overflow "1" = Overflow
0	0	0	R = A + 8	No EAC ("0") because R is correct result.	Since A and B are positive signed, R is positive signed ("0").	When C_{out} = "0", there is no carry ($R < 10^N$) and thus no overflow ("0").
0	0	1				When C_{out} = "1", there is a carry ($R \geq 10^N$) and thus overflow ("1").
0	1	0	R = A – B = A + (10^N – 1 – B) = A – B + 10^N – 1	No EAC ("0") because 9's complement expression for R is correct result.	A $\leq$ B when C_{out} = "0"; thus sign of R must be negative ("1").	There is never an overflow when numbers of opposite sign are added.
0	1	1		EAC = "1" because expression for R is in error by 1.	A > B when C_{out} = "1"; thus sign of R must be positive ("0").	
1	0	0	R = B – A = B + (10^N – 1 – A) = B – A + 10^N – 1	No EAC ("0") because 9's complement expression for R is correct result.	B $\leq$ A when C_{out} = "0"; thus sign of R must be negative ("1").	
1	0	1		EAC = "1" because expression for R is in error by 1.	B > A when C_{out} = "1"; thus sign of R must be positive ("0").	
1	1	0	R = – A – B = (10^N – 1 – A) + (10^N – 1 – B) = – (A + B) + 2 x 10^N – 2	EAC = "1" because 9's complement expression for R is in error by 1.	Since A and B are negative signed. R is negative signed ("1").	When C_{out} = "0", there is no Carry ($R < 0^N$) and (A + B) > 10^N – 1 indicating overflow ("1").
1	1	1				When C_{out} = "1", there is a carry ($R \geq 10^N$) and (A + B) $\leq$ 10^N – 1 indicating no overflow ("0").

* Output of Adders

Figure 9. Truth Table Generation for EAC, Sign, and Overflow Logic

TRUTH TABLE

Inputs			Outputs		
A_S	B_S'	C_{out}	EAC	SGN	OVF
0	0	0	0	0	0
0	1	0	0	1	0
1	0	0	0	1	0
1	1	0	1	1	1
0	0	1	0	0	1
0	1	1	1	0	0
1	0	1	1	0	0
1	1	1	1	1	0

B_S = (Add/Sub) $\oplus$ B_S
A_S = Sign of A (“1” = Negative)
B_S = Sign of B (“1” = Negative)
C_{out} = Adder Carry Out

KARNAUGH MAPS

End Around Carry

C_{out} \ A_S	0	1
0	0	1
1	1	1
B_S' 0	0	1
0*	0	0

Sign (SGN)

C_{out} \ A_S	0	1
0	1	1
1	0	1
B_S' 0	0*	0
0	0	1

Overflow (OVF)

C_{out} \ A_S	0	1
0	0	1
0	0	0
B_S' 1	0	0
0	0	0

* = Center of Symmetry

EAC = S2 ($A_S B_S' C_{out}$) + S3 ($A_S B_S' C_{out}$)
= M_3 ($A_S B_S' C_{out}$)

SGN = S2 ($A_S B_S' \overline{C}_{out}$) + S3 ($A_S B_S' C_{out}$)
= M_3 ($A_S B_S' \overline{C}_{out}$)

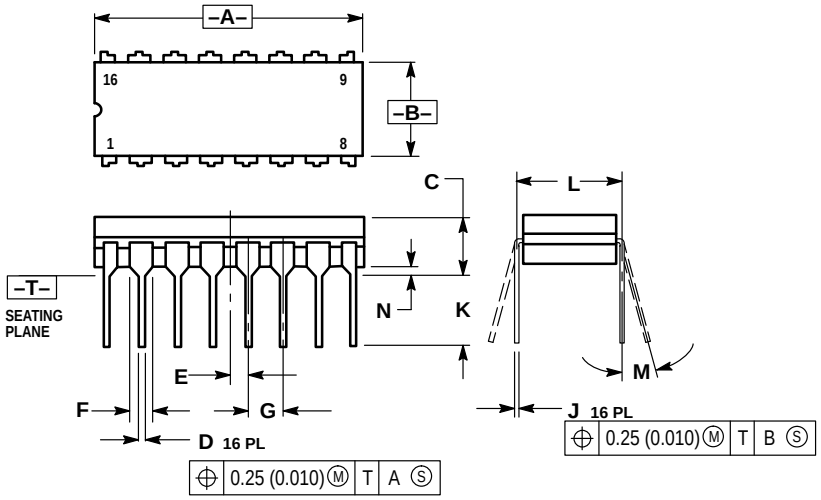
EAC $\oplus$ C_{out} = OVF

EAC		C_{out}		OVF
0	1	0	0	0 1
1	1	1	1	0 0
0	1	1	1	1 0
0	0	0	0	0 0

Figure 10. Mapping of EAC, Sign and Overflow Logic

OUTLINE DIMENSIONS

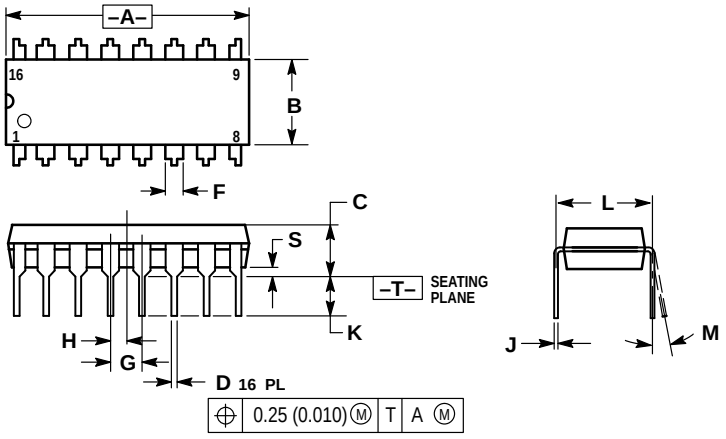
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

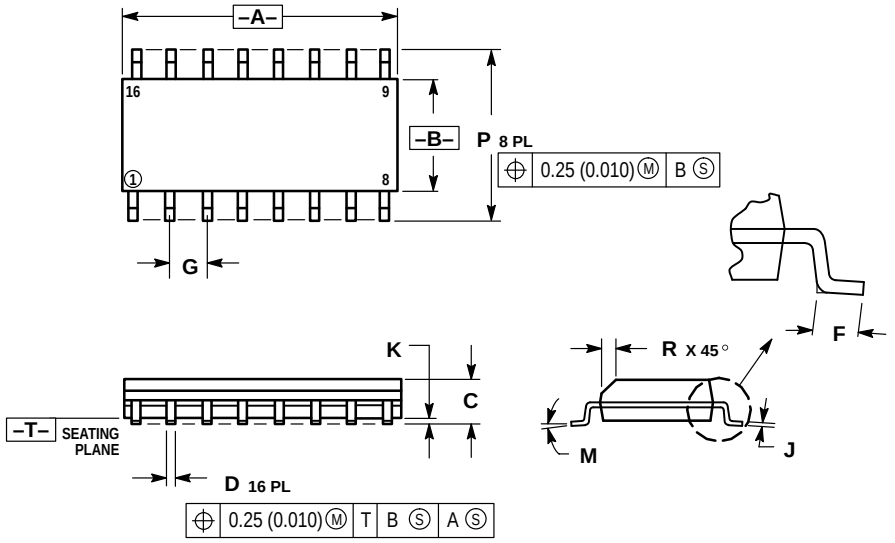


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298