

Product Preview

Calling Line Identification (CLID) Receiver with Ring Detector

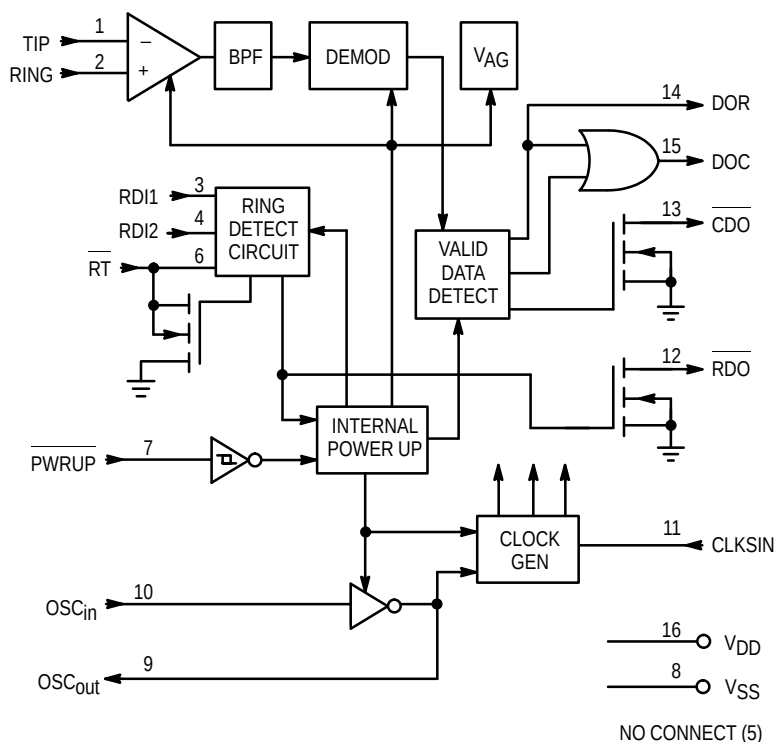
The MC14LC5447 is a silicon gate HCMOS IC designed to demodulate Bell 202 and V.23 1200-baud FSK asynchronous data. The primary application for this device is in products that will be used to receive and display the calling number, or message waiting indicator sent to subscribers from participating central office facilities of the public switched network. The device also contains a carrier detect circuit and ring detector which may be used to power up the device.

Applications for this device include adjunct boxes, answering machines, feature phones, fax machines, and computer interface products.

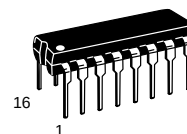
The MC14LC5447 offers the following performance features.

- Ring Detector On-Chip
- Ring Detect Output for MCU Interrupt
- Power-Down Mode, Less than 1 μ A
- Single Supply: + 3.5 to + 6.0 V
- Pin Selectable Clock Frequencies: 3.68 MHz, 3.58 MHz, or 455 kHz
- Two Stage Power-Up for Power Management Control
- Demodulates Bell 202 and V.23

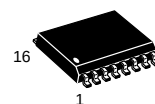
BLOCK DIAGRAM



MC14LC5447



P SUFFIX
PLASTIC DIP
CASE 648



DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

MC14LC5447P Plastic DIP
MC14LC5447DW SOG Package

PIN ASSIGNMENT

TI	1	16	V _{DD}
RI	2	15	DOC
RD1	3	14	DOR
RD2	4	13	CDO
NC	5	12	RDO
RT	6	11	CLKSIN
PWRUP	7	10	OSC _{in}
VSS	8	9	OSC _{out}

NC = NO CONNECTION

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 0
7/96

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND, except where noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 6.0	V
Input Voltage, All Pins	V_{in}	– 0.5 to $V_{DD} + 0.5$	V
DC Current Drain Per Pin	I	± 10	mA
Power Dissipation	P_D	20	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 40 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

(All polarities referenced to $V_{SS} = 0$ V, $V_{DD} = +5$ V ± 10%, unless otherwise noted, $T_A = 0$ to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	3.5	5	6	V
Supply Current (All Output Pins Unloaded) (See Figure 1) RT = 0, PWRUP = 1, XTAL = 3.58 MHz	I_{DD}	—	2.4	3	mA
Supply Current (All Output Pins Unloaded) (See Figure 1) PWRUP = 0, RT = Don't Care, XTAL = 3.58 MHz	I_{DD}	—	4.0	5.5	mA
Standby Current (All Output Pins Unloaded) (See Figure 1) RT = 1, PWRUP = 1	I_{STBY}	—	—	1	μA
Input Voltage 0 Level (CLKSIN, OSC _{in})	V_{IL}	—	—	$V_{DD} \times 0.3$	V
Input Voltage 1 Level (CLKSIN, OSC _{in})	V_{IH}	$V_{DD} \times 0.7$	—	—	V
Output Voltage High: $V_{DD} = 5$ V (DOR, DOC, OSC _{out}) $I_{OH} = 40$ μA $I_{OH} \leq 1$ μA	V_{OH}	2.4 4.95	—	—	V
Output Voltage Low: $V_{DD} = 5$ V (DOR, DOC, OSC _{out}) $I_{OL} = 1.6$ mA $I_{OL} \leq 1$ μA	V_{OL}	—	—	0.4 0.05	V
Input Leakage Current (OSC _{in} , CLKSIN, PWRUP, RT, RDI1, and RDI2)	I_{in}	—	—	±1	μA
Output Voltage Low: $V_{DD} = 5$ V (RDO, RT, CDO) $I_{OL} = 2.0$ mA	V_{OL}	—	—	0.4	V
Input Threshold Voltage Positive Going: $V_{DD} = 5$ V (RDI1, RT, PWRUP) (See Figure 3)	V_{T+}	2.5	2.75	3.0	V
Input Threshold Voltage Negative Going: $V_{DD} = 5$ V (RDI1, RT, PWRUP) (See Figure 3)	V_{T-}	2.0	2.3	2.6	V
RDI2 Threshold	$R_{D2}V_T$	1.0	1.1	1.2	V
TIP/RING Input dc Resistance	R_{in}	—	250	—	kΩ

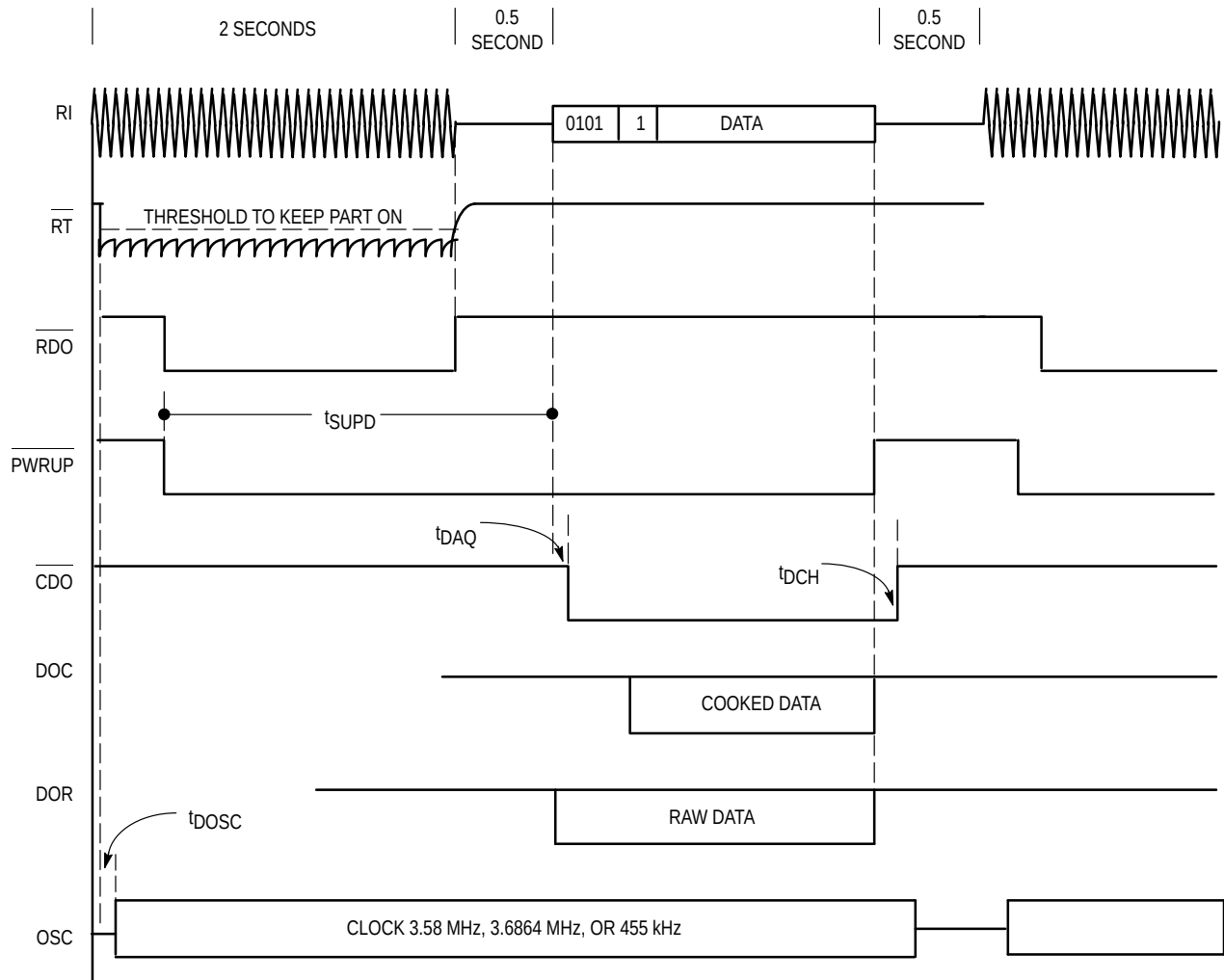
ANALOG CHARACTERISTICS ($V_{DD} = +5$ V, $T_A = +25$ °C, unless otherwise noted, 0 dBm = 0.7746 Vrms @ 600 Ω)

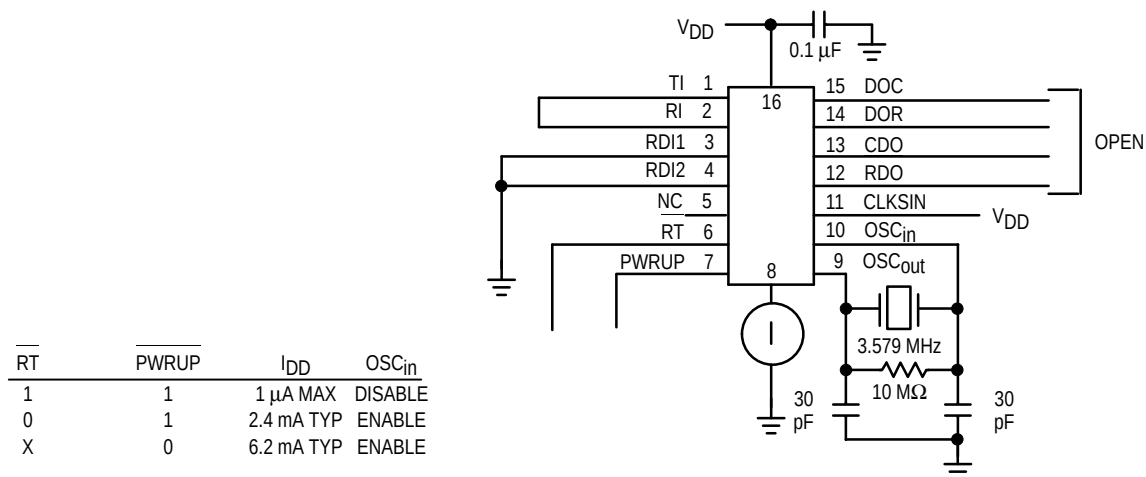
Characteristic	Min	Typ	Max	Unit
Input Sensitivity: TIP and RING (Pins 1 and 2, $V_{DD} = +5$ V)	– 40	– 45	—	dBm
Band-Pass Filter (BPF) Frequency Response (Relative to 1700 Hz @ 0 dBm)				dB
60 Hz	—	– 64	—	
500 Hz	—	– 4	—	
2700 Hz	—	– 3	—	
≥ 3300 Hz	—	– 34	—	
Carrier Detect Sensitivity	—	– 48	—	dBm

SWITCHING CHARACTERISTICS ($V_{DD} = +5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = +25^\circ\text{C}$)

Description	Symbol	Min	Typ	Max	Unit
OSC Startup (CLKSIN = 1; 3.579 MHz XTAL)	t_{DOSC}	—	2	—	ms
Power-Up Low to FSK (Setup Time)	t_{SUPD}	15	—	—	ms
Carrier Detect Acquisition Time	t_{DAQ}	—	14	—	ms
End of Data to Carrier Detect High	t_{DCH}	8	—	—	ms

TIMING DIAGRAM





DOR

Data Out Raw (Pin 14)

This pin presents the output of the demodulator whenever CDO is low. This data stream includes the alternate 1 and 0 pattern, and the 150 ms of marking, which precedes the data. At all other times, DOR is held high.

DOC

Data Out Cooked (Pin 15)

This output presents the output of the demodulator whenever CDO is low, and when an internal validation sequence has been successfully passed. The output does not include the alternate 1 and 0 pattern. At all other times, DOC is held high.

VDD

Positive Power Supply (Pin 16)

The digital supply pin, which is connected to the positive side of the power supply.

APPLICATIONS INFORMATION

The MC14LC5447 has been designed to be one of the main functional blocks in products targeted for the CLASS (Custom Local Area Signaling Service) market. CLASS is a set of subscriber features now being presented to the consumer by the RBOCs (Regional Bell Operating Companies) and independent TELCOs. Among CLASS features, such as distinctive ringing and selective call forwarding, the subscriber will also have available a service known as Calling Number Delivery (CND) and message waiting. With these services, a subscriber will have the ability to display at a minimum, a message containing the phone number of the calling party, the date, and the time. A message containing only this information is known as a single format message, as shown in Figure 9. An extended message, known as multiple format message, can contain additional information as shown in Figure 10.

The interface should be arranged to allow simplex data transmission from the terminating central office, to the CPE (Customer Premises Equipment), only when the CPE is in an on-hook state. The data will be transmitted in the silent period between the first and second power ring after a voice path has been established.

The data signaling interface should conform to Bell 202, which is described as follows:

- Analog, phase coherent, frequency shift keying
- Logical 1 (Mark) = 1200 ± 12 Hz
- Logical 0 (Space) = 2200 ± 22 Hz
- Transmission rate = 1200 bps
- Application of data = serial, binary, asynchronous

The transmission level from the terminating C.O. will be $-13.5 \text{ dBm} \pm 1.0$. The expected worst case attenuation through the loop is expected to be -20 dB . The receiver therefore, should have a sensitivity of approximately -34.5 dBm to handle the worst case installations.

Additional information on CLASS services can be obtained from:

BELLCORE CUSTOMER SVS.

1-800-521-2673

201-699-5800 FOREIGN CALLS

201-699-0936 FAX

The document number is: TA-NWT-000030

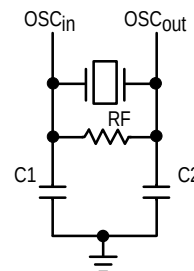
Title: "Voice Band Data Transmission Interface Generic Requirements"

Figure 7 is a conceptual design of how the MC14LC5447 can be implemented into a product which will retrieve the incoming message and convert it to EIA-232 levels for transmission to the serial port of a PC. With this message and appropriate software, the PC can be used to look up the name and any additional information associated with the caller that had been previously stored.

Figure 8 is a conceptual design of an adjunct unit in parallel with an existing phone. This arrangement gives the subscriber CND service without having to replace existing equipment.

Table 1. Oscillator Specifications

Clock Select Pin 11 = 1	
Crystal Mode	Parallel
Frequency	3.579 MHz or 3.6864 MHz
R_f	10 M Ω
C1 and C2	30 pF
Source: Fox Electronics 5570 Enterprise Pkwy. Ft. Myers, FL 33905 Tel. 813-693-0099	
Clock Select Pin 11 = 0	
Resonator	#CSB455J
Frequency	455 kHz $\pm 0.5\%$
R_f	1.0 M Ω
C1 and C2	100 pF
Source: Murata Manufacturing Co. Ltd. 2200 Lake Park Dr. Smyrna, GA 30080 Tel. 404-436-1300	
NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing.	



DESIGN INFORMATION

The circuit in Figure 2 illustrates in greater detail the relationship between Pins 3, 4, 6, and 7.

The external component values shown in Figure 2 are the same as those shown in Figures 7 and 8. When V_{DD} is applied to the circuit in these two figures, the RC network will charge cap C1 to V_{DD} holding RT (Pin 6) off. If the PWRUP (Pin 7) is also held at V_{DD} , the MC14LC5447 will be in a power-down mode, and will consume 1 μ A of supply current (max).

The resistor network (R2 – R4) attenuates the incoming power ring applied to the top of R2. The values given have been chosen to provide a sufficient voltage at RDI1 (Pin 3) to turn on the Schmitt-trigger input with approximately a 40 Vrms or greater power ring input from tip and ring. When V_{T+} of the Schmitt is exceeded, Q1 will be driven to saturation discharging cap C1 on RT. This will initialize a partial power-up, with only the portions of the part involved with the ring signal analysis enabled, including RDI2 (Pin 4). At this time the MC14LC5447 power consumption is increased to approximately 2.4 mA (typ).

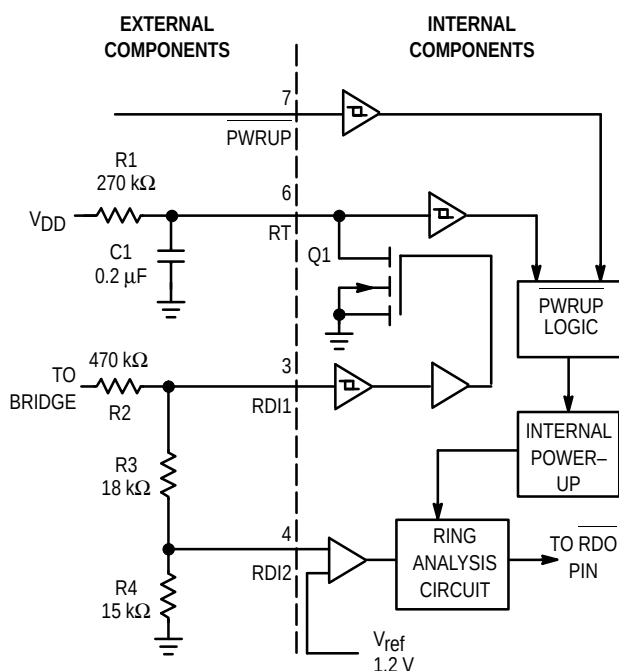


Figure 2.

The value of R1 and C1 must be chosen to hold the RT pin voltage below the V_{T+} of the RT Schmitt between the individual cycles of the power ring. The values shown will work for ring frequencies of 15.3 Hz (min).

With RDI2 now enabled, a portion of the power ring above 1.2 V is fed to the ring analysis circuit. This circuit is a digital integrator which looks at the duty cycle of the incoming signal. When the input to RDI2 is above 1.2 V, the integrator is counting up at an 800 Hz rate. When the input to RDI2 falls below 1.2 V, the integrator counts down at a 400 Hz rate.

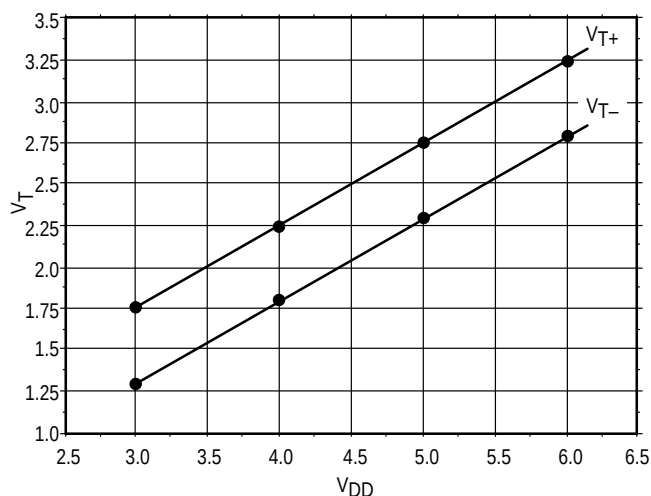


Figure 3. V_{DD} versus V_{T+} and V_{T-}

A ring is qualified when an internal count of binary 48 is reached. The ring is disqualified when the count drops to a binary 32. The number of ring cycles required to qualify the signal will depend on the amplitude of the voltage presented to RDI2. The shortest amount of time needed to do the qualification is approximately 60 ms. The shortest amount of time required for dequalification will be approximately 40 ms.

Once the ring signal is qualified, the RDO pin will be sent low. This can be fed back to PWRUP as shown in Figure 7, or with a pull-up resistor, can be used as an interrupt to an MCU as shown in Figure 8. In either case, once the PWRUP pin is below V_{T-} , the part will be fully powered up, and ready to receive FSK. During this mode, the device current will increase to approximately 6.2 mA (typ). The state of the RT pin is now a "don't care" as far as the part is concerned. Normally, however, this pin will be allowed to return to V_{DD} .

After the FSK message has been received, the PWRUP pin can be allowed to return to V_{DD} and the part will return to the standby mode, consuming less than 1 μ A of supply current. The part is now ready to repeat the same sequence for the next incoming message.

TYPICAL DEMODULATOR PERFORMANCE

The following describes the performance of the MC14LC5447 demodulator in the presence of noise over a simulated Bell 3002 telephone loop.

The Bell 3002 loop represents a worst case local telephone loop in North America. The characteristics of this loop, which affect performance, are high frequency attenuation and Envelope Delay Distortion (EDD) or group delay.

The minimum receiver sensitivity of the MC14LC5447 under these conditions is typically – 45 dBm.

The MC14LC5447 achieves a Bit Error Rate (BER) of 1×10^{-5} at a Signal-to-Noise Ratio (SNR) of 15 dB in V.23 operation and at an SNR of 18 dB in Bell 202 operation (see Figures 4 and 5).

All measurements in dBm are referenced to 600 Ω : 0 dBm = 0.7746 Vrms.

All measurements were taken using the MC145460EVK evaluation board.

Electronic file not available for this figure. To view the complete document, order it from the Literature Center.

Electronic file not available for this figure. To view the complete document, order it from the Literature Center.

**Figure 4. MC14LC5447 V.23 Operation
(Typical BER vs SNR)**

**Figure 5. MC14LC5447 Bell 202 Operation
(Typical BER vs SNR)**

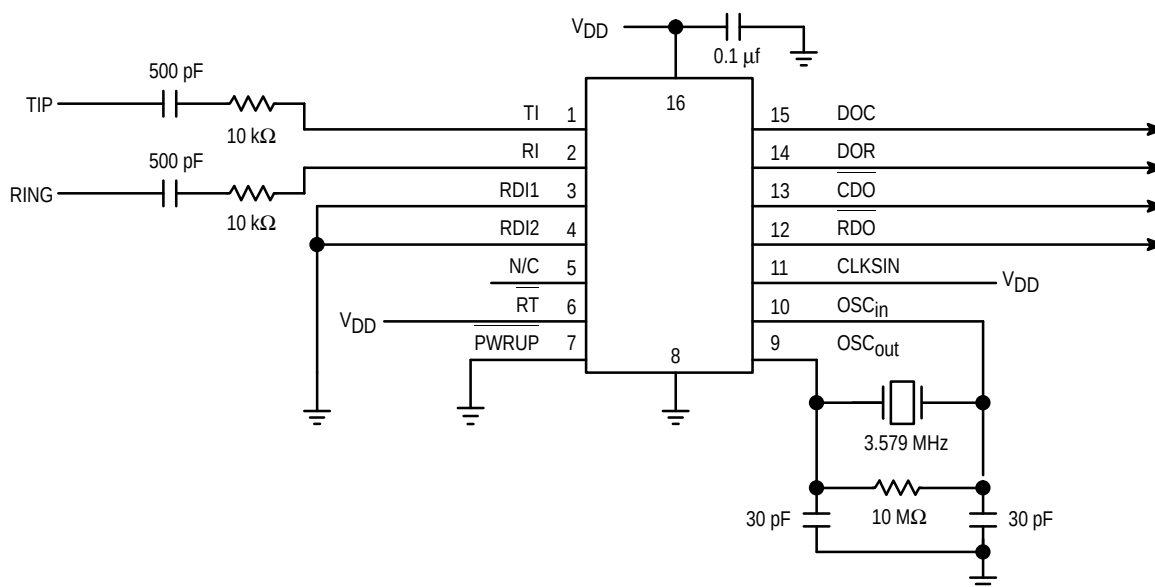


Figure 6. Full-Time Power without Ring Detect

APPLICATION CIRCUIT

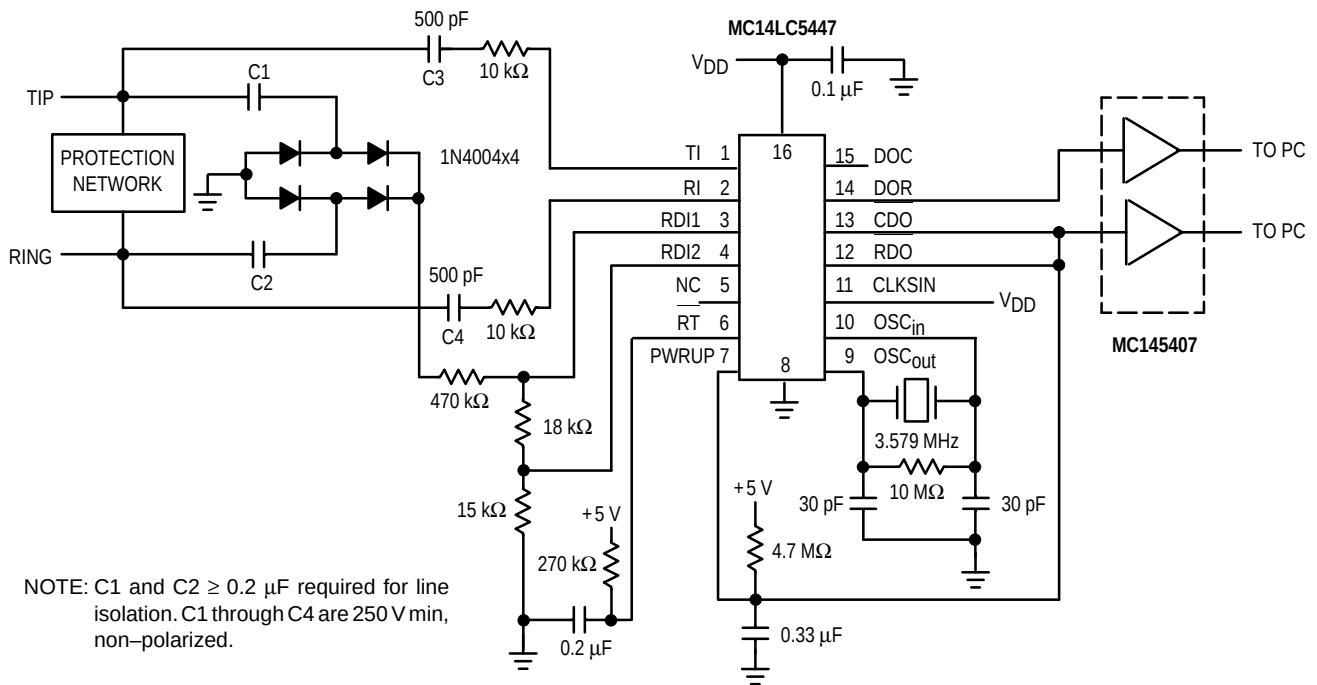
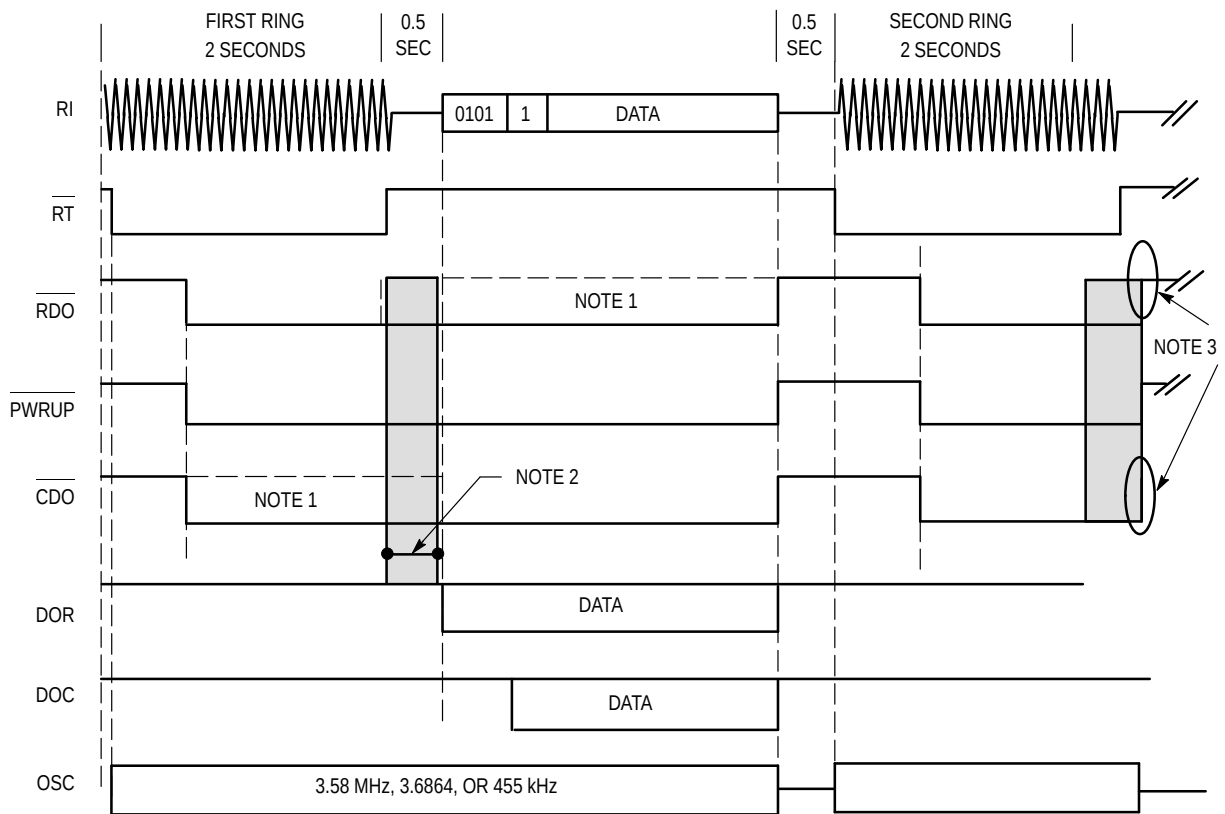


Figure 7. Partial Implementation of PC Interface to Tip and Ring



NOTES:

1. Wired 'OR' RDO with CDO.
2. Overlap of RDO edge with CDO edge to ensure part stays in PWRUP determined by RC time constant on RDO, PWRUP, and CDO pin.
3. Part reverts to PWR ON, on rising edge of RDO since there is no CDO.

Timing Diagram for Figure 7

APPLICATION CIRCUIT

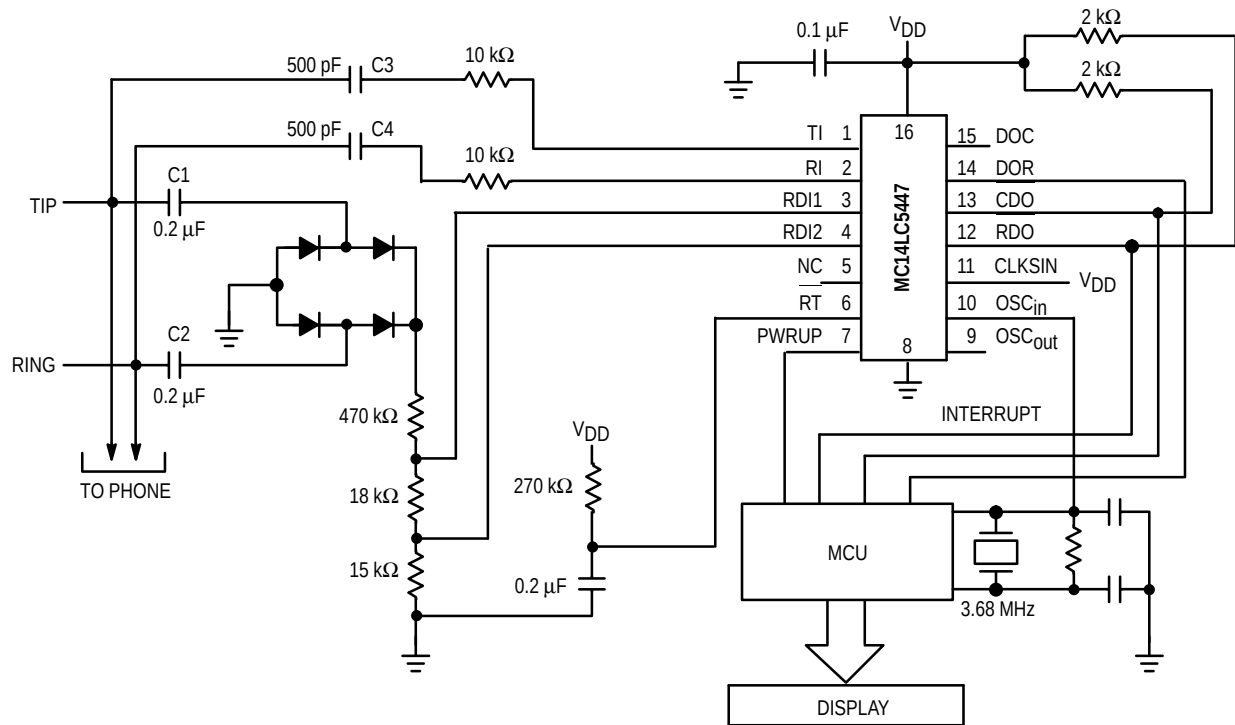
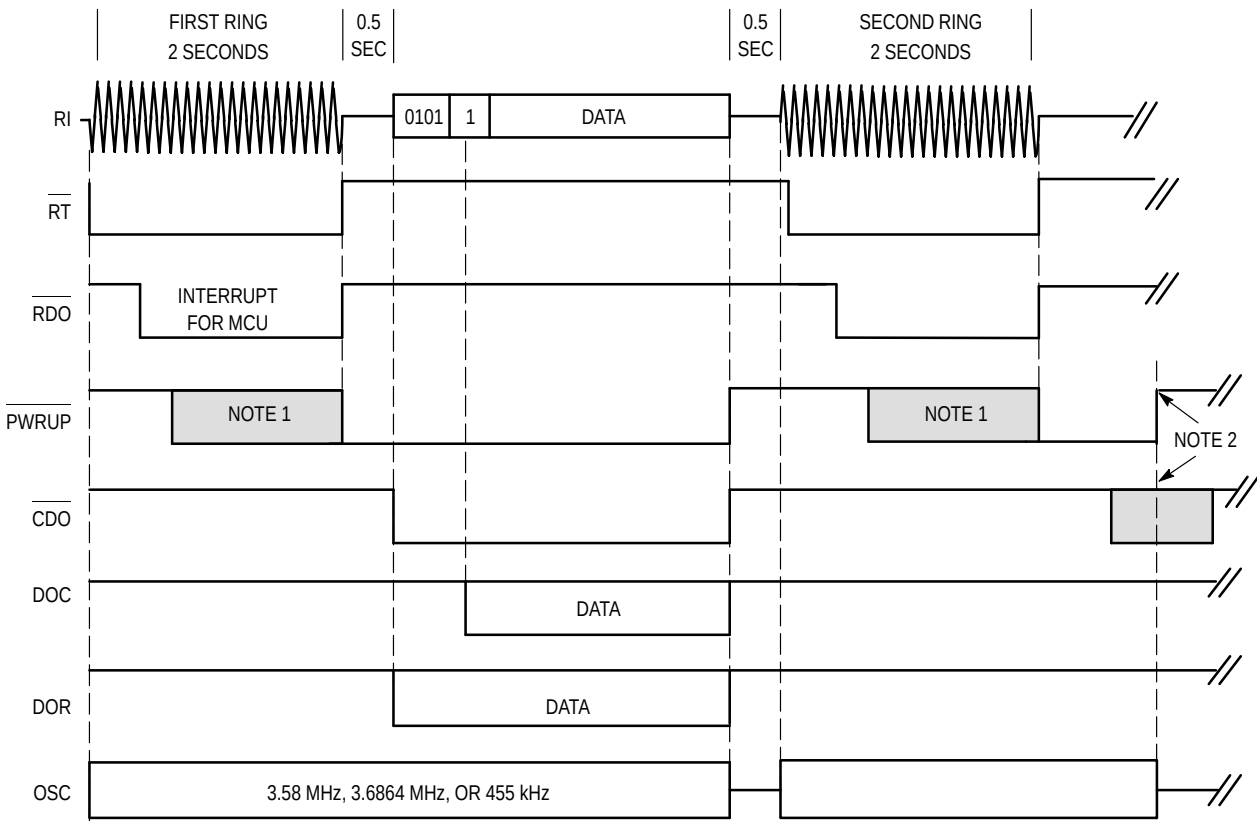


Figure 8. Adjunct Box Concept for Calling Number Display



NOTES:

1. MCU must assert PWRUP to MC14LC5447.
2. No data detected, MCU powers down the MC14LC5447.

Timing Diagram for Figure 8

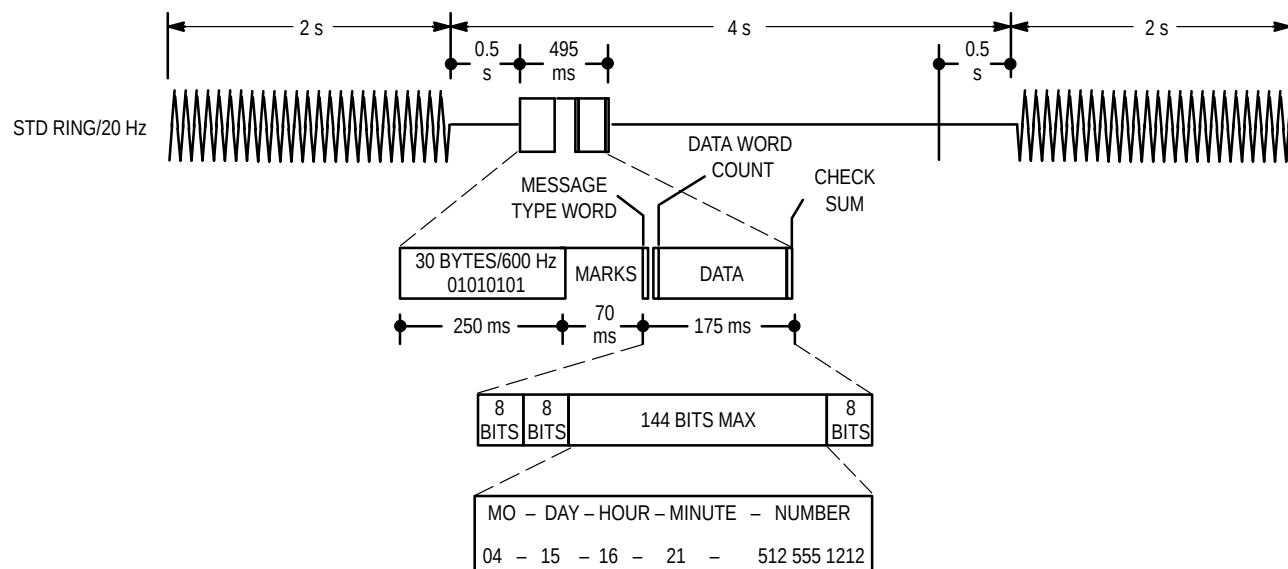


Figure 9. Single Message Format

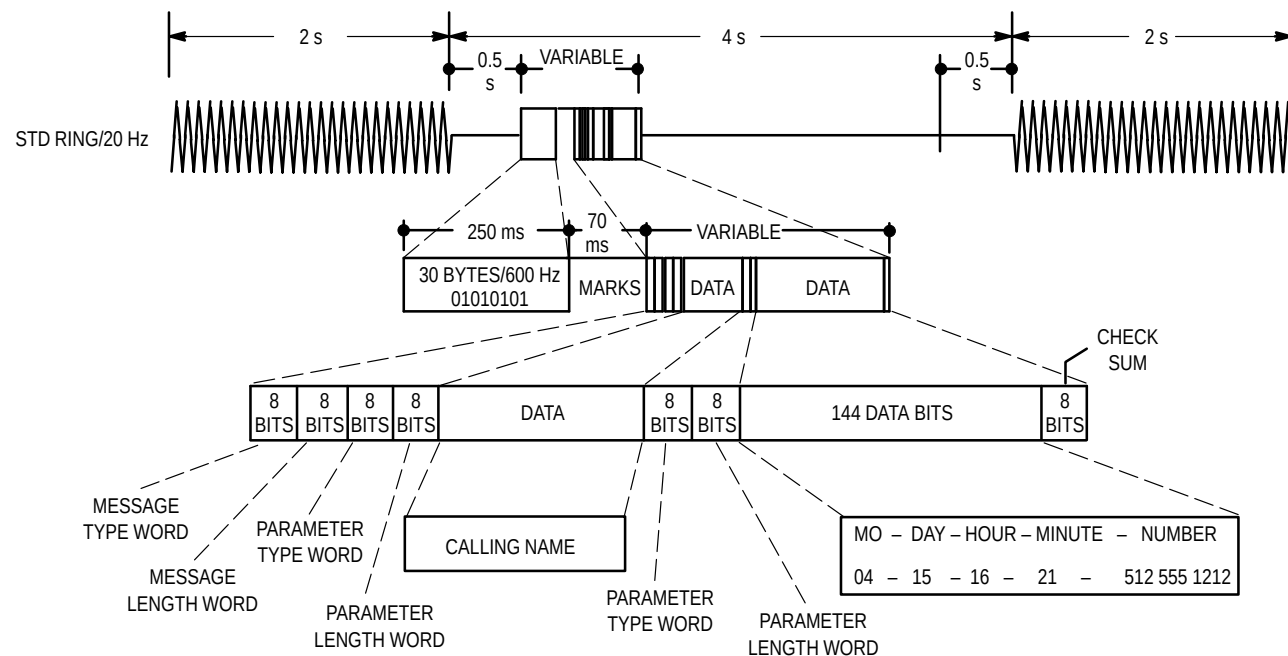
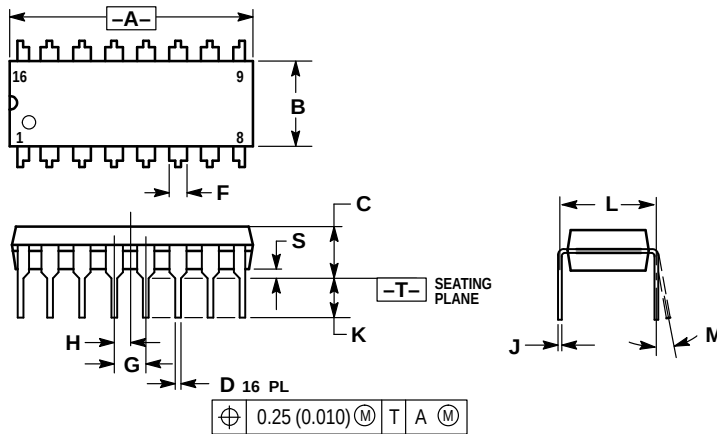


Figure 10. Multiple Message Format

PACKAGE DIMENSIONS

P SUFFIX PLASTIC DIP CASE 648-08

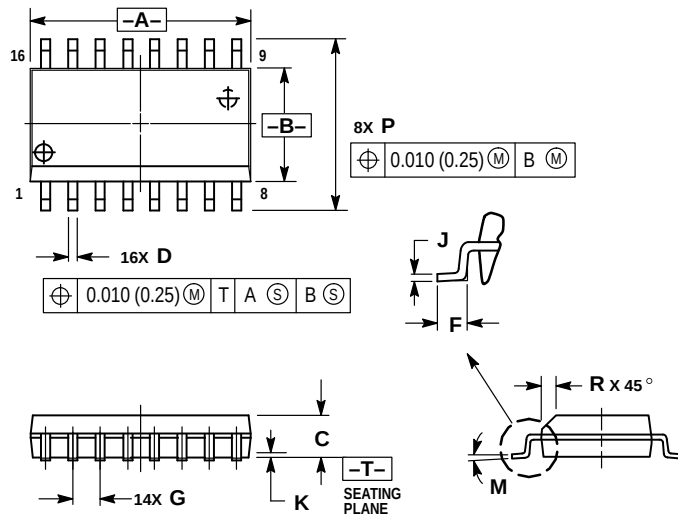


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

DW SUFFIX SOG PACKAGE CASE 751G-02



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
151 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



MC14LC5447/D

