

MC3437

HEX BUS RECEIVER WITH INPUT HYSTERESIS

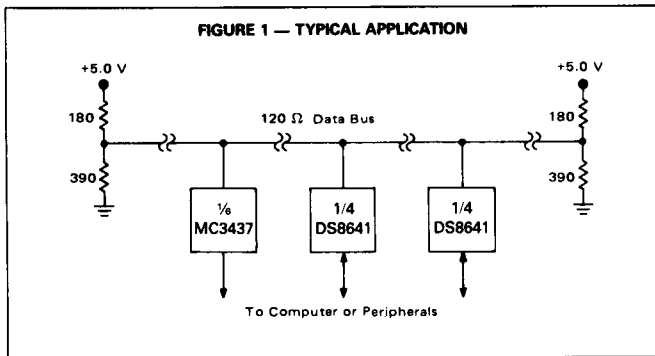
These high-speed bus receivers are useful in bus organized data transmission systems employing terminated 120 Ω lines. The receivers feature input hysteresis to obtain improved noise immunity. The receivers low input current requirement allows up to 27 driver/receiver pairs to share a common bus. A pair of Disable Inputs are provided. These Disable Inputs along with the receiver outputs are MTTL compatible.

- Built in receiver hysteresis
- Receiver input threshold is not affected by temperature
- Propagation delay time—20 ns (Typ)
- Direct Replacement for DM8837

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

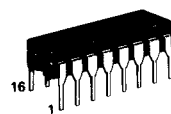
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation Derate above 25°C	P_D	625 3.85	mW mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to 70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

FIGURE 1 — TYPICAL APPLICATION

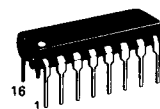


HEX BUS RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

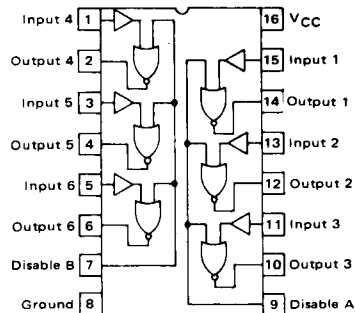


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



TRUTH TABLE

Input	Disable	Output
O	L	H
O	H	L
I	L	L
I	H	L

O = < 1.05 V
I = > 2.5 V
H = High Logic State
L = Low Logic State

MC3437

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $0 \leq T_A \leq 70^\circ\text{C}$ and $4.75 \text{ V} \leq V_{CC} \leq 5.25 \text{ V}$.)

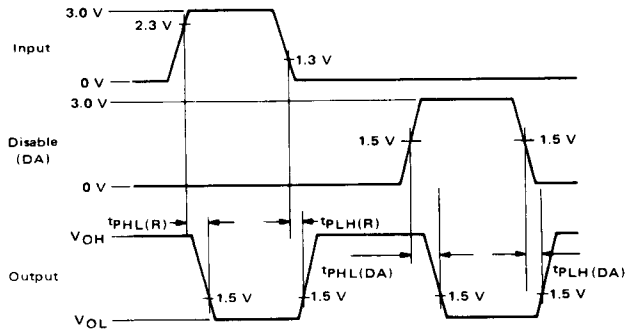
Characteristic	Symbol	Min	Typ	Max	Unit
Receiver Input Threshold Voltage – High Logic State ($V_{IL}(\text{DA}) = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$, $V_{OL} \leq 0.4 \text{ V}$)	$V_{ILH}(\text{R})$	1.80	2.25	2.50	V
Receiver Input Threshold Voltage – Low Logic State ($V_{IL}(\text{DA}) = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$, $V_{OH} \geq 2.4 \text{ V}$)	$V_{IHL}(\text{R})$	1.05	1.30	1.55	V
Receiver Input Current ($V_{I(\text{R})} = 4.0 \text{ V}$, $V_{CC} = 5.25 \text{ V}$) ($V_{I(\text{R})} = 4.0 \text{ V}$, $V_{CC} = 0 \text{ V}$)	$I_{I(\text{R})}$	— —	15 1.0	50 50	μA
Disable Input Voltage – High Logic State ($V_{I(\text{R})} = 0.5 \text{ V}$, $V_{OL} \leq 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$)	$V_{IH}(\text{DA})$	2.0	—	—	V
Disable Input Voltage – Low Logic State ($V_{I(\text{R})} = 0.5 \text{ V}$, $V_{OH} \geq 2.4 \text{ V}$, $I_{OH} = -400 \mu\text{A}$)	$V_{IL}(\text{DA})$	—	—	0.8	V
Output Voltage – High Logic State ($V_{I(\text{R})} = 0.5 \text{ V}$, $V_{IL}(\text{DA}) = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$)	V_{OH}	2.4	—	—	V
Output Voltage – Low Logic State ($V_{I(\text{R})} = 4.0 \text{ V}$, $V_{IL}(\text{DA}) = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$)	V_{OL}	—	0.25	0.4	V
Disable Input Current – High Logic State ($V_{IH}(\text{DA}) = 2.4 \text{ V}$) ($V_{IH}(\text{DA}) = 5.5 \text{ V}$)	$I_{IH}(\text{DA})$	— —	— —	80 2.0	μA mA
Disable Input Current – Low Logic State ($V_{I(\text{R})} = 4.0 \text{ V}$, $V_{IL}(\text{DA}) = 0.4 \text{ V}$)	$I_{IL}(\text{DA})$	—	—	-3.2	mA
Output Short Circuit Current ($V_{I(\text{R})} = 0.5 \text{ V}$, $V_{IL}(\text{DA}) = 0 \text{ V}$, $V_{CC} = 5.25 \text{ V}$)	I_{OS}	-18	—	-55	mA
Power Supply Current ($V_{I(\text{R})} = 0.5 \text{ V}$, $V_{IL}(\text{DA}) = 0 \text{ V}$)	I_{CC}	—	45	65	mA
Input Clamp Diode Voltage ($I_{I(\text{R})} = -12 \text{ mA}$, $I_{I(\text{DA})} = -12 \text{ mA}$)	V_I	—	-1.0	-1.5	V

SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Receiver Input to High Logic State Output	$t_{PLH}(\text{R})$	—	20	30	ns
Propagation Delay Time from Receiver Input to Low Logic State Output	$t_{PHL}(\text{R})$	—	18	30	ns
Propagation Delay Time from Disable Input to High Logic State Output	$t_{PLH}(\text{DA})$	—	9.0	15	ns
Propagation Delay Time from Disable Input to Low Logic State Output	$t_{PHL}(\text{DA})$	—	4.0	15	ns

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The diagram shows a test circuit for a diode. Two pulse generators provide input signals to a 1/6 MC3437 NAND gate. The output of the gate is connected to a 390 ohm resistor and the anode of the diode under test. The cathode of the diode is connected to a +5.0 V supply. A 15 pF capacitor is connected from the output node to ground. The circuit is designed to measure the forward voltage drop of the diode during the pulse. Waveform traces are provided for the input signals, the output of the gate, and the voltage across the diode.



The circuit diagram illustrates a 12-bit digital-to-analog converter (DAC) implemented using a current mirror array and a resistor ladder network. The circuit is powered by a VCC supply and Ground.

Input Stage: The Input signal is connected to the base of transistor Q1. Q1 is part of a current mirror array consisting of transistors Q1 through Q12. The emitters of Q1, Q2, Q3, and Q4 are connected to Ground. The emitters of Q5, Q6, Q7, and Q8 are connected to a common node that is biased by a current source (Q9, Q10) and a resistor network (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13).

Current Mirror Array: The current mirror array consists of transistors Q1 through Q12. The bases of Q1, Q2, Q3, and Q4 are connected to the Input. The bases of Q5, Q6, Q7, and Q8 are connected to a common node that is biased by a current source (Q9, Q10) and a resistor network (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13). The emitters of Q1, Q2, Q3, and Q4 are connected to Ground. The emitters of Q5, Q6, Q7, and Q8 are connected to a common node that is biased by a current source (Q9, Q10) and a resistor network (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13).

Resistor Ladder Network: The resistor ladder network consists of resistors R1 through R13. R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, and R13 are connected in a ladder configuration between VCC and Ground. The resistors are labeled R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, and R13.

Output Stage: The Output signal is taken from the collector of transistor Q13. The collector of Q13 is connected to VCC through resistor R13. The emitter of Q13 is connected to a common node that is biased by a current source (Q9, Q10) and a resistor network (R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13). The collector of Q12 is connected to Ground through resistor R11. The collector of Q11 is connected to Ground through resistor R12. The collector of Q10 is connected to Ground through resistor R10. The collector of Q9 is connected to Ground through resistor R9.

Diodes: Diodes D1, D2, D3, and D4 are connected in series with the input and output signals. D1 is connected between the Input and the base of Q1. D2 is connected between the base of Q4 and the base of Q8. D3 is connected between the collector of Q13 and the Output. D4 is connected between the Output and Ground.