

Advance Information

128K x 36 and 256K x 18 Bit Flow-Through ZBT™ RAM Synchronous Fast Static RAM

The ZBT RAM is a 4M-bit synchronous fast static RAM designed to provide zero bus turnaround. The ZBT RAM allows 100% use of bus cycles during back-to-back read/write and write/read cycles. The MCM63Z737 is organized as 128K words of 36 bits each and the MCM63Z819 is organized as 256K words of 18 bits each, fabricated with high performance silicon gate CMOS technology. This device integrates input registers, a 2-bit address counter, and high speed SRAM onto a single monolithic circuit for reduced parts count in communication applications. Synchronous design allows precise cycle control with the use of an external clock (CK). CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

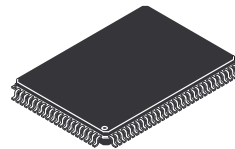
Addresses (SA), data inputs (DQ), and all control signals except output enable (G) and linear burst order (LBO) are clock (CK) controlled through positive-edge-triggered noninverting registers.

Write cycles are internally self-timed and are initiated by the rising edge of the clock (CK) input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

For read cycles, a flow-through SRAM allows output data to simply flow freely from the memory array.

- 3.3 V LVTTTL and LVCMOS Compatible
- MCM63Z737/MCM63Z819-11 = 11 ns Access/15 ns Cycle (66 MHz)
MCM63Z737/MCM63Z819-15 = 15 ns Access/20 ns Cycle (50 MHz)
- Selectable Burst Sequencing Order (Linear/Interleaved)
- Internally Self-Timed Write Cycle
- Single-Cycle Deselect
- Byte Write Control
- ADV Controlled Burst
- 100-Pin TQFP Package

**MCM63Z737
MCM63Z819**



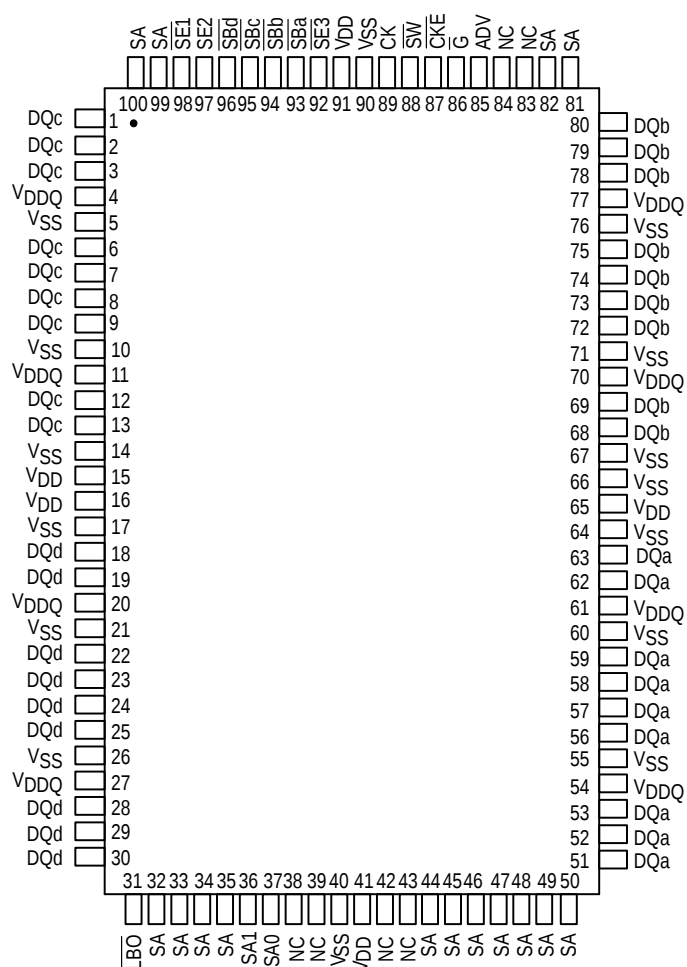
**TQ PACKAGE
TQFP
CASE 983A-01**

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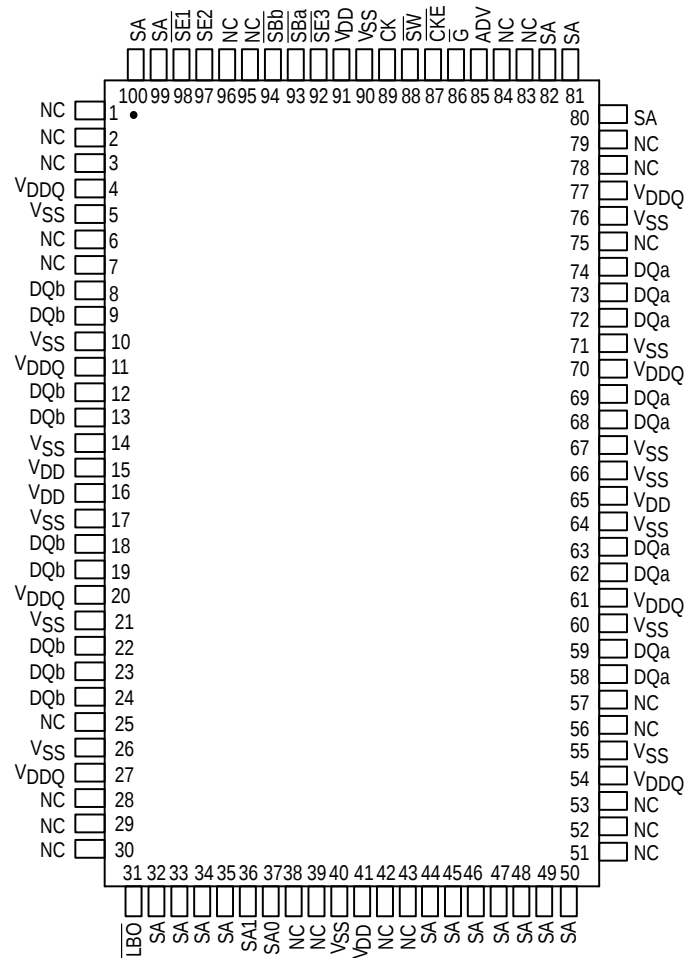
This document contains information on a new product. Specifications and information herein are subject to change without notice.



TOP VIEW
MCM63Z737



PIN ASSIGNMENT



TOP VIEW
MCM63Z819

MCM63Z737 PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	ADV	Input	Synchronous Load/Advance: Loads a new address into counter when low. RAM uses internally generated burst addresses when high.
89	CK	Input	Clock: <u>This signal</u> registers the address, data in, and all control signals except G and LBO.
87	CKE	Input	Clock Enable: Disables the CK input when CKE is high.
(a) 51, 52, 53, 56, 57, 58, 59, 62, 63 (b) 68, 69, 72, 73, 74, 75, 78, 79, 80 (c) 1, 2, 3, 6, 7, 8, 9, 12, 13 (d) 18, 19, 22, 23, 24, 25, 28, 29, 30	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b, c, d).
86	G	Input	Asynchronous Output Enable.
31	LBO	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low – linear burst counter. High – interleaved burst counter.
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA0, SA1	Input	Synchronous Burst Address Inputs: The two LSB's of the address field. These pins must preset the burst address counter values. These inputs are registered and must meet setup and hold times.
93, 94, 95, 96 (a) (b) (c) (d)	SBx	Input	Synchronous Byte Write Inputs: <u>Enables</u> write to byte "x" (byte a, b, c, d) in conjunction with SW. Has no effect on read cycles.
98	SE1	Input	Synchronous Chip Enable: Active low to enable chip.
97	SE2	Input	Synchronous Chip Enable: Active high for depth expansion.
92	SE3	Input	Synchronous Chip Enable: Active low for depth expansion.
88	SW	Input	Synchronous Write: This signal <u>writes</u> only those bytes that have been selected using the byte write SBx pins.
15, 16, 41, 65, 91	V _{DD}	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	V _{DDQ}	Supply	I/O Power Supply.
5, 10, 14, 17, 21, 26, 40, 55, 60, 64, 66, 67, 71, 76, 90	V _{SS}	Supply	Ground.
38, 39, 42, 43, 83, 84	NC	—	No Connection: There is no connection to the chip.

MCM63Z819 PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
85	ADV	Input	Synchronous Load/Advance: Loads a new address into counter when low. RAM uses internally generated burst addresses when high.
89	CK	Input	Clock: <u>This signal</u> registers the address, data in, and all control signals except G and LBO.
87	CKE	Input	Clock Enable: Disables the CK input when CKE is high.
(a) 58, 59, 62, 63, 68, 69, 72, 73, 74 (b) 8, 9, 12, 13, 18, 19, 22, 23, 24	DQx	I/O	Synchronous Data I/O: "x" refers to the byte being read or written (byte a, b).
86	G	Input	Asynchronous Output Enable.
31	LBO	Input	Linear Burst Order Input: This pin must remain in steady state (this signal not registered or latched). It must be tied high or low. Low – linear burst counter. High – interleaved burst counter.
32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 80, 81, 82, 99, 100	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
36, 37	SA0, SA1	Input	Synchronous Burst Address Inputs: The two LSB's of the address field. These pins must preset the burst address counter values. These inputs are registered and must meet setup and hold times.
93, 94 (a) (b)	SBx	Input	Synchronous Byte Write Inputs: Enables write to byte "x" (byte a, b) in conjunction with SW. Has no effect on read cycles.
98	SE1	Input	Synchronous Chip Enable: Active low to enable chip.
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92	SE3	Input	Synchronous Chip Enable: Active low for depth expansion.
88	SW	Input	Synchronous Write: This signal writes only those bytes that have been selected using the byte write SBx pins.
15, 16, 41, 65, 91	V _{DD}	Supply	Core Power Supply.
4, 11, 20, 27, 54, 61, 70, 77	V _{DDQ}	Supply	I/O Power Supply.
5, 10, 14, 17, 21, 26, 40, 55, 60, 64, 66, 67, 71, 76, 90	V _{SS}	Supply	Ground.
1, 2, 3, 6, 7, 25, 28, 29, 30, 38, 39, 42, 43, 51, 52, 53, 56, 57, 75, 78, 79, 83, 84, 95, 96	NC	—	No Connection: There is no connection to the chip.

TRUTH TABLE

CK	$\overline{\text{CKE}}$	E	$\overline{\text{SW}}$	$\overline{\text{SBx}}$	ADV	SA0 – SAx	Next Operation	Input Command Code	Notes
L–H	1	X	X	X	X	X	Hold	H	1, 2
L–H	0	False	X	X	0	X	Deselect	D	1, 2
L–H	0	True	0	V	0	V	Load Address, New Write	W	1, 2, 3, 4, 5
L–H	0	True	1	X	0	V	Load Address, New Read	R	1, 2
L–H	0	X	X	V (W)	1	X	Burst	B	1, 2, 4, 6, 7
				X (R, D)			Continue		

NOTES:

1. X = don't care, 1 = logic high, 0 = logic low, V = valid signal, according to AC Operating Conditions and Characteristics.
2. E = true if SE1 and SE3 = 0, and SE2 = 1.
3. Byte write enables, SBx, are evaluated only as new write addresses are loaded.
4. No control inputs except CKE, SBx, and ADV are recognized in a clock cycle where ADV is sampled high.
5. A write with SBx not valid does load addresses.
6. A burst write with SBx not valid does increment address.
7. ADV controls whether the RAM enters burst mode. If the previous cycle was a write, then ADV = 1 results in a burst write. If the previous cycle is a read, then ADV = 1 results in a burst read. ADV = 1 will also continue a deselect cycle.

WRITE TRUTH TABLE

Cycle Type	$\overline{\text{SW}}$	$\overline{\text{SBa}}$	$\overline{\text{SBb}}$	SBc (See Note 1)	SBd (See Note 1)
Read	H	X	X	X	X
Write Byte a	L	L	H	H	H
Write Byte b	L	H	L	H	H
Write Byte c (See Note 1)	L	H	H	L	H
Write Byte d (See Note 1)	L	H	H	H	L
Write All Bytes	L	L	L	L	L

NOTE:

1. Valid only for MCM63Z737.

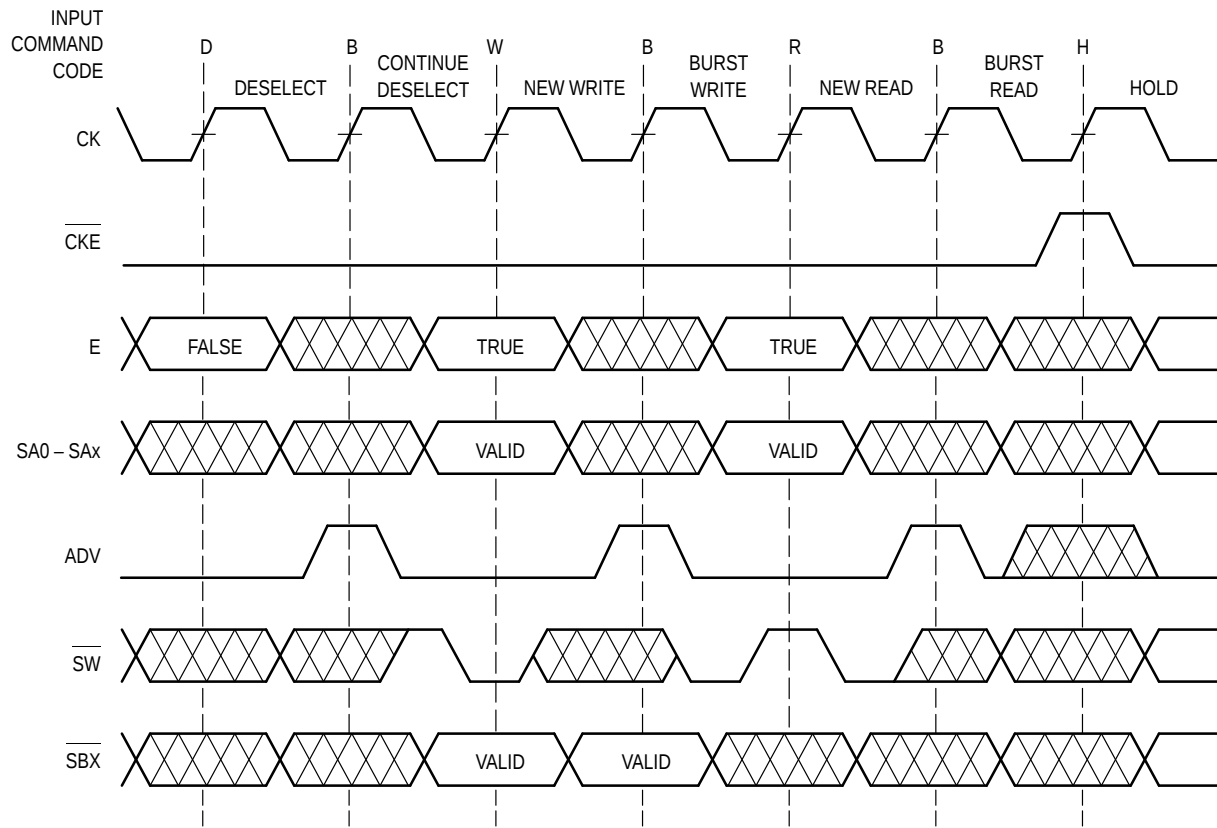
LINEAR BURST ADDRESS TABLE ($\overline{\text{LBO}} = V_{\text{SS}}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X ... X00	X ... X01	X ... X10	X ... X11
X ... X01	X ... X10	X ... X11	X ... X00
X ... X10	X ... X11	X ... X00	X ... X01
X ... X11	X ... X00	X ... X01	X ... X10

INTERLEAVED BURST ADDRESS TABLE ($\overline{\text{LBO}} = V_{\text{DD}}$)

1st Address (External)	2nd Address (Internal)	3rd Address (Internal)	4th Address (Internal)
X ... X00	X ... X01	X ... X10	X ... X11
X ... X01	X ... X00	X ... X11	X ... X10
X ... X10	X ... X11	X ... X00	X ... X01
X ... X11	X ... X10	X ... X01	X ... X00

INPUT COMMAND CODE AND STATE NAME DEFINITION DIAGRAM



NOTE: Cycles are named for their control inputs, not for data I/O state.

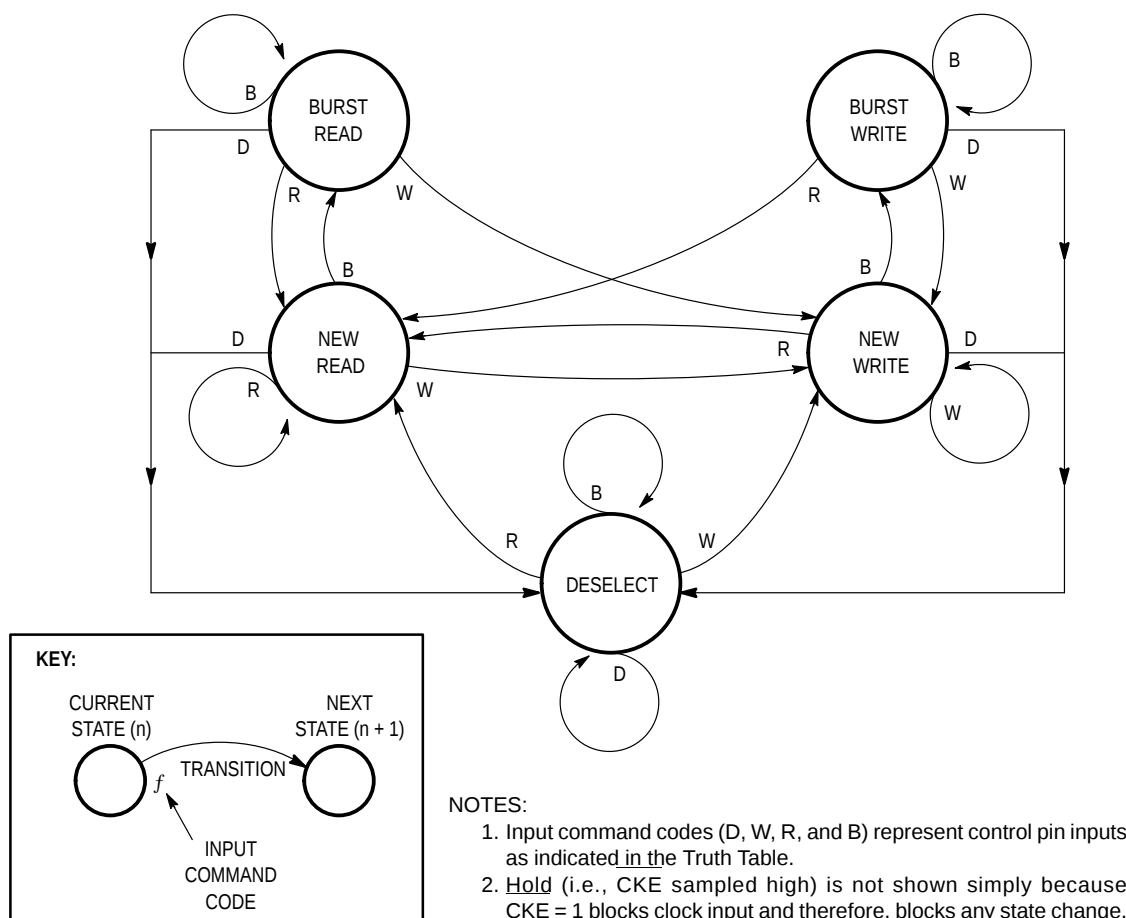


Figure 1. ZBT RAM State Diagram

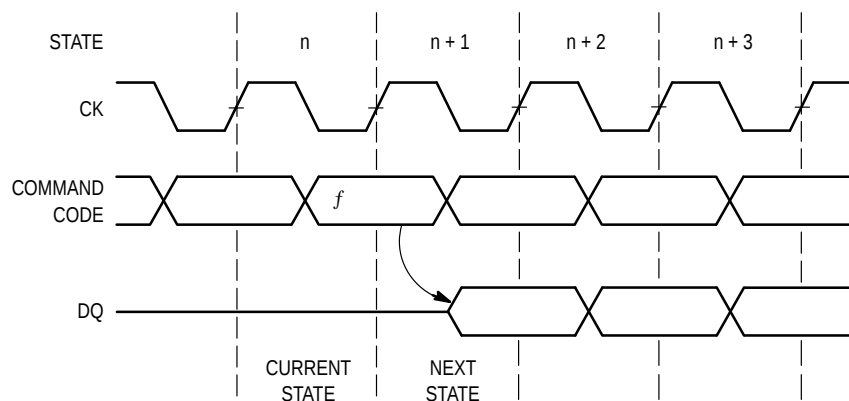


Figure 2. State Definitions for ZBT RAM State Diagram

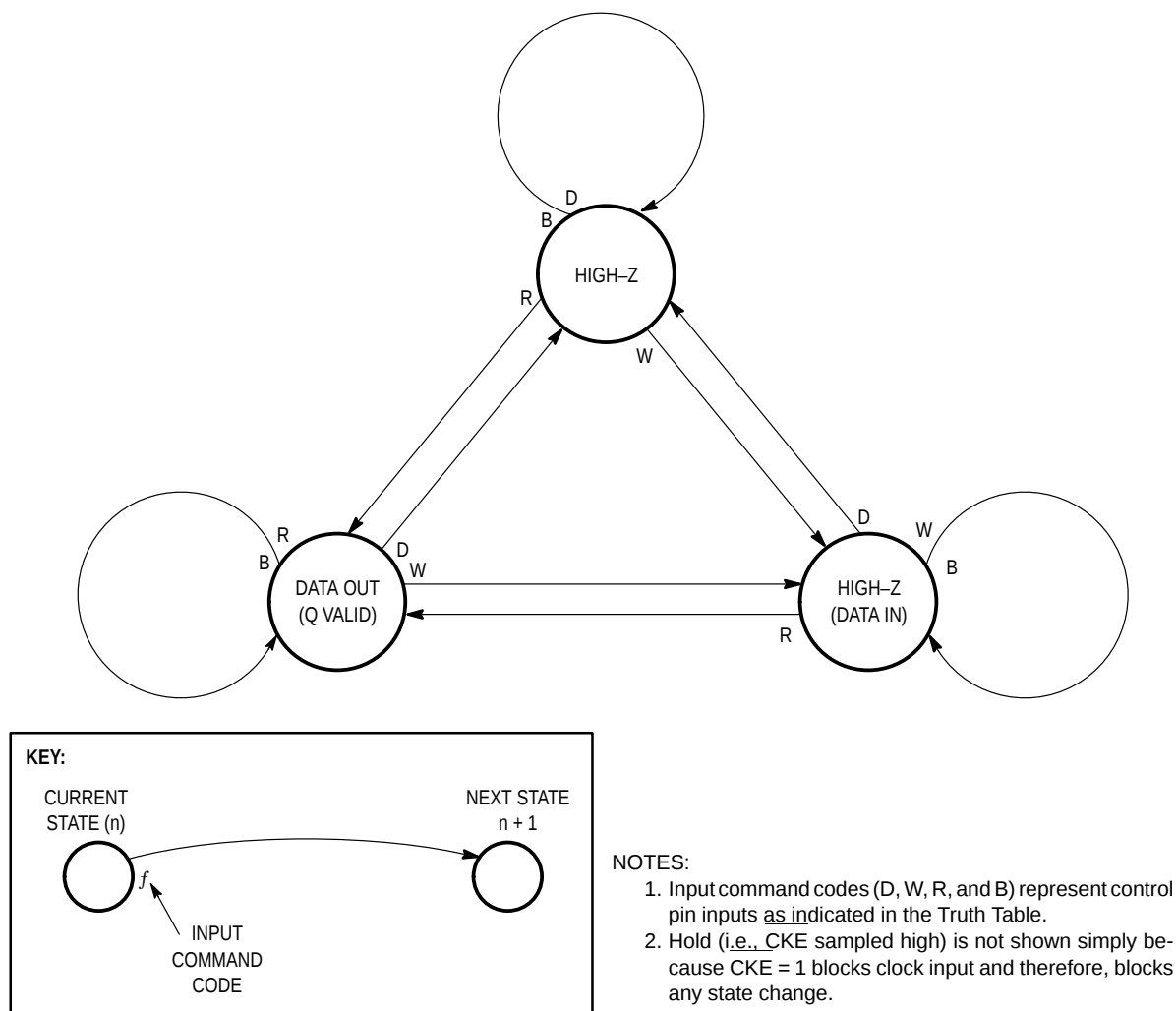


Figure 3. Data I/O State Diagram

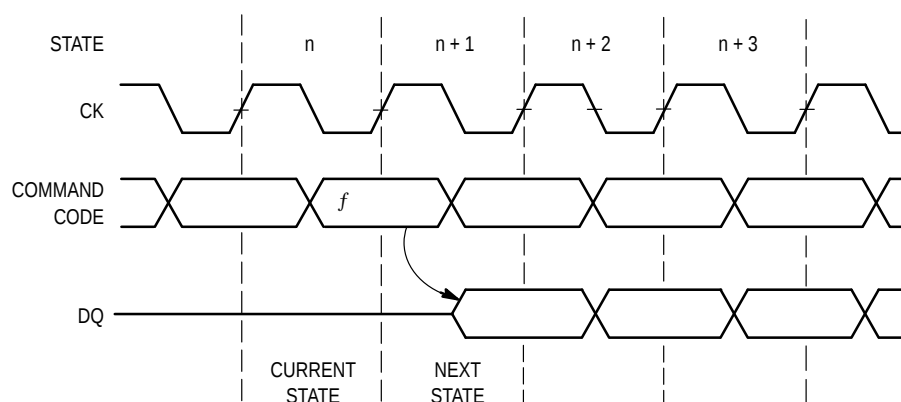


Figure 4. State Definitions for ZBT RAM State Diagram

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit	Notes
Power Supply Voltage	V_{DD}	- 0.5 to + 4.6	V	
I/O Supply Voltage	V_{DDQ}	$V_{SS} - 0.5$ to V_{DD}	V	2
Input Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	- 0.5 to $V_{DD} + 0.5$	V	2
Input Voltage (Three State I/O)	V_{IT}	$V_{SS} - 0.5$ to $V_{DDQ} + 0.5$	V	2
Output Current (per I/O)	I_{out}	± 20	mA	
Package Power Dissipation	P_D	1.3	W	3
Temperature Under Bias	T_{bias}	- 10 to 85	°C	
Storage Temperature	T_{stg}	- 55 to 125	°C	

NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This is a steady-state DC parameter that is in effect after the power supply has achieved its nominal operating level. Power sequencing is not necessary.
3. Power dissipation capability is dependent upon package characteristics and use environment. See Package Thermal Characteristics.

PACKAGE THERMAL CHARACTERISTICS

Thermal Resistance		Symbol	Max	Unit	Notes
Junction to Ambient (@ 200 lfm)	Single-Layer Board	$R_{\theta JA}$	40	°C/W	1, 2
	Four-Layer Board		25		
Junction to Board (Bottom)		$R_{\theta JB}$	17	°C/W	3
Junction to Case (Top)		$R_{\theta JC}$	9	°C/W	4

NOTES:

1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2. Per SEMI G38-87.
3. Indicates the average thermal resistance between the die and the printed circuit board.
4. Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC-883 Method 1012.1).

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{DD} = 3.3 \text{ V} \pm 5\%$, $T_A = 0 \text{ to } 70^\circ\text{C}$ Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
I/O Supply Voltage	V_{DDQ}^*	3.135	3.3	V_{DD}	V
Ambient Temperature	T_A	0	—	70	$^\circ\text{C}$
Input Low Voltage	V_{IL}	-0.3	—	0.8	V
Input High Voltage	V_{IH}	2	—	$V_{DD} + 0.3$	V
Input High Voltage I/O Pins	V_{IH2}	2	—	$V_{DDQ} + 0.3$	V

* V_{DD} and V_{DDQ} are shorted together on the device and must be supplied with identical voltage levels.

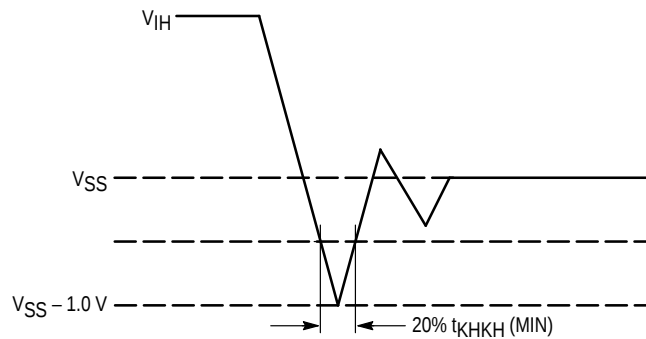


Figure 5. Undershoot Voltage

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Leakage Current ($0 \text{ V} \leq V_{in} \leq V_{DD}$)	$I_{lkg(I)}$	—	—	± 1	μA	1
Output Leakage Current ($0 \text{ V} \leq V_{in} \leq V_{DDQ}$)	$I_{lkg(O)}$	—	—	± 1	μA	
AC Supply Current (Device Selected, All Outputs Open, Freq = Max) Includes Supply Current for Both V_{DD} and V_{DDQ}	I_{DDA}	—	—	300	mA	2, 3, 4
Hold Supply Current (Device Selected, Freq = Max, $V_{DD} = \text{Max}$, $V_{DDQ} = \text{Max}$, $\text{CKE} \geq V_{DD} - 0.2 \text{ V}$, All Inputs Static at CMOS Levels)	I_{DD1}	—	—	15	mA	6
CMOS Standby Supply Current (Device Deselected, Freq = 0, $V_{DD} = \text{Max}$, $V_{DDQ} = \text{Max}$, All Inputs Static at CMOS Levels)	I_{SB2}	—	—	5	mA	5, 6
TTL Standby Supply Current (Device Deselected, Freq = 0, $V_{DD} = \text{Max}$, $V_{DDQ} = \text{Max}$, All Inputs Static at TTL Levels)	I_{SB3}	—	—	25	mA	5, 7
Output Low Voltage ($I_{OL} = 8 \text{ mA}$)	V_{OL}	—	—	0.4	V	
Output High Voltage ($I_{OH} = -8 \text{ mA}$)	V_{OH}	2.4	—	—	V	

NOTES:

1. LBO has an internal pullup and will exhibit leakage currents of $\pm 5 \mu\text{A}$.
2. Reference AC Operating Conditions and Characteristics for Input and Timing.
3. All addresses transition simultaneously low (LSB) then high (MSB).
4. Data states are all zero.
5. Device in deselected mode as defined by the Truth Table.
6. CMOS levels for I/O's are $V_{IT} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DDQ} - 0.2 \text{ V}$. CMOS levels for other inputs are $V_{in} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$.
7. TTL levels for I/O's are $V_{IT} \leq V_{IL}$ or $\geq V_{IH2}$. TTL levels for other inputs are $V_{in} \leq V_{IL}$ or $\geq V_{IH}$.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A = 0 \text{ to } 70^\circ\text{C}$, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	5	pF
Input/Output Capacitance	$C_{I/O}$	—	7	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{DD} = 3.3 \text{ V} \pm 5\%$, $T_A = 0 \text{ to } 70^\circ\text{C}$ Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V
 Input Pulse Levels 0 to 3.0 V
 Input Rise/Fall Time 1 V/ns (20% to 80%)

Output Timing Reference Level 1.5 V
 Output Load See Figure 6 Unless Otherwise Noted
 $R_{\theta JA}$ Under Test TBD

READ/WRITE CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM63Z737-11 MCM63Z819-11 66 MHz		MCM63Z737-15 MCM63Z819-15 50 MHz		Unit	Notes
		Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	20	—	ns	
Clock High Pulse Width	t_{KHKL}	6	—	8	—	ns	3
Clock Low Pulse Width	t_{KLKH}	6	—	8	—	ns	3
Clock Access Time	t_{KHQV}	—	11	—	15	ns	
Output Enable to Output Valid	t_{GLQV}	—	6	—	7	ns	
Clock High to Output Active	t_{KHQX1}	1.5	—	1.5	—	ns	4, 5
Output Hold Time	t_{KHQX}	1.5	—	1.5	—	ns	4
Output Enable to Output Active	t_{GLQX}	0	—	0	—	ns	4, 5
Output Disable to Q High-Z	t_{GHQZ}	—	4.5	—	5	ns	4, 5
Clock High to Q High-Z	t_{KHQZ}	1.5	4.5	1.5	5	ns	4, 5
Setup Times:							
Address	t_{ADKH}	2.5	—	2.5	—	ns	
ADV	t_{LVKH}	2.5		2.5			
Data In	t_{DVKH}	2		2			
Write	t_{WVKH}	2.5		2.5			
Chip Enable	t_{EVKH}	2.5		2.5			
Clock Enable	t_{CVKH}	2.5		2.5			
Hold Times:							
Address	t_{KHAX}	0.5	—	0.5	—	ns	
ADV	t_{KHLX}	0.5		0.5			
Data In	t_{KHDX}	0.5		0.5			
Write	t_{KHWX}	0.5		0.5			
Chip Enable	t_{KHEX}	0.5		0.5			
Clock Enable	$t_{KH CX}$	0.5		0.5			

NOTES:

1. Write is defined as any SBx and SW low. Chip enable is defined as SE1 low, SE2 high, and SE3 low whenever ADV is low.
2. All read and write cycle timings are referenced from CK or G.
3. In order to reduce test correlation issues and to reduce the effects of application specific input edge rate variations on correlation between data sheet parameters and actual system performance, FSRAM AC parametric specifications are always specified at $V_{DDQ}/2$. In some design exercises, it is desirable to evaluate timing using other reference levels. Since the maximum test input edge rate is known and is given in the AC Test Conditions section of the data sheet as 1 V/ns, one can easily interpolate timing values to other reference levels.
4. This parameter is sampled and not 100% tested.
5. Measured at $\pm 200 \text{ mV}$ from steady state.

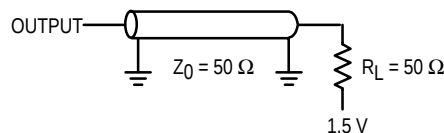


Figure 6. AC Test Load

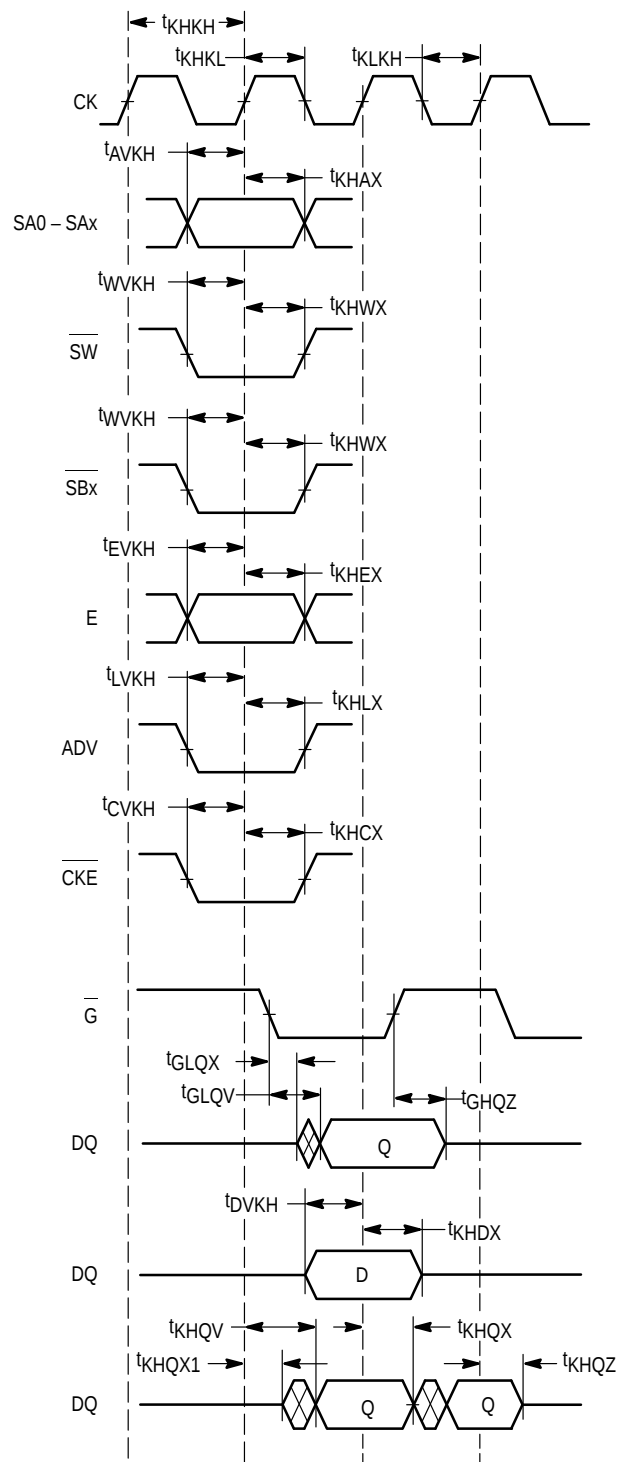
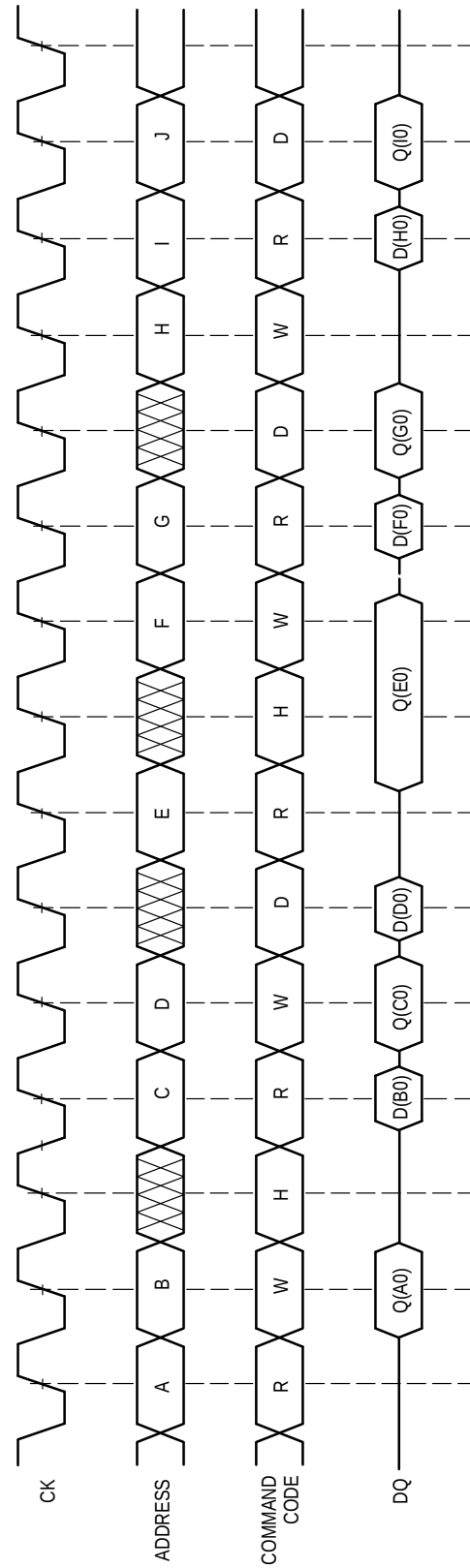


Figure 7. AC Timing Parameter Definitions

READ/WRITE CYCLES WITH HOLD AND DESELECT CYCLES



NOTE: Command code definitions are shown in Truth Table.

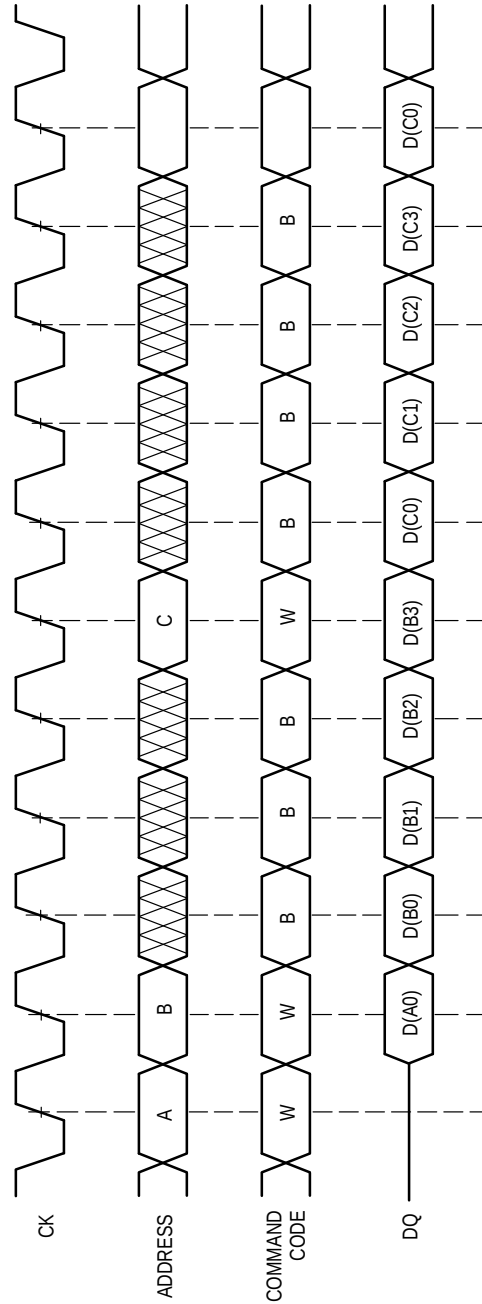
The timing diagram illustrates the sequence of operations for the 24C02. It features four signals: CK (clock), ADDRESS, COMMAND CODE, and DQ (data).

- CK:** A periodic square wave representing the clock signal.
- ADDRESS:** A sequence of 16-bit addresses. The first address is 'A', followed by a series of addresses marked with 'X' (representing unknown or don't-care values), and then 'C'. The last address is also marked with 'X'.
- COMMAND CODE:** A sequence of 8-bit command codes. The first code is 'R', followed by a series of codes marked with 'B' (representing busy or wait states), and then 'R'. The last code is also marked with 'B'.
- DQ:** A sequence of 8-bit data values. The first value is 'Q(A0)', followed by a series of values marked with 'Q(B0)', 'Q(B1)', 'Q(B2)', 'Q(B3)', 'Q(C0)', 'Q(C1)', 'Q(C2)', 'Q(C3)', and finally 'Q(C0)'.

The diagram shows the relationship between these signals over time, with vertical dashed lines indicating the sampling points for the data values.

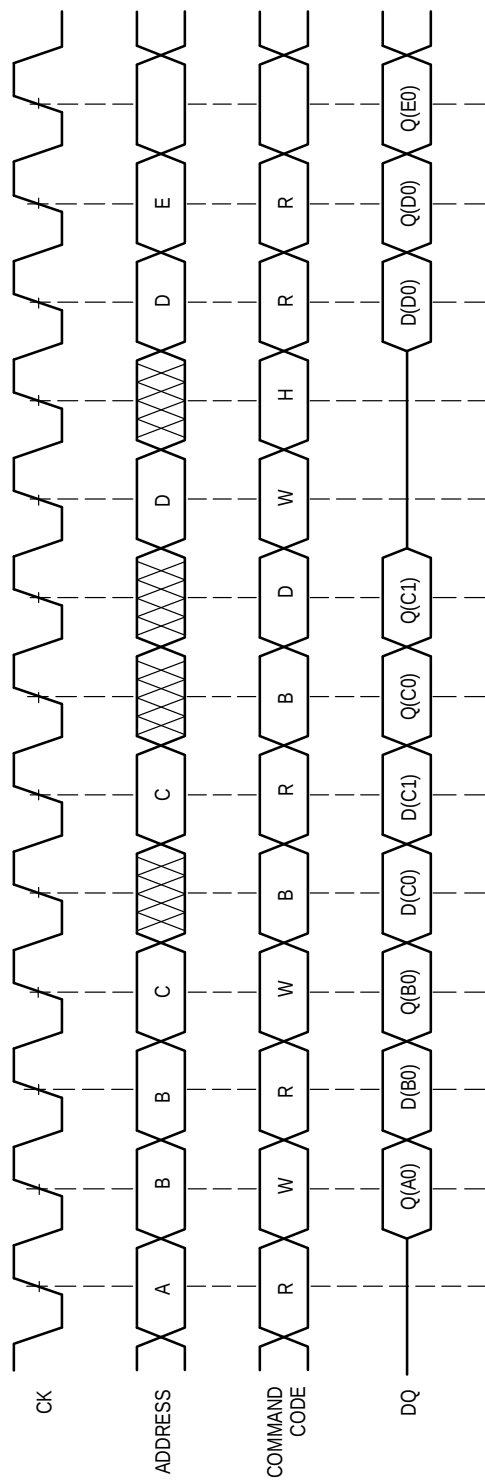
MCM63Z737●MCM63Z819
15

WRITE CYCLES (SINGLE, BURST, AND BURST WRAP-AROUND)

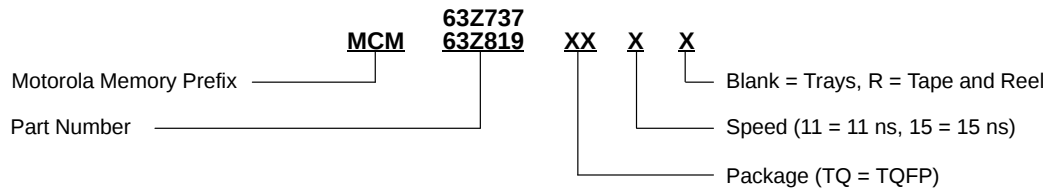


NOTE: Command code definitions are shown in Truth Table.

READ, WRITE, READ COHERENCY WITH HOLD, AND DESELECT CYCLES



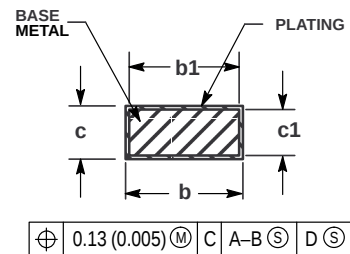
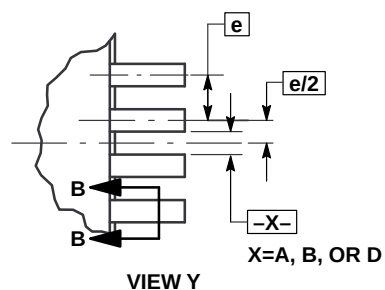
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers —

MCM63Z737TQ11	MCM63Z737TQ15
MCM63Z737TQ11R	MCM63Z737TQ15R
MCM63Z819TQ11	MCM63Z819TQ15
MCM63Z819TQ11R	MCM63Z819TQ15R

**TQ PACKAGE
100-PIN TQFP
CASE 983A-01**



SECTION B-B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS D1 AND B1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.45 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015
b1	0.22	0.33	0.009	0.013
c	0.09	0.20	0.004	0.008
c1	0.09	0.16	0.004	0.006
D	22.00 BSC		0.866 BSC	
D1	20.00 BSC		0.787 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
L1	1.00 REF		0.039 REF	
L2	0.50 REF		0.020 REF	
S	0.20	—	0.008	—
R1	0.08	—	0.003	—
R2	0.08	0.20	0.003	0.008
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	11°	13°	11°	13°
θ3	11°	13°	11°	13°

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