

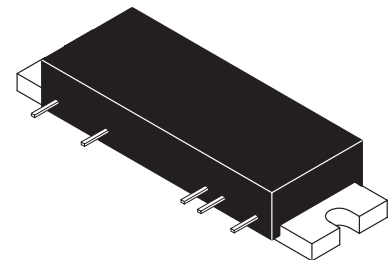
The RF Line PCS Band RF Linear LDMOS Amplifier

Designed for ultra-linear amplifier applications in 50 ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 49.5 dBm Typ
- Power Gain: 29 dB Typ (@ f = 1960 MHz)
- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications

MHL19936

1900–2000 MHz
12 W, 29 dB
RF LINEAR LDMOS AMPLIFIER



CASE 301AY-01, STYLE 1

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	30	Vdc
RF Input Power	P _{in}	+10	dBm
Storage Temperature Range	T _{stg}	-40 to +100	°C
Operating Case Temperature Range	T _C	-20 to +100	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 26 Vdc, T_C = 25°C; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I _{DD}	—	1.4	1.45	A
Power Gain (f = 1960 MHz)	G _p	28	29	30	dB
Gain Flatness (f = 1900–2000 MHz)	G _F	—	0.2	0.4	dB
Power Output @ 1 dB Comp. (f = 1950 MHz)	P _{1dB}	40	41	—	dBm
Input VSWR (f = 1900–2000 MHz)	VSWR _{in}	—	1.2:1	1.5:1	
Third Order Intercept (f ₁ = 1950 MHz, f ₂ = 1955 MHz)	ITO	49	49.5	—	dBm
Noise Figure (f = 2000 MHz)	NF	—	4.2	4.5	dB

TYPICAL CHARACTERISTICS

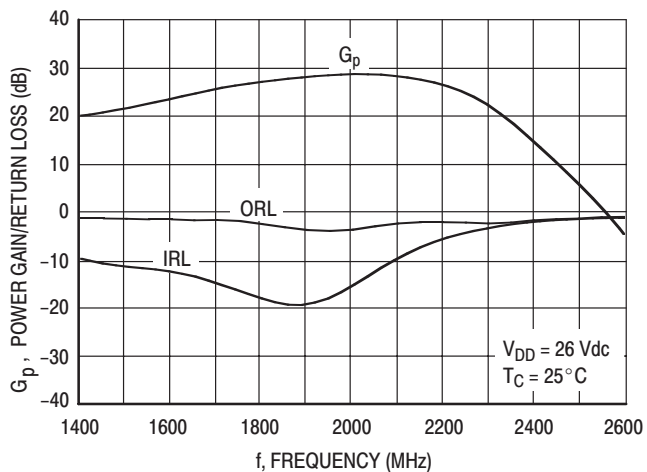


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

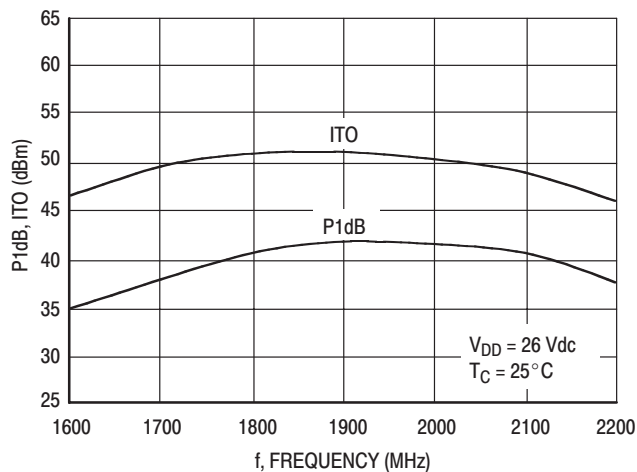


Figure 2. P1dB, ITO versus Frequency

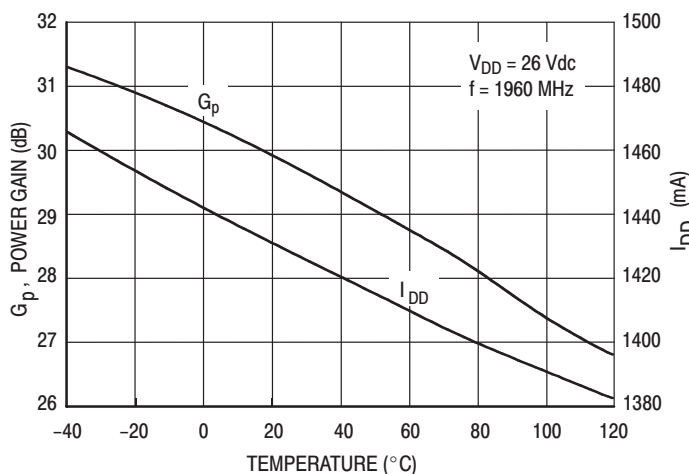


Figure 3. Power Gain, I_{DD} versus Temperature

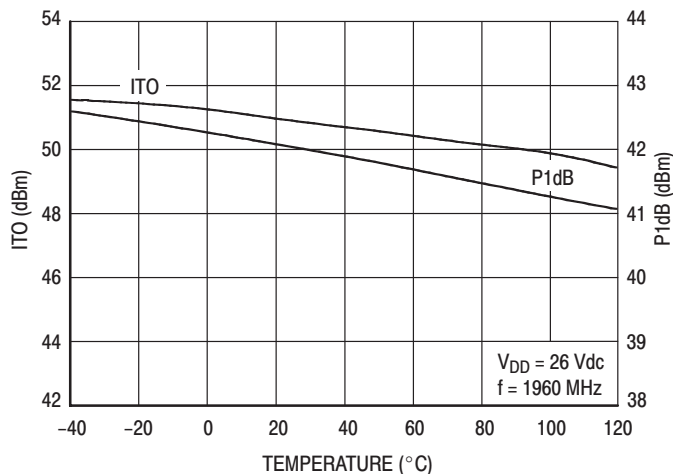


Figure 4. ITO, P1dB versus Temperature

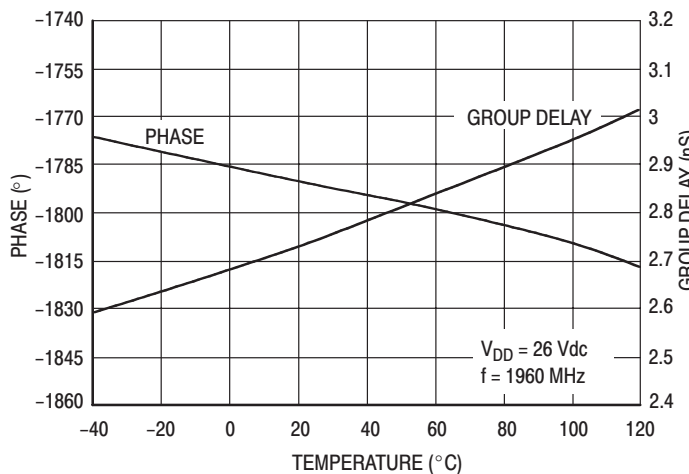


Figure 5. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Temperature

⁽¹⁾In Production Test Fixture

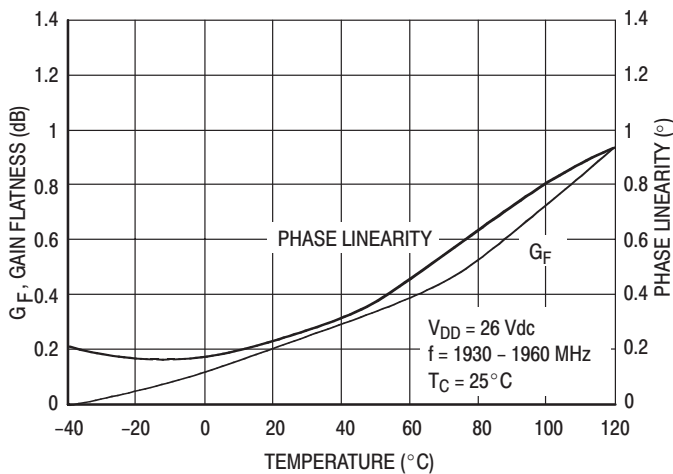


Figure 6. Gain Flatness, Phase Linearity versus Temperature

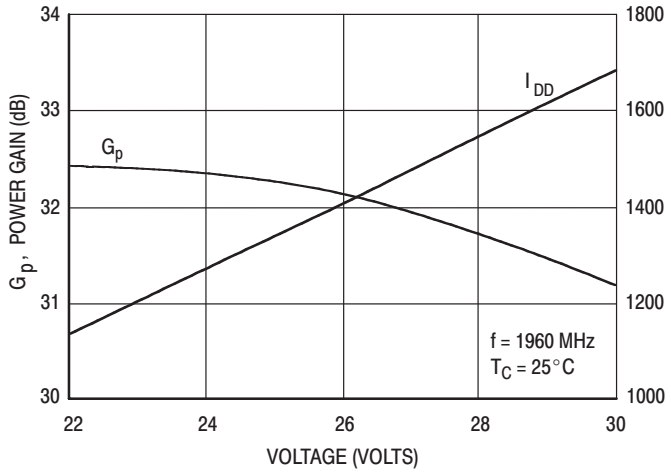


Figure 7. Power Gain, I_{DD} versus Voltage

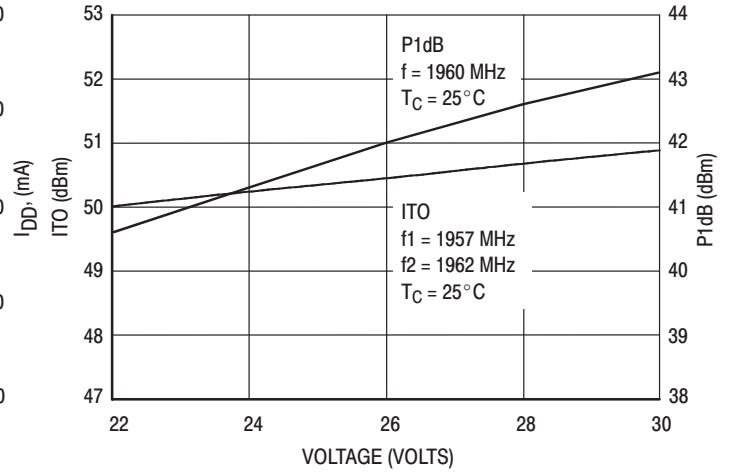


Figure 8. ITO, P1dB versus Voltage

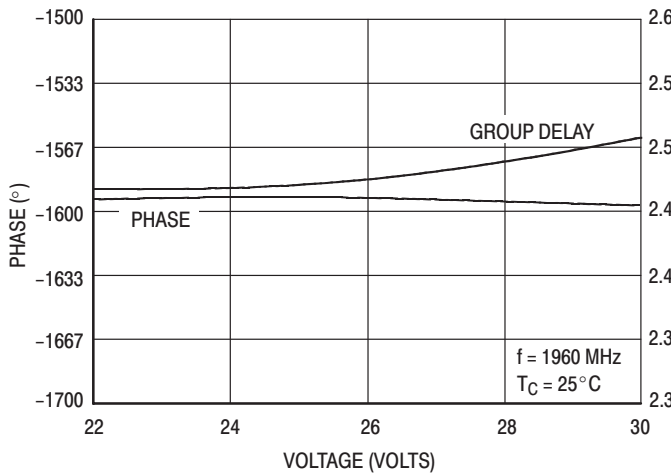


Figure 9. Phase⁽¹⁾, Group Delay⁽¹⁾ versus Voltage

⁽¹⁾In Production Test Fixture

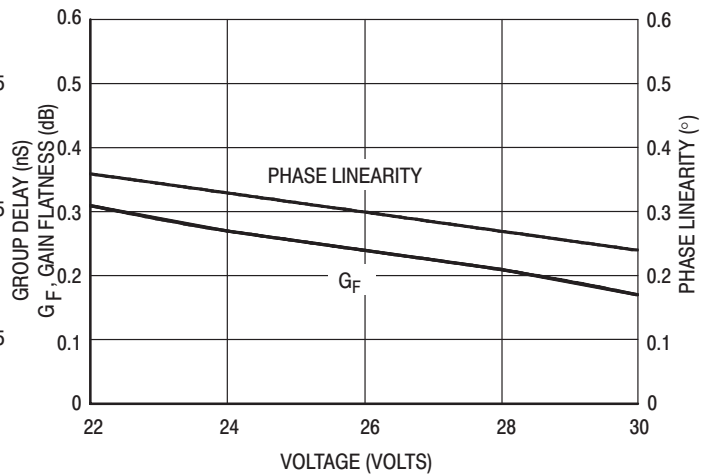
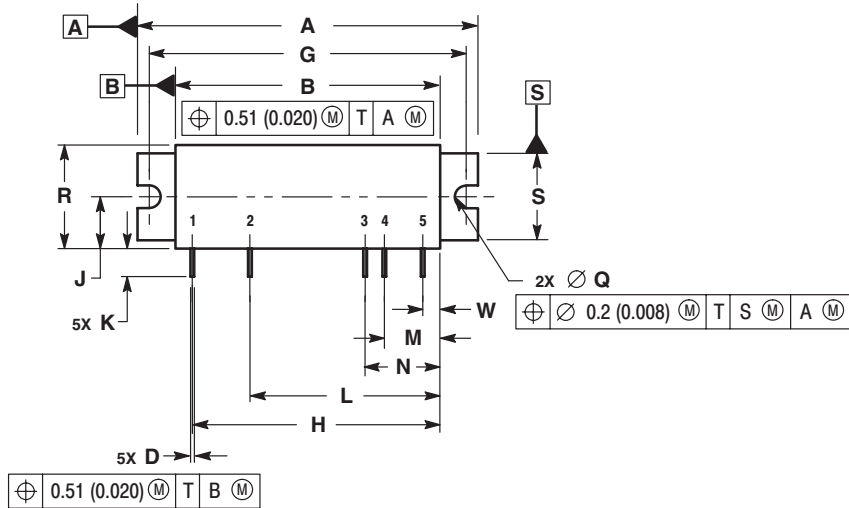


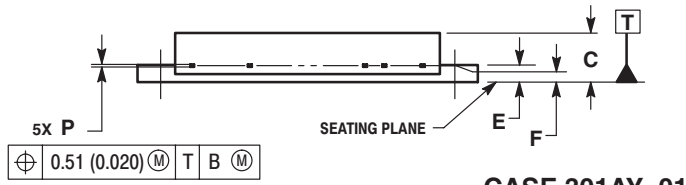
Figure 10. Phase Linearity, Gain Flatness versus Voltage

PACKAGE DIMENSIONS



- NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
 3. DIMENSION F TO CENTER LINE OF LEADS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	44.7	45.21	1.760	1.780
B	34.8	35.31	1.370	1.390
C	6.22	6.73	0.245	0.265
D	0.43	0.58	0.017	0.023
E	2.03	2.54	0.080	0.100
F	2.18 BSC		0.086 BSC	
G	41.91 BSC		1.650 BSC	
H	32.77 BSC		1.290 BSC	
J	6.76	7.11	0.266	0.280
K	3.18	4.19	0.125	0.165
L	25.15 BSC		0.990 BSC	
M	7.37 BSC		0.290 BSC	
N	9.91 BSC		0.390 BSC	
P	0.2	0.33	0.008	0.013
Q	3	3.35	0.118	0.132
R	13.59	14.1	0.535	0.555
S	11.3	11.81	0.445	0.465
W	2.29 BSC		0.090 BSC	



- STYLE 1:
- PIN 1. RF INPUT
 2. VDD1
 3. VDD2
 4. VDD3
 5. RF OUTPUT
- CASE: GROUND

**CASE 301AY-01
ISSUE O**

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