

Complementary Plastic Silicon Power Transistors

... designed for low power audio amplifier and low current, high speed switching applications.

- Collector–Emitter Sustaining Voltage —
 $V_{CEO(sus)} = 60 \text{ Vdc}$ — MJE171, MJE181
 $= 80 \text{ Vdc}$ — MJE172, MJE182
- DC Current Gain —
 $h_{FE} = 30 \text{ (Min) @ } I_C = 0.5 \text{ Adc}$
 $= 12 \text{ (Min) @ } I_C = 1.5 \text{ Adc}$
- Current–Gain — Bandwidth Product —
 $f_T = 50 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$
- Annular Construction for Low Leakages —
 $I_{CBO} = 100 \text{ nA (Max) @ Rated } V_{CB}$

MAXIMUM RATINGS

Rating	Symbol	MJE171 MJE181	MJE172 MJE182	Unit
Collector–Base Voltage	V_{CB}	80	100	Vdc
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	3.0 6.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.5 0.012		Watts $\text{W}/^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	12.5 0.1		Watts $\text{W}/^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	$^\circ\text{C}/\text{W}$

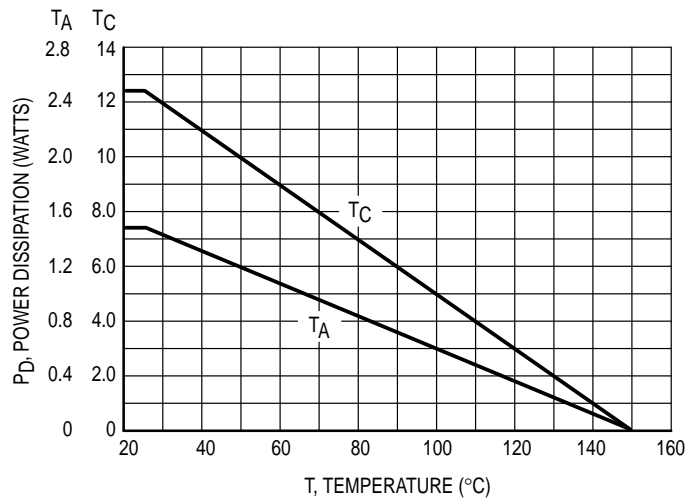


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

PNP
MJE171*

MJE172*
NPN
MJE181*

MJE182*

*Motorola Preferred Device

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60–80 VOLTS
12.5 WATTS

CASE 77–08
TO–225AA

MJE171 MJE172 MJE181 MJE182

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I _C = 10 mAdc, I _B = 0)	V _{CEO(sus)}	60 80	— —	Vdc
Collector Cutoff Current (V _{CB} = 80 Vdc, I _E = 0) (V _{CB} = 100 Vdc, I _E = 0) (V _{CB} = 80 Vdc, I _E = 0, T _C = 150°C) (V _{CB} = 100 Vdc, I _E = 0, T _C = 150°C)	I _{CBO}	— — — —	0.1 0.1 0.1 0.1	μAdc mAdc
Emitter Cutoff Current (V _{BE} = 7.0 Vdc, I _C = 0)	I _{EBO}	—	0.1	μAdc

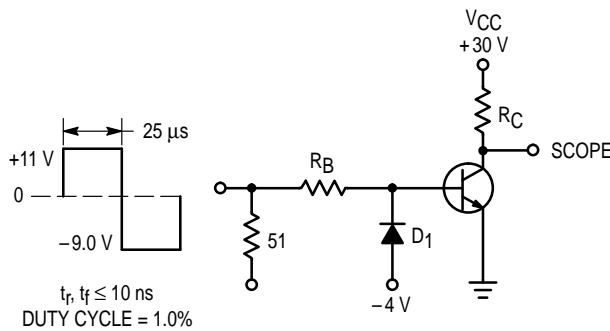
ON CHARACTERISTICS

DC Current Gain (I _C = 100 mAdc, V _{CE} = 1.0 Vdc) (I _C = 500 mAdc, V _{CE} = 1.0 Vdc) (I _C = 1.5 Adc, V _{CE} = 1.0 Vdc)	h _{FE}	50 30 12	250 — —	—
Collector–Emitter Saturation Voltage (I _C = 500 mAdc, I _B = 50 mAdc) (I _C = 1.5 Adc, I _B = 150 mAdc) (I _C = 3.0 Adc, I _B = 600 mAdc)	V _{CE(sat)}	— — —	0.3 0.9 1.7	Vdc
Base–Emitter Saturation Voltage (I _C = 1.5 Adc, I _B = 150 mAdc) (I _C = 3.0 Adc, I _B = 600 mAdc)	V _{BE(sat)}	— —	1.5 2.0	Vdc
Base–Emitter On Voltage (I _C = 500 mAdc, V _{CE} = 1.0 Vdc)	V _{BE(on)}	—	1.2	Vdc

DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product (1) (I _C = 100 mAdc, V _{CE} = 10 Vdc, f _{test} = 10 MHz)	f _T	50	—	MHz
Output Capacitance (V _{CB} = 10 Vdc, I _E = 0, f = 0.1 MHz)	C _{ob}	— —	60 40	pF

(1) f_T = |h_{fe}| • f_{test}.



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
 D₁ MUST BE FAST RECOVERY TYPE, e.g.:
 1N5825 USED ABOVE I_B ≈ 100 mA
 MSD6100 USED BELOW I_B ≈ 100 mA
 FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES.

Figure 2. Switching Time Test Circuit

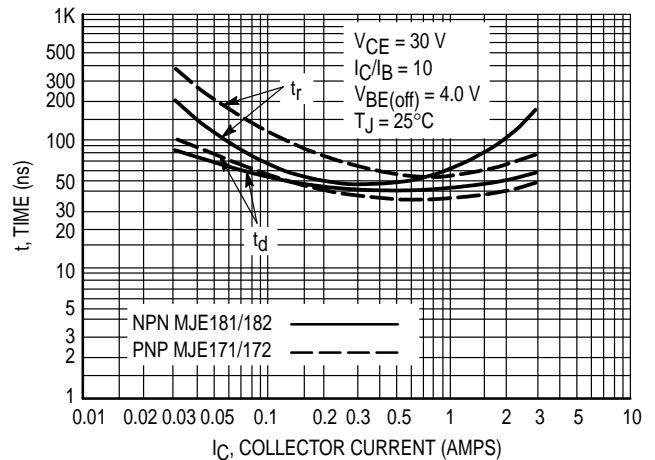


Figure 3. Turn–On Time

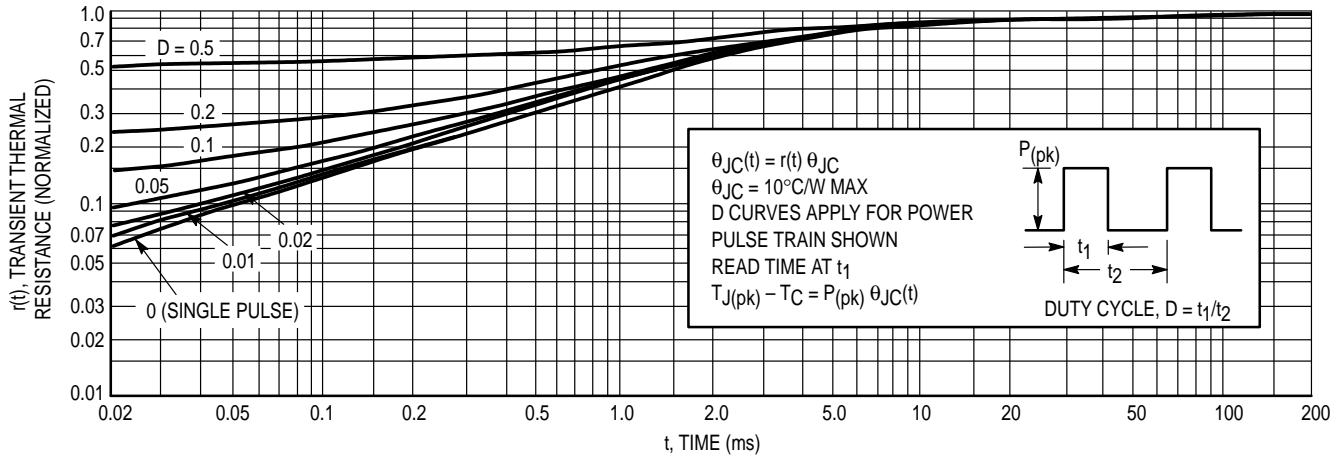


Figure 4. Thermal Response

ACTIVE-REGION SAFE OPERATING AREA

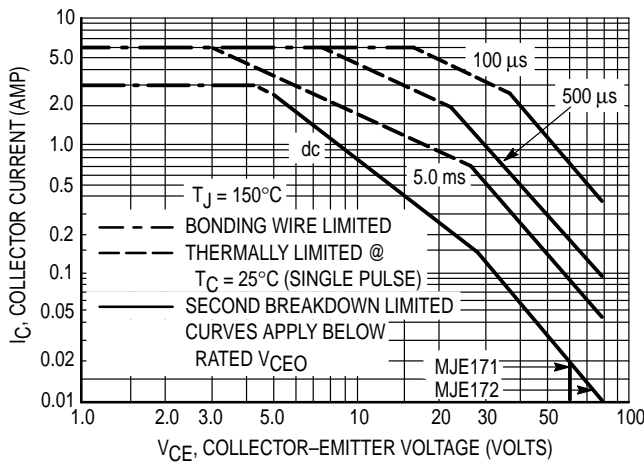


Figure 5. MJE171, MJE172

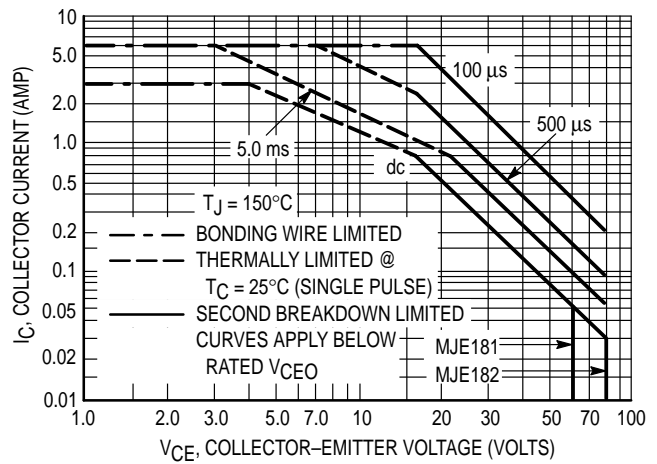


Figure 6. MJE181, MJE182

There are two limitations on the power handling ability of a transistor — average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150^{\circ}\text{C}$; T_C

is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperature, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

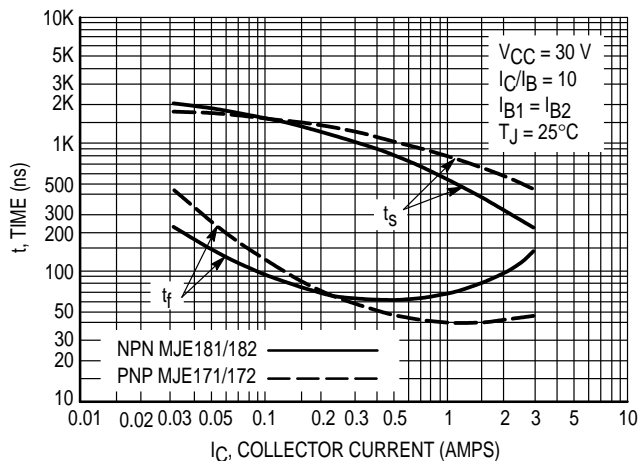


Figure 7. Turn-Off Time

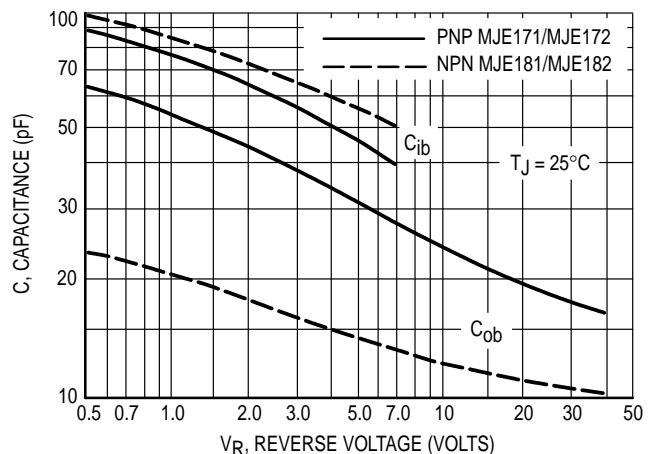
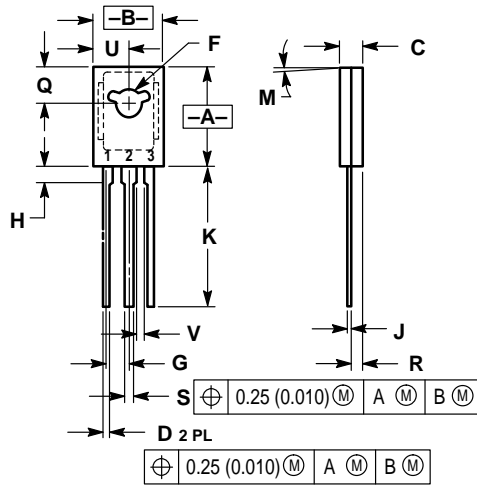


Figure 8. Capacitance

PACKAGE DIMENSIONS



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.055	1.15	1.39
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	—	1.02	—

- STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. BASE

CASE 77-08
 TO-225AA
 ISSUE V

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