

Product Preview

TMOS V™

SOT-223 for Surface Mount N-Channel Enhancement-Mode Silicon Gate

TMOS V is a new technology designed to achieve an on-resistance area product about one-half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E-FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

New Features of TMOS V

- On-resistance Area Product about One-half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E-FET Predecessors

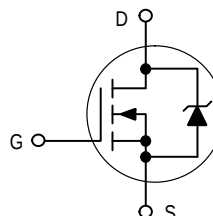
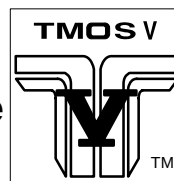
Features Common to TMOS V and TMOS E-FETs

- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E-FET
- Available in 12 mm Tape & Reel
 - Use MMFT3055VT1 to order the 7 inch/1000 unit reel
 - Use MMFT3055VT3 to order the 13 inch/4000 unit reel

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

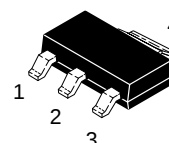
Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	Vdc
Drain-to-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	60	Vdc
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	Vdc
– Non-repetitive ($t_p \leq 10 \text{ ms}$)	V_{GSM}	± 25	Vpk
Drain Current – Continuous	I_D	1.7	Adc
– Continuous @ 100°C	I_D	1.4	
– Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_{DM}	6.0	Apk
Total PD @ $T_A = 25^\circ\text{C}$ mounted on 1" sq. Drain pad on FR-4 bd material	P_D	2.0	Watts
Total PD @ $T_A = 25^\circ\text{C}$ mounted on 0.70" sq. Drain pad on FR-4 bd material		1.7	
Total PD @ $T_A = 25^\circ\text{C}$ mounted on min. Drain pad on FR-4 bd material		0.9	
Derate above 25°C		6.3	mW/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 25 \text{ Vdc}$, $V_{GS} = 10 \text{ Vdc}$, Peak $I_L = 3.4 \text{ Apk}$, $L = 10 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	58	mJ
Thermal Resistance			$^\circ\text{C/W}$
– Junction to Ambient on 1" sq. Drain pad on FR-4 bd material	$R_{\theta JA}$	70	
– Junction to Ambient on 0.70" sq. Drain pad on FR-4 bd material	$R_{\theta JA}$	88	
– Junction to Ambient on min. Drain pad on FR-4 bd material	$R_{\theta JA}$	159	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

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MMFT3055V

TMOS POWER FET
1.7 AMPERES
60 VOLTS
 $R_{DS(on)} = 0.130 \text{ OHM}$



CASE 318E-04, Style 3
TO-261AA

MMFT3055V**ELECTRICAL CHARACTERISTICS** ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 0.25\text{ mAdc}$) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	60 —	— 63	— —	Vdc mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ($V_{DS} = 60\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) ($V_{DS} = 60\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 150^\circ\text{C}$)	I_{DSS}	— —	— —	10 100	μAdc
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	100	nAdc

ON CHARACTERISTICS (1)

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{Adc}$) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	2.0 —	2.8 5.6	4.0 —	Vdc mV/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 0.85\text{ Adc}$)	$R_{DS(on)}$	—	0.115	0.13	Ohm
Drain-to-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.7\text{ Adc}$) ($V_{GS} = 10\text{ Vdc}$, $I_D = 0.85\text{ Adc}$, $T_J = 150^\circ\text{C}$)	$V_{DS(on)}$	— —	— —	0.27 0.25	Vdc
Forward Transconductance ($V_{DS} = 8.0\text{ Vdc}$, $I_D = 1.7\text{ Adc}$)	g_{FS}	1.0	2.7	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{iss}	—	360	500	pF
Output Capacitance		C_{oss}	—	110	150	
Transfer Capacitance		C_{rss}	—	25	50	

SWITCHING CHARACTERISTICS (2)

Turn-On Delay Time	$(V_{DD} = 30\text{ Vdc}$, $I_D = 1.7\text{ Adc}$, $V_{GS} = 10\text{ Vdc}$, $R_G = 9.1\text{ }\Omega$)	$t_{d(on)}$	—	8.0	20	ns
Rise Time		t_r	—	9.0	20	
Turn-Off Delay Time		$t_{d(off)}$	—	32	60	
Fall Time		t_f	—	18	40	
Gate Charge	$(V_{DS} = 48\text{ Vdc}$, $I_D = 1.7\text{ Adc}$, $V_{GS} = 10\text{ Vdc}$)	Q_T	—	13	20	nC
		Q_1	—	2.0	—	
		Q_2	—	5.0	—	
		Q_3	—	4.0	—	

SOURCE-DrAIN DIODE CHARACTERISTICS

Forward On-Voltage (1)	$(I_S = 1.7\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$) ($I_S = 1.7\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 150^\circ\text{C}$)	V_{SD}	— —	0.85 0.7	1.6 —	Vdc
Reverse Recovery Time	$(I_S = 1.7\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $dI_S/dt = 100\text{ A}/\mu\text{s}$)	t_{rr}	—	40	—	ns
		t_a	—	34	—	
		t_b	—	6.0	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.089	—	μC

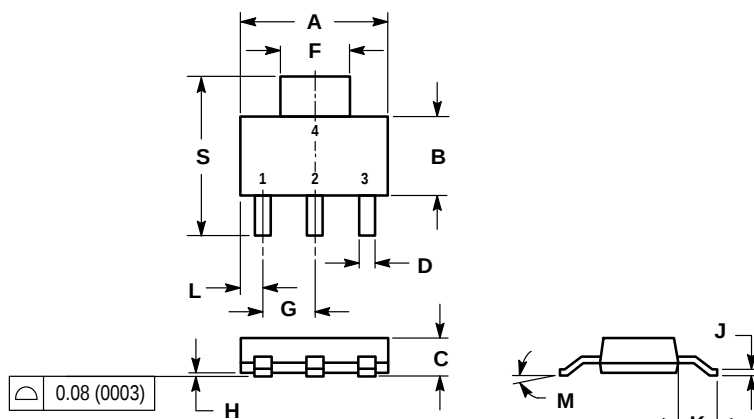
INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)	L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

(2) Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0°	10°	0°	10°
S	0.264	0.287	6.70	7.30

- STYLE 3:
- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 318E-04
ISSUE H

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