

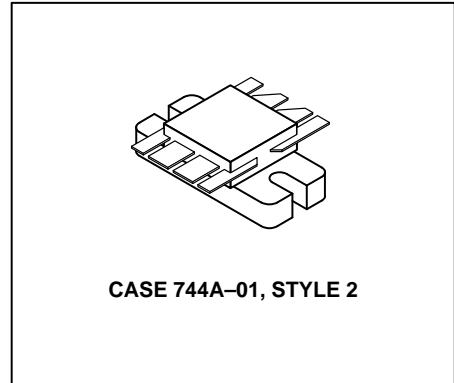
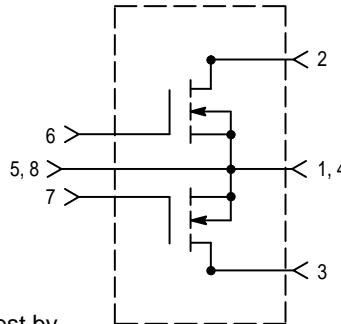
The RF MOSFET Line  
**RF Power**  
**Field Effect Transistors**  
N-Channel Enhancement Mode MOSFET

**MRF177**

**100 W, 28 V, 400 MHz**  
**N-CHANNEL**  
**BROADBAND**  
**RF POWER MOSFET**

Designed for broadband commercial and military applications up to 400 MHz frequency range. Primarily used as a driver or output amplifier in push-pull configurations. Can be used in manual gain control, ALC and modulation circuits.

- Typical Performance at 400 MHz, 28 V:  
Output Power — 100 W  
Gain — 12 dB  
Efficiency — 60%
- Low Thermal Resistance
- Low  $C_{rss}$  — 10 pF Typ @  $V_{DS} = 28$  Volts
- Ruggedness Tested at Rated Output Power
- Nitride Passivated Die for Enhanced Reliability
- Excellent Thermal Stability; Suited for Class A Operation
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.



**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	Vdc
Drain-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	65	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 40$	Vdc
Drain Current — Continuous	$I_D$	16	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ (1) Derate above $25^\circ\text{C}$	$P_D$	270 1.54	Watts W/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Operating Temperature Range	$T_J$	200	$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.65	$^\circ\text{C}/\text{W}$

(1) Total device dissipation rating applies only when the device is operated as an RF push-pull amplifier.

NOTE — **CAUTION** — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic (1)	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain–Source Breakdown Voltage ( $V_{GS} = 0$ , $I_D = 50$ mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 28$ V, $V_{GS} = 0$ )	$I_{DSS}$	—	—	2.0	mAdc
Gate–Source Leakage Current ( $V_{GS} = 20$ V, $V_{DS} = 0$ )	$I_{GSS}$	—	—	1.0	$\mu\text{Adc}$

**ON CHARACTERISTICS (1)**

Gate Threshold Voltage ( $V_{DS} = 10$ V, $I_D = 50$ mA)	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Drain–Source On–Voltage ( $V_{GS} = 10$ V, $I_D = 3.0$ A)	$V_{DS(on)}$	—	—	1.4	Vdc
Forward Transconductance ( $V_{DS} = 10$ V, $I_D = 2.0$ A)	$g_{fs}$	1.8	2.2	—	mhos

**DYNAMIC CHARACTERISTICS (1)**

Input Capacitance ( $V_{DS} = 28$ V, $V_{GS} = 0$ , $f = 1.0$ MHz)	$C_{iss}$	—	100	—	pF
Output Capacitance ( $V_{DS} = 28$ V, $V_{GS} = 0$ , $f = 1.0$ MHz)	$C_{oss}$	—	105	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 28$ V, $V_{GS} = 0$ , $f = 1.0$ MHz)	$C_{rss}$	—	10	—	pF

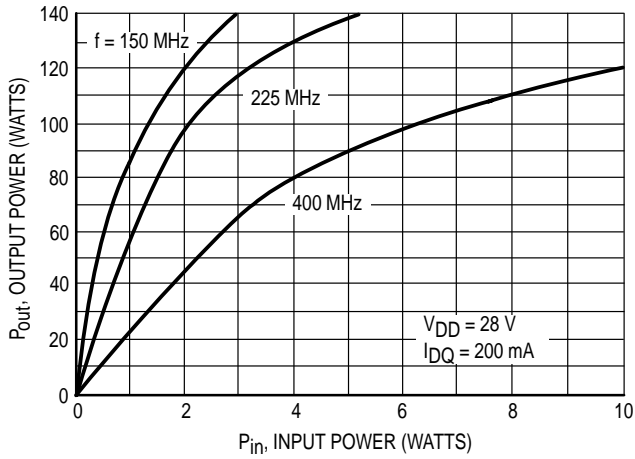
**FUNCTIONAL CHARACTERISTICS (Figure 8) (2)**

Common Source Power Gain ( $V_{DD} = 28$ Vdc, $P_{out} = 100$ W, $f = 400$ MHz, $I_{DQ} = 200$ mA)	$G_{PS}$	10	12	—	dB
Drain Efficiency ( $V_{DD} = 28$ Vdc, $P_{out} = 100$ W, $f = 400$ MHz, $I_{DQ} = 200$ mA)	$\eta$	55	60	—	%
Electrical Ruggedness ( $V_{DD} = 28$ Vdc, $P_{out} = 100$ W, $f = 400$ MHz, $I_{DQ} = 200$ mA, Load VSWR = 30:1, All Phase Angles At Frequency of Test)	$\psi$	No Degradation in Output Power Before & After Test			

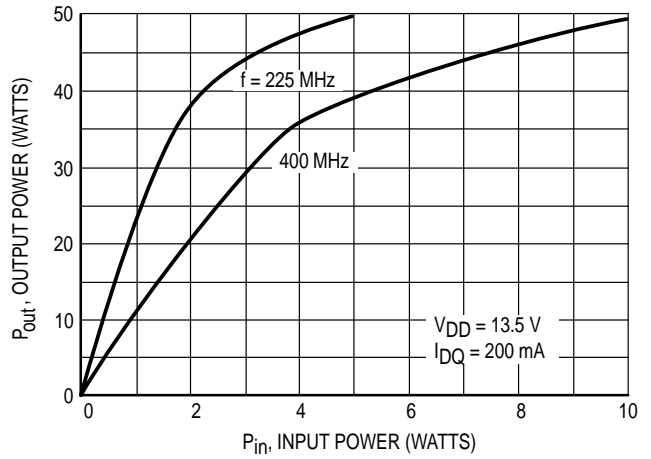
(1) Note each transistor chip measured separately

(2) Both transistor chips operating in push–pull amplifier

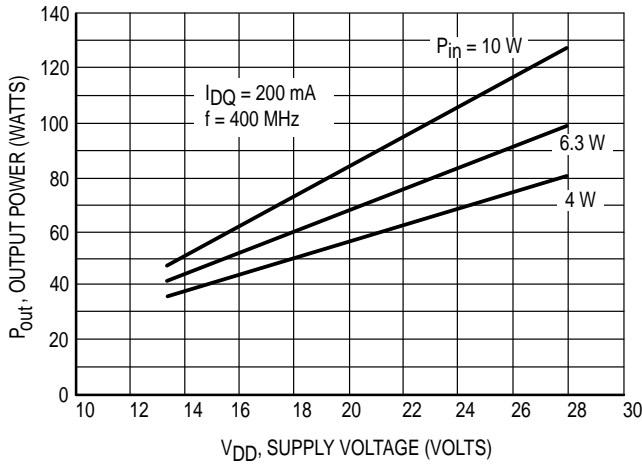
## TYPICAL CHARACTERISTICS



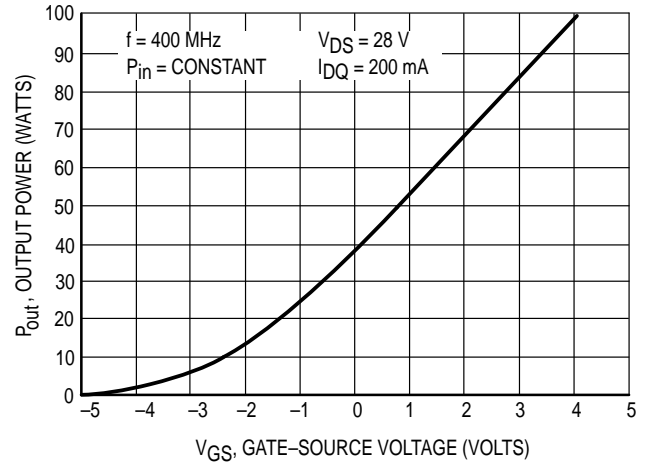
**Figure 1. Output Power versus Input Power**



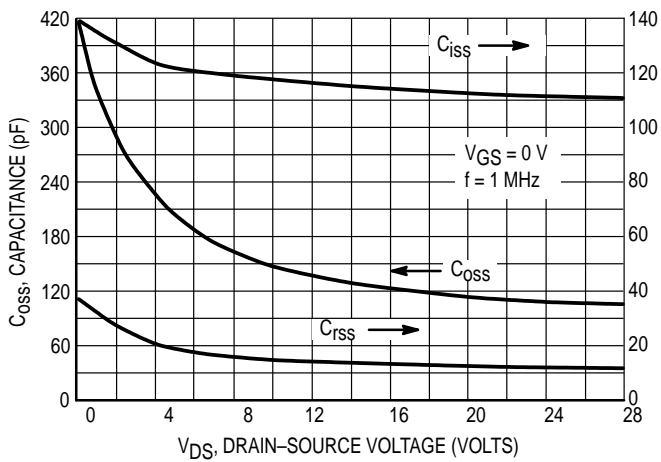
**Figure 2. Output Power versus Input Power**



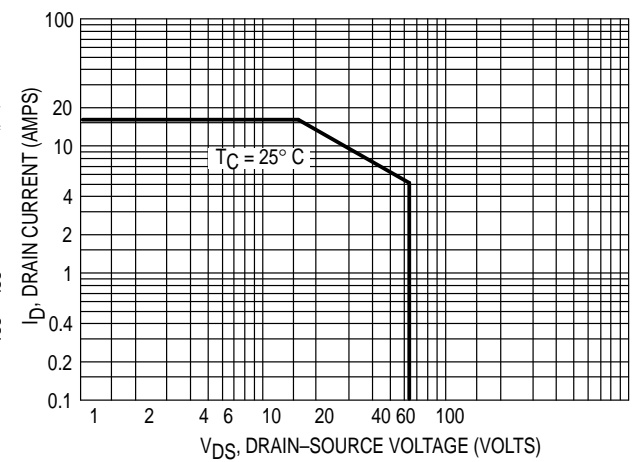
**Figure 3. Output Power versus Supply Voltage**



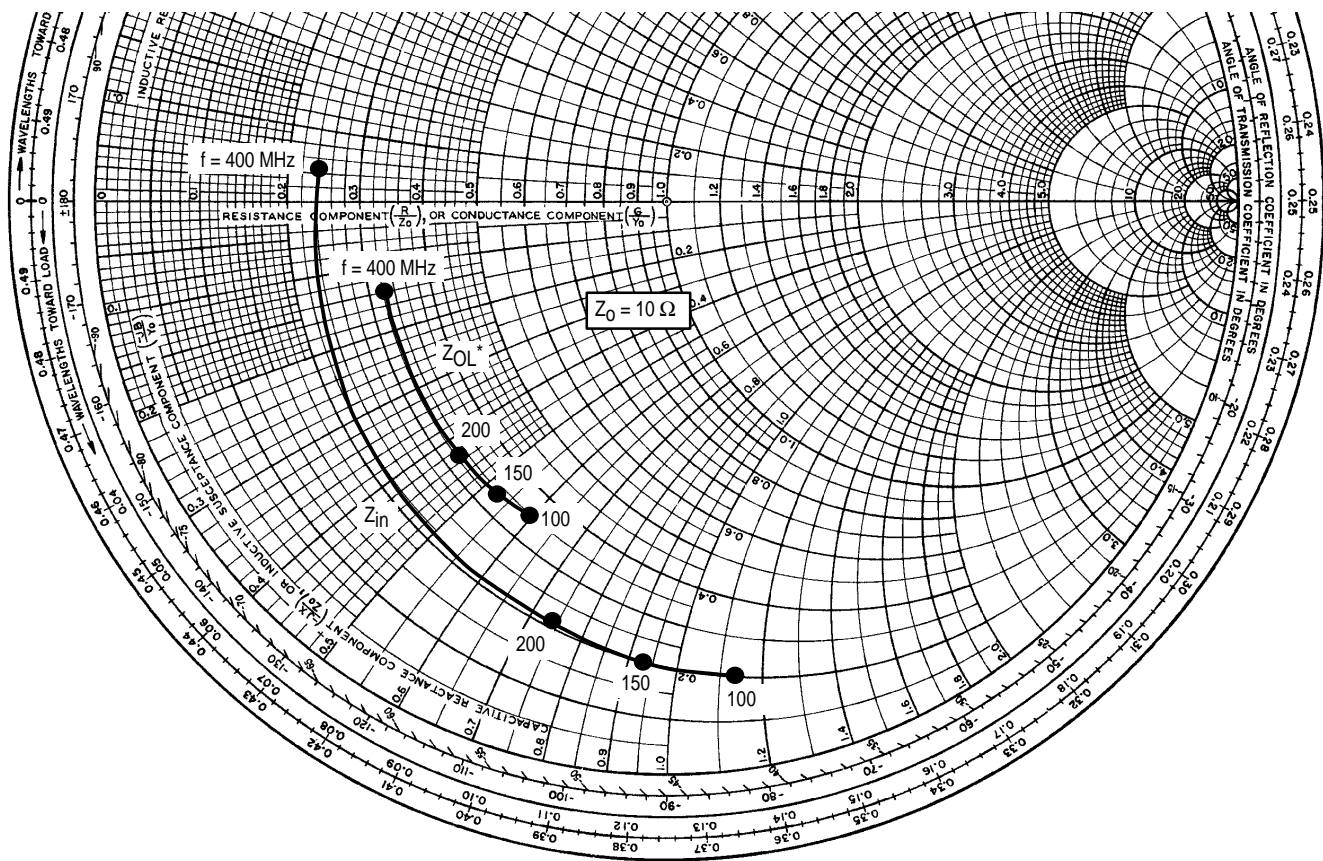
**Figure 4. Output Power versus Gate Voltage**



**Figure 5. Capacitance versus Drain Voltage**



**Figure 6. DC Safe Operating Area**

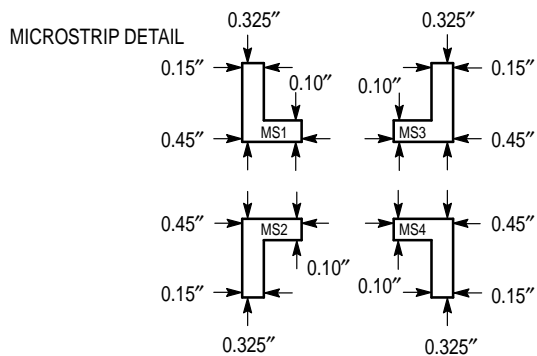
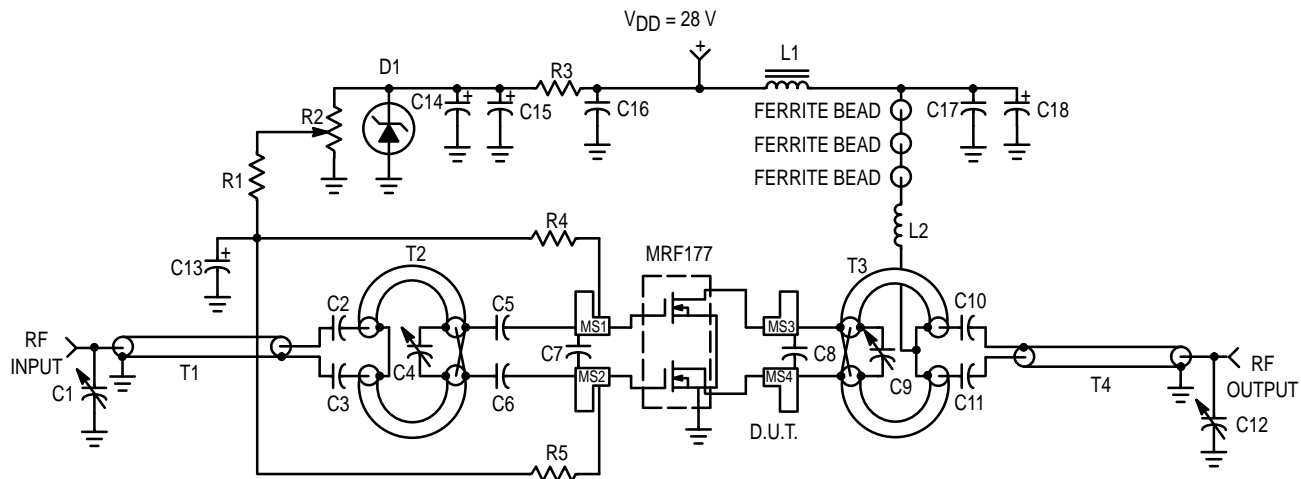


NOTE: Input and Output Impedance values given are measured gate-to-gate and drain-to-drain respectively.

V <sub>DD</sub> = 28 V I <sub>DQ</sub> = 200 mA P <sub>out</sub> = 100 W		
f (MHz)	Z <sub>in</sub> Ohms	Z <sub>OL</sub> * Ohms
100	2.0 - j11.5	3.5 - j6
150	2.05 - j9.45	3.35 - j5.34
200	2.1 - j7.5	3.3 - j4.4
400	2.35 + j0.4	3.2 - j1.38

Z<sub>OL</sub>\*: Conjugate of optimum load impedance into which the device operates at a given output power, voltage, current and frequency.

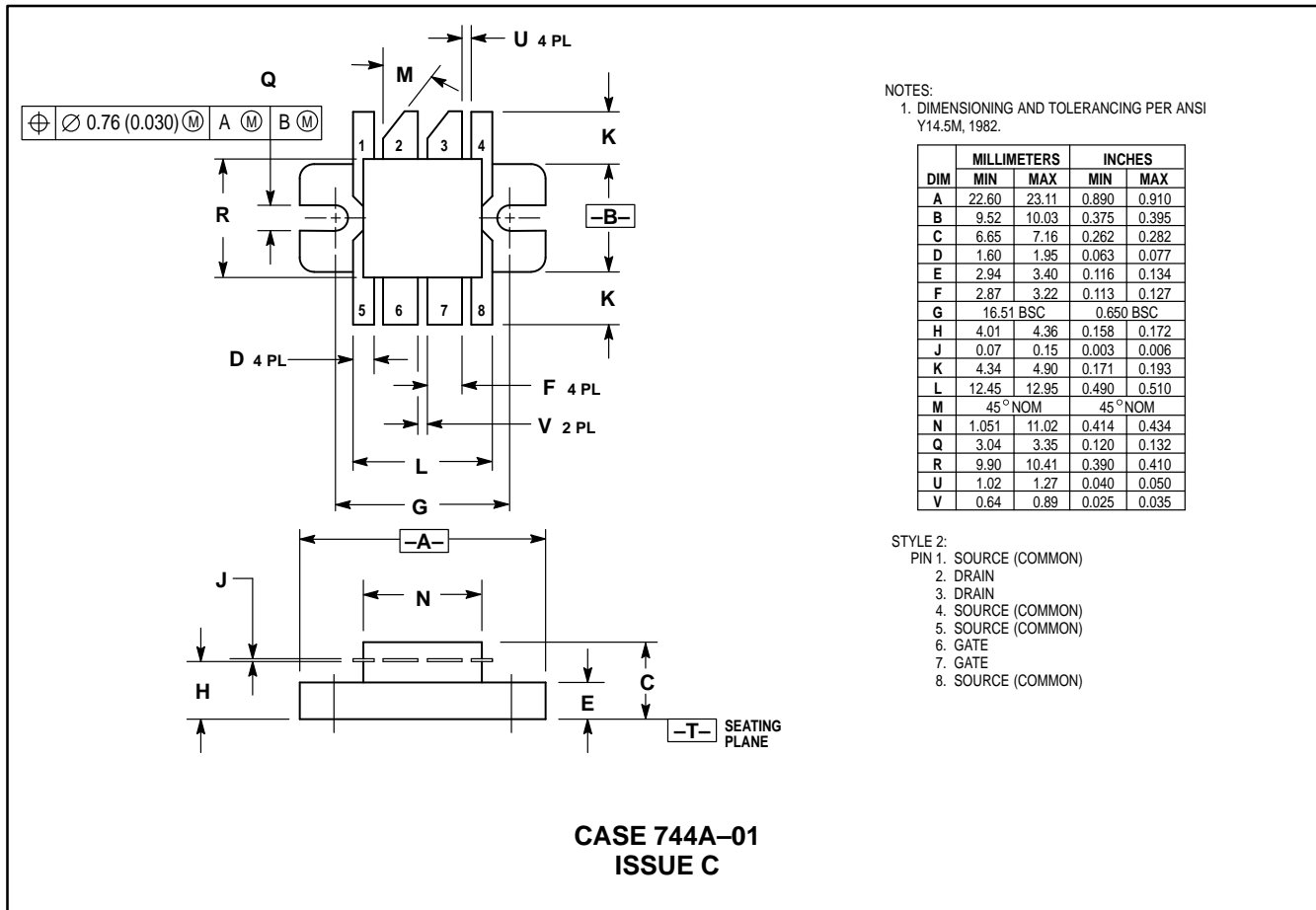
Figure 7. Impedance or Admittance Coordinates



- |                          |                                |            |   |
|--------------------------|--------------------------------|------------|---|
| C1, C12                  | 1-10 pF JOHANSON OR EQUIVALENT | D1         | 1N5347B, 20 Vdc   |
| C2, C3, C5, C6, C10, C11 | 270 pF ATC 100 MIL CHIP CAP    | L1         | 1-TURN NO. 18, 0.25", 2-HOLE FERRITE BEAD   |
| C4, C9                   | 1-20 pF                        | L2         | 8-1/2 TURNS NO. 18, CLOSE WOUND .375" DIA.  |
| C7                       | 36 pF CHIP CAP                 | R1, R4, R5 | 10 kΩ @ 1/2 W RESISTOR  |
| C8                       | 10 pF CHIP CAP                 | R2         | 10 kΩ, 10 TURN RESISTOR   |
| C13, C14                 | 0.1 μFD @ 50 Vdc               | R3         | 2.0 kΩ @ 1/2 W RESISTOR   |
| C15, C18                 | 10 μFD @ 50 Vdc                | T1         | 1-1/2 T, 50 Ω COAX, .034" DIA. ON DUAL 0.5" FERRITE CORE                                    |
| C16                      | 500 pF BUTTON                  | T2         | 2.0" 25 Ω COAX, .075" DIA.  |
| C17                      | 1000 pF UNCASSED MICA          | T3         | 2.1" 10 Ω COAX, .075" DIA.  |
|                          |                                | T4         | 4.0" 50 Ω COAX, .0865" DIA.   |
|                          |                                | BOARD      | Dielectric Thickness = 0.060" 2oz Copper, Cu-Clad, Teflon Fiberglass, ε <sub>r</sub> = 2.55 |

Figure 8. Test Circuit Electrical Schematic

# PACKAGE DIMENSIONS



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