

# The RF MOSFET Line

## Power Field-Effect Transistor

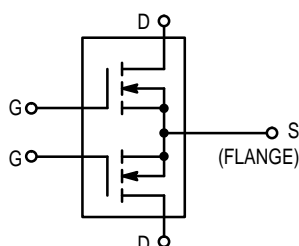
### N-Channel Enhancement-Mode

Designed primarily for wideband large-signal output and driver stages from 100 – 500 MHz.

- Guaranteed Performance @ 500 MHz, 28 Vdc
  - Output Power — 150 Watts
  - Power Gain — 10 dB (Min)
  - Efficiency — 50% (Min)
  - 100% Tested for Load Mismatch at all Phase Angles with VSWR 30:1
- Overall Lower Capacitance @ 28 V
  - $C_{iss}$  — 135 pF
  - $C_{oss}$  — 140 pF
  - $C_{rss}$  — 17 pF
- Simplified AVC, ALC and Modulation

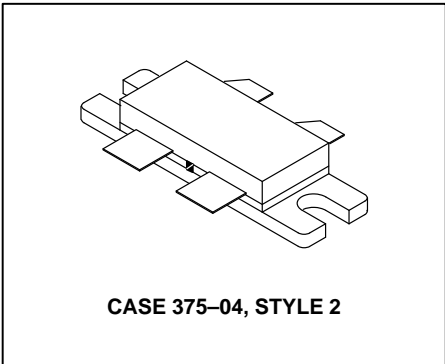
Typical data for power amplifiers in industrial and commercial applications:

- Typical Performance @ 400 MHz, 28 Vdc
  - Output Power — 150 Watts
  - Power Gain — 12.5 dB
  - Efficiency — 60%
- Typical Performance @ 225 MHz, 28 Vdc
  - Output Power — 200 Watts
  - Power Gain — 15 dB
  - Efficiency — 65%



**MRF275G**

**150 W, 28 V, 500 MHz**  
**N-CHANNEL MOS**  
**BROADBAND**  
**100 – 500 MHz**  
**RF POWER FET**



#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	Vdc
Drain-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	65	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 40$	Adc
Drain Current — Continuous	$I_D$	26	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	400 2.27	Watts W/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.44	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS (1)**

Drain–Source Breakdown Voltage ( $V_{GS} = 0$ , $I_D = 50$ mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 28$ V, $V_{GS} = 0$ )	$I_{DSS}$	—	—	1	mA
Gate–Source Leakage Current ( $V_{GS} = 20$ V, $V_{DS} = 0$ )	$I_{GSS}$	—	—	1	$\mu\text{A}$

**ON CHARACTERISTICS (1)**

Gate Threshold Voltage ( $V_{DS} = 10$ V, $I_D = 100$ mA)	$V_{GS(th)}$	1.5	2.5	4.5	Vdc
Drain–Source On–Voltage ( $V_{GS} = 10$ V, $I_D = 5$ A)	$V_{DS(on)}$	0.5	0.9	1.5	Vdc
Forward Transconductance ( $V_{DS} = 10$ V, $I_D = 2.5$ A)	$g_{fs}$	3	3.75	—	mhos

**DYNAMIC CHARACTERISTICS (1)**

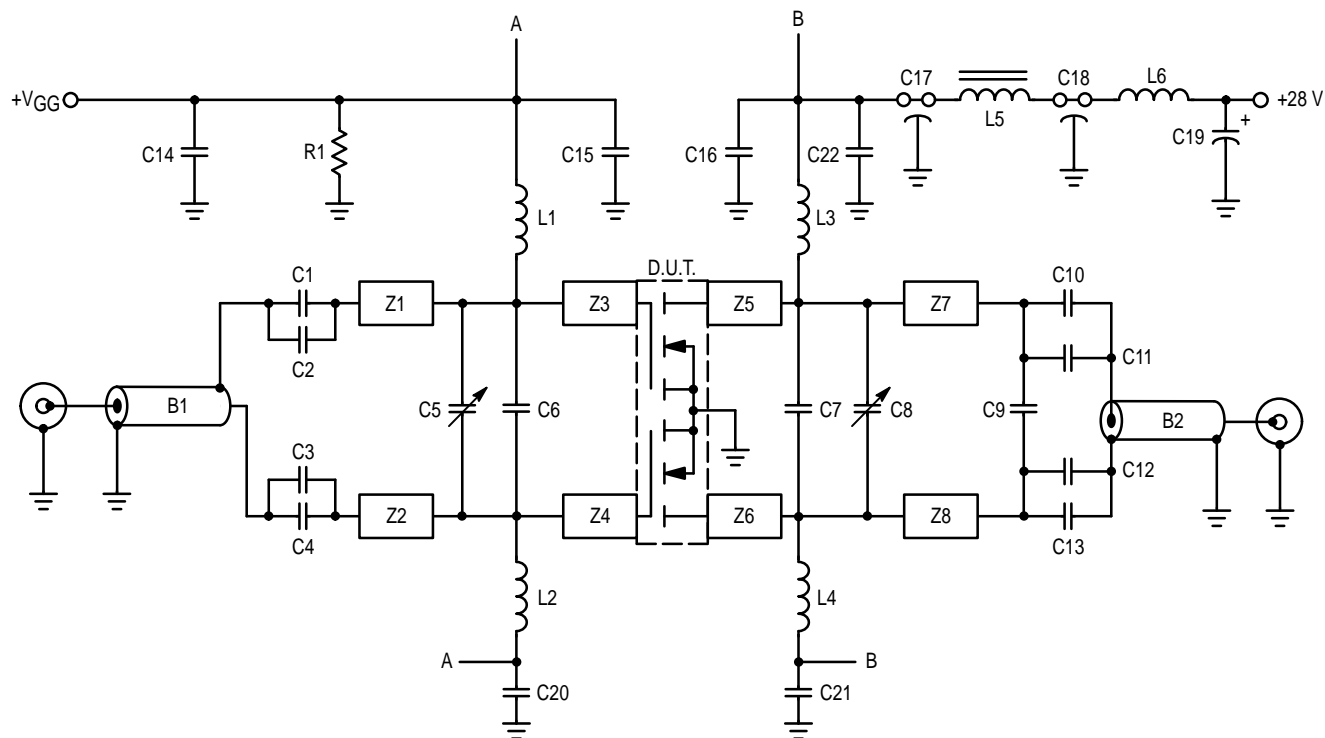
Input Capacitance ( $V_{DS} = 28$ V, $V_{GS} = 0$ , $f = 1$ MHz)	$C_{iss}$	—	135	—	pF
Output Capacitance ( $V_{DS} = 28$ V, $V_{GS} = 0$ , $f = 1$ MHz)	$C_{oss}$	—	140	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 28$ V, $V_{GS} = 0$ , $f = 1$ MHz)	$C_{rss}$	—	17	—	pF

**FUNCTIONAL CHARACTERISTICS (2) (Figure 1)**

Common Source Power Gain ( $V_{DD} = 28$ V, $P_{out} = 150$ W, $f = 500$ MHz, $I_{DQ} = 2 \times 100$ mA)	$G_{ps}$	10	11.2	—	dB
Drain Efficiency ( $V_{DD} = 28$ V, $P_{out} = 150$ W, $f = 500$ MHz, $I_{DQ} = 2 \times 100$ mA)	$\eta$	50	55	—	%
Electrical Ruggedness ( $V_{DD} = 28$ V, $P_{out} = 150$ W, $f = 500$ MHz, $I_{DQ} = 2 \times 100$ mA, VSWR 30:1 at all Phase Angles)	$\psi$	No Degradation in Output Power			

(1.) Each side of device measured separately.

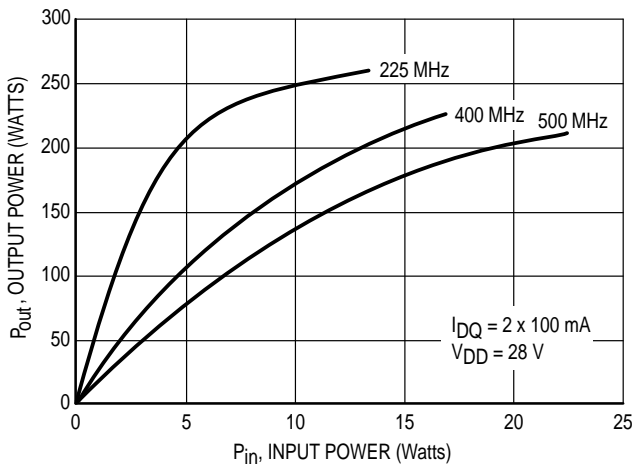
(2.) Measured in push–pull configuration.



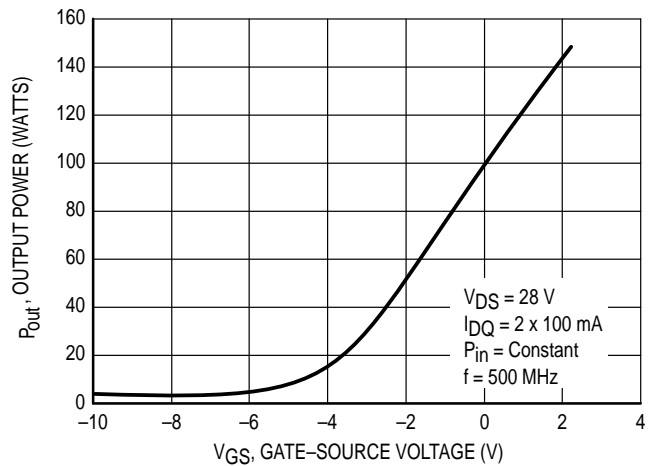
B1	Balun, 50 $\Omega$ , 0.086" O.D. 2" Long, Semi Rigid Coax	L5	Ferroxcube VK200 20/4B
B2	Balun, 50 $\Omega$ , Coax 0.141" O.D. 2" Long, Semi Rigid	L6	4 Turns #16, 0.340" I.D., Enameled Wire
C1, C2, C3, C4,	270 pF, ATC Chip Capacitor	R1	1.0 k $\Omega$ , 1/4 W Resistor
C10, C11, C12, C13	1.0–20 pF, Trimmer Capacitor, Johanson	W1 – W4	20 x 200 x 250 mils, Wear Pads, Beryllium–Copper, (See Component Location Diagram)
C5, C8	22 pF, Mini–Unelco Capacitor	Z1, Z2	1.10" x 0.245", Microstrip Line
C6	15 pF, Unelco Capacitor	Z3, Z4, Z5, Z6	0.300" x 0.245", Microstrip Line
C7	2.1 pF, ATC Chip Capacitor	Z7, Z8	1.00" x 0.245", Microstrip Line
C9	0.1 $\mu$ F, Ceramic Capacitor	Board material	0.060" Teflon–fiberglass, $\epsilon_r = 2.55$ , copper clad both sides, 2 oz. copper.
C14, C15, C16,	680 pF, Feedthru Capacitor	Points A are connected together on PCB.	
C20, C21, C22	10 $\mu$ F, 50 V, Electrolytic Capacitor, Tantalum	Points B are connected together on PCB.	
C17, C18	10 Turns AWG #24, 0.145" O.D., 106 nH Taylor–Spring Inductor		
C19	10 Turns AWG #18, 0.340" I.D., Enameled Wire		
L1, L2			
L3, L4			

Figure 1. 500 MHz Test Circuit

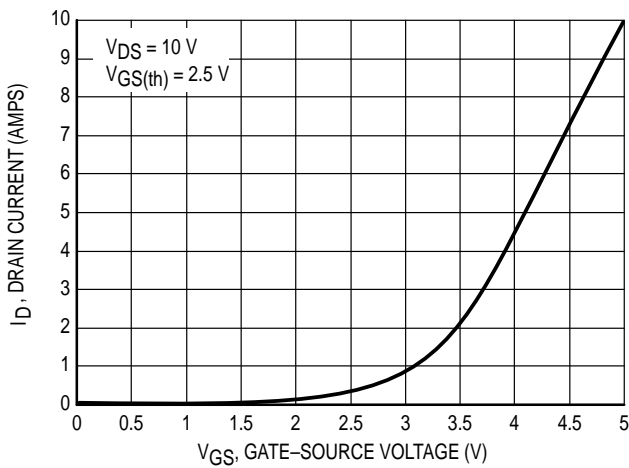
## TYPICAL CHARACTERISTICS



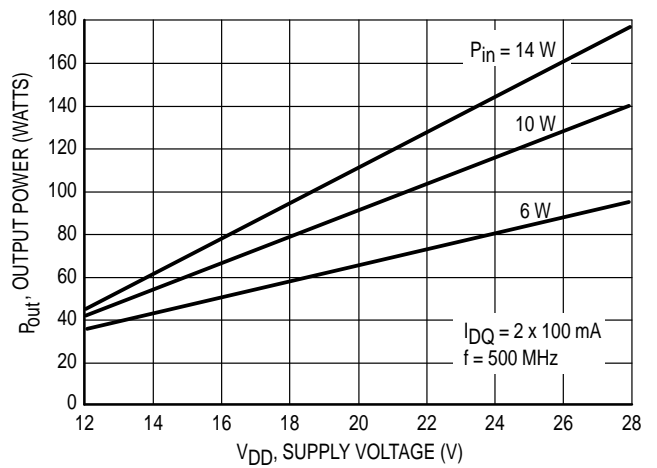
**Figure 2. Output Power versus Input Power**



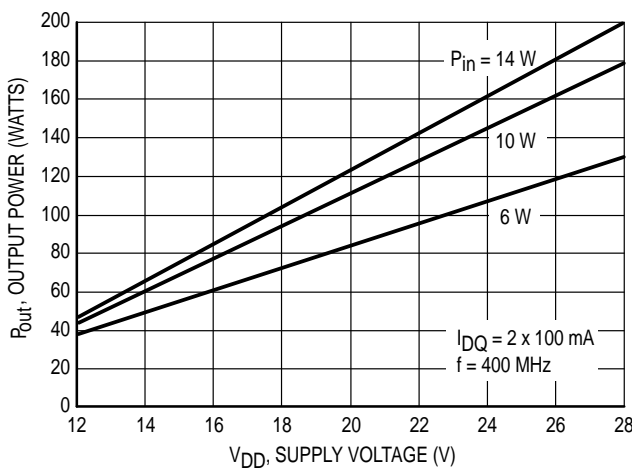
**Figure 3. Output Power versus Gate Voltage**



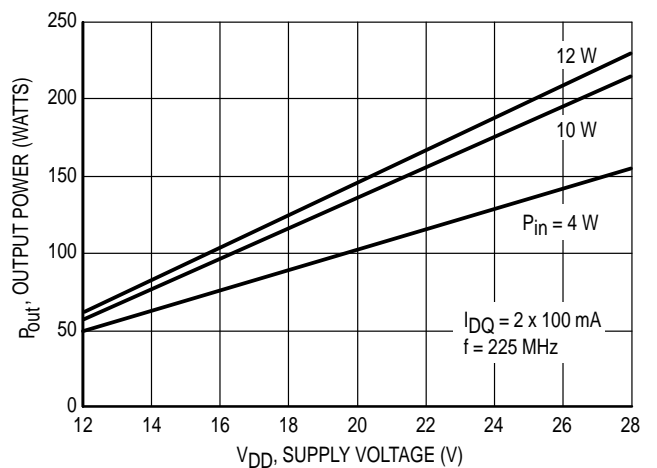
**Figure 4. Drain Current versus Gate Voltage (Transfer Characteristics)**



**Figure 5. Output Power versus Supply Voltage**

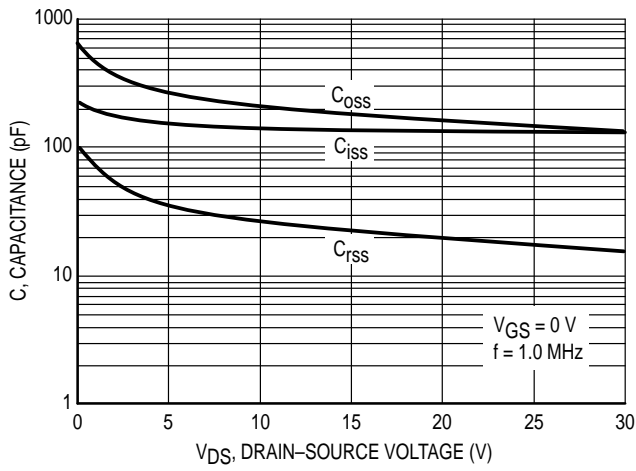


**Figure 6. Output Power versus Supply Voltage**

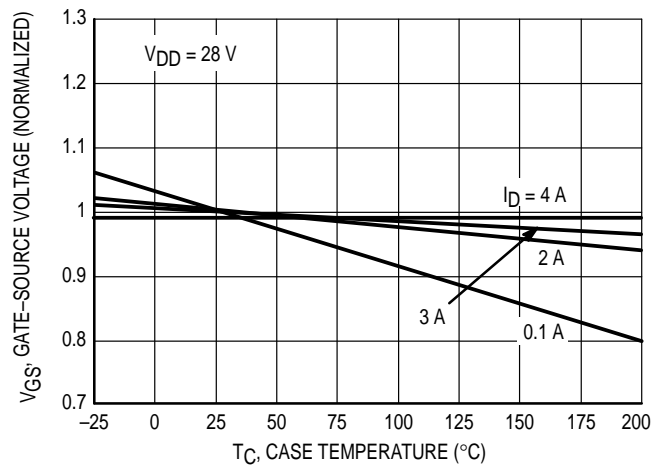


**Figure 7. Output Power versus Supply Voltage**

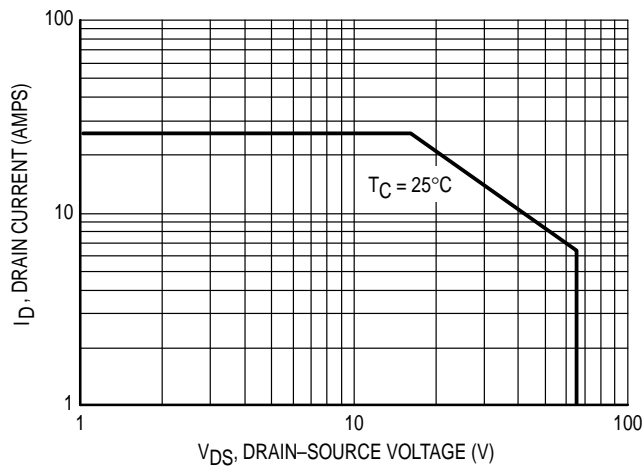
## TYPICAL CHARACTERISTICS



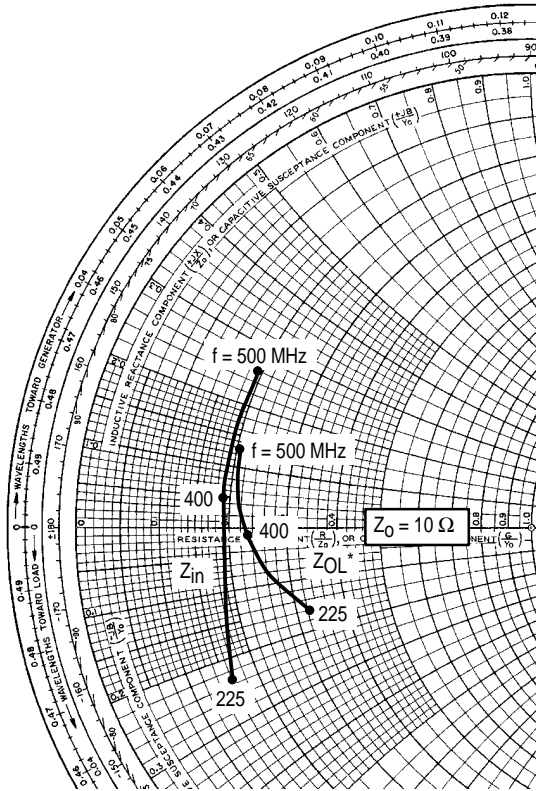
**Figure 8. Capacitance versus Drain-Source Voltage\***  
 \*Data shown applies only to one half of device, MRF275G



**Figure 9. Gate-Source Voltage versus Case Temperature**



**Figure 10. DC Safe Operating Area**



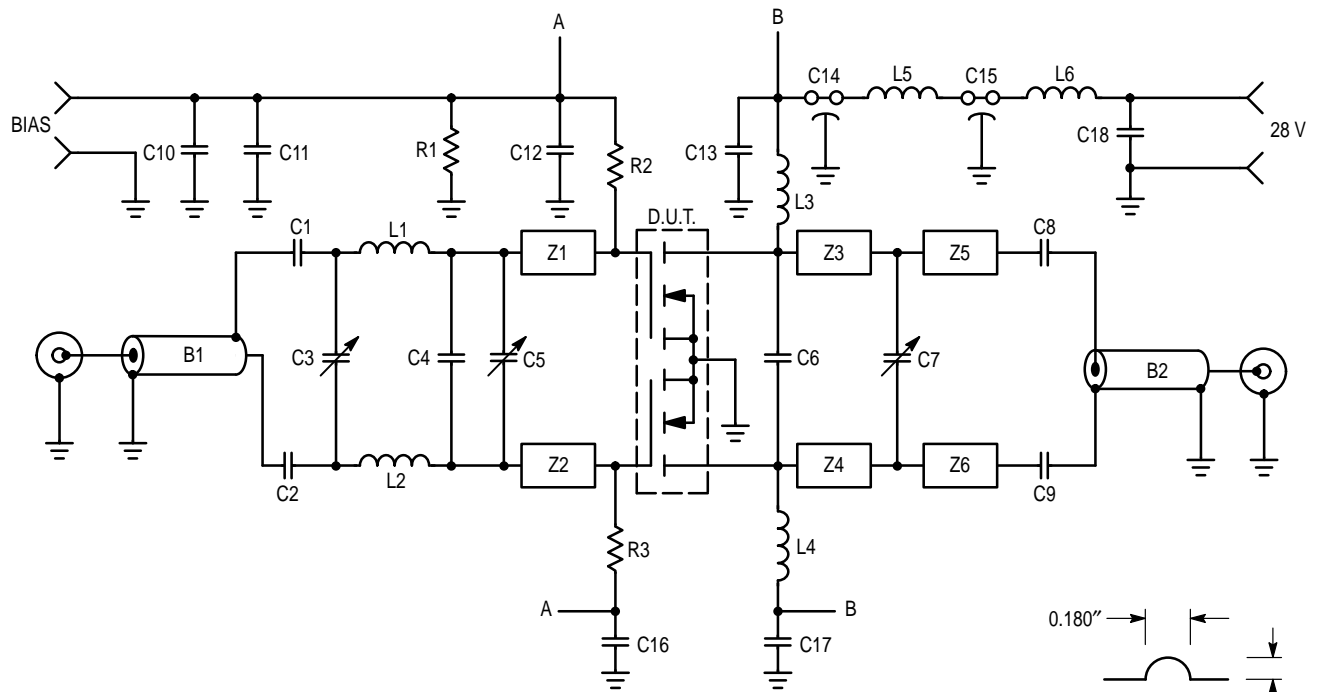
$V_{DD} = 28 \text{ V}$ ,  $I_{DQ} = 2 \times 100 \text{ mA}$ ,  $P_{out} = 150 \text{ W}$

f (MHz)	$Z_{in}$ Ohms	$Z_{OL}^*$ Ohms
225	$1.6 - j2.30$	$3.2 - j1.50$
400	$1.9 + j0.48$	$2.3 - j0.19$
500	$1.9 + j2.60$	$2.0 + j1.30$

$Z_{OL}^*$  = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

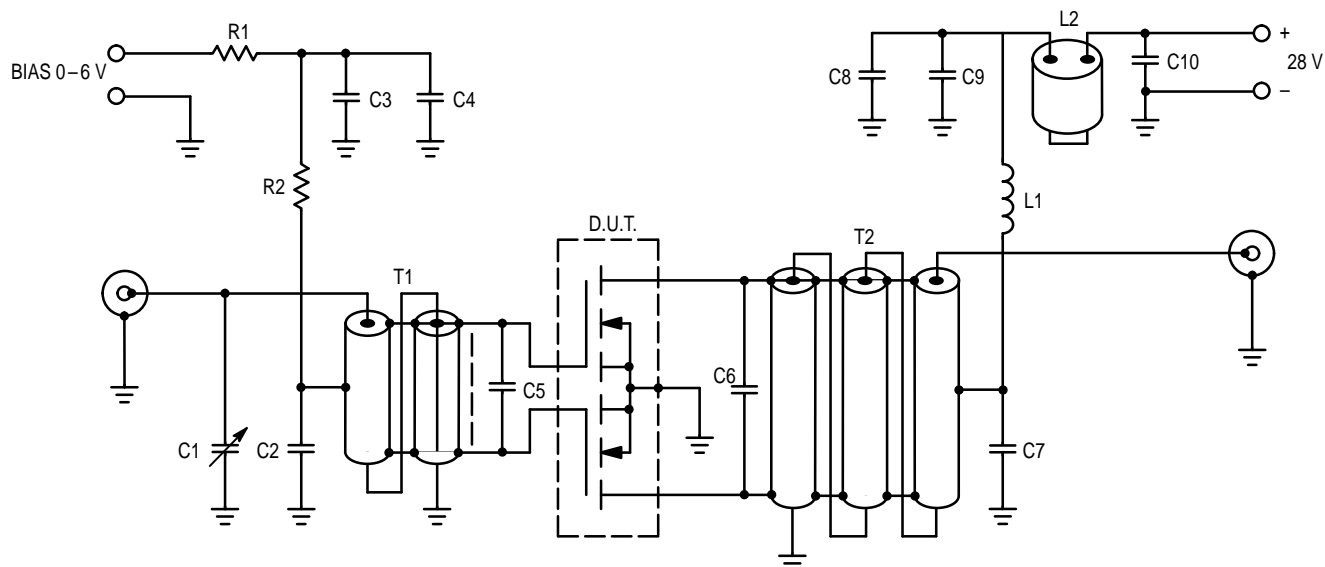
Note: Input and output impedance values given are measured from gate to gate and drain to drain respectively.

Figure 11. Series Equivalent Input/Output Impedance



B1	Balun, 50 $\Omega$ , 0.086" O.D. 2" Long, Semi Rigid Coax	L1, L2	#18 Wire, Hairpin Inductor
B2	Balun, 50 $\Omega$ , 0.141" O.D. 2" Long, Semi Rigid Coax	L3, L4	12 Turns #18, 0.340" I.D., Enameled Wire
C1, C2, C8, C9	270 pF, ATC Chip Capacitor	L5	Ferroxcube VK200 20/4B
C3, C5, C7	1.0–20 pF, Trimmer Capacitor	L6	3 Turns #16, 0.340" I.D., Enameled Wire
C4	15 pF, ATC Chip Capacitor	R1	1.0 k $\Omega$ , 1/4 W Resistor
C6	33 pF, ATC Chip Capacitor	R2, R3	10 k $\Omega$ , 1/4 W Resistor
C10, C12, C13, C16, C17	0.01 $\mu$ F, Ceramic Capacitor	Z1, Z2	0.400" x 0.250", Microstrip Line
C11	1.0 $\mu$ F, 50 V, Tantalum	Z3, Z4	0.870" x 0.250", Microstrip Line
C14, C15	680 pF, Feedthru Capacitor	Z5, Z6	0.500" x 0.250", Microstrip Line
C18	20 $\mu$ F, 50 V, Tantalum	Board material	0.060" Teflon–fiberglass, $\epsilon_r = 2.55$ , copper clad both sides, 2 oz. copper.

**Figure 12. 400 MHz Test Circuit**



C1	8.0–60 pF, Arco 404	R1	100 $\Omega$ , 1/2 W
C2, C3, C7, C8	1000 pF, Chip Capacitor	R2	1.0 k $\Omega$ , 1/2 W
C4, C9	0.1 $\mu$ F, Chip Capacitor	T1	4:1 Impedance Ratio, RF Transformer Can Be Made of 25 $\Omega$ , Semi Rigid Coax, 47–52 Mils O.D.
C5	180 pF, Chip Capacitor	T2	1:9 Impedance Ratio, RF Transformer. Can Be Made of 15–18 $\Omega$ , Semi Rigid Coax, 62–90 Mils O.D.
C6	100 pF and 130 pF, Chips in Parallel		
C10	0.47 $\mu$ F, Chip Capacitor, 1215 or Equivalent, Kemet		
L1	10 Turns AWG #16, 1/4" I.D., Enamel Wire, Close Wound		
L2	Ferrite Beads of Suitable Material for 1.5–2.0 $\mu$ H Total Inductance		

NOTE: For stability, the input transformer T1 should be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

Board material 062" fiberglass (G10),  
 $\epsilon_r \approx 5$ , Two sided, 1 oz. Copper.  
 Unless otherwise noted, all chip capacitors  
 are ATC Type 100 or Equivalent.

**Figure 13. 225 MHz Test Circuit**



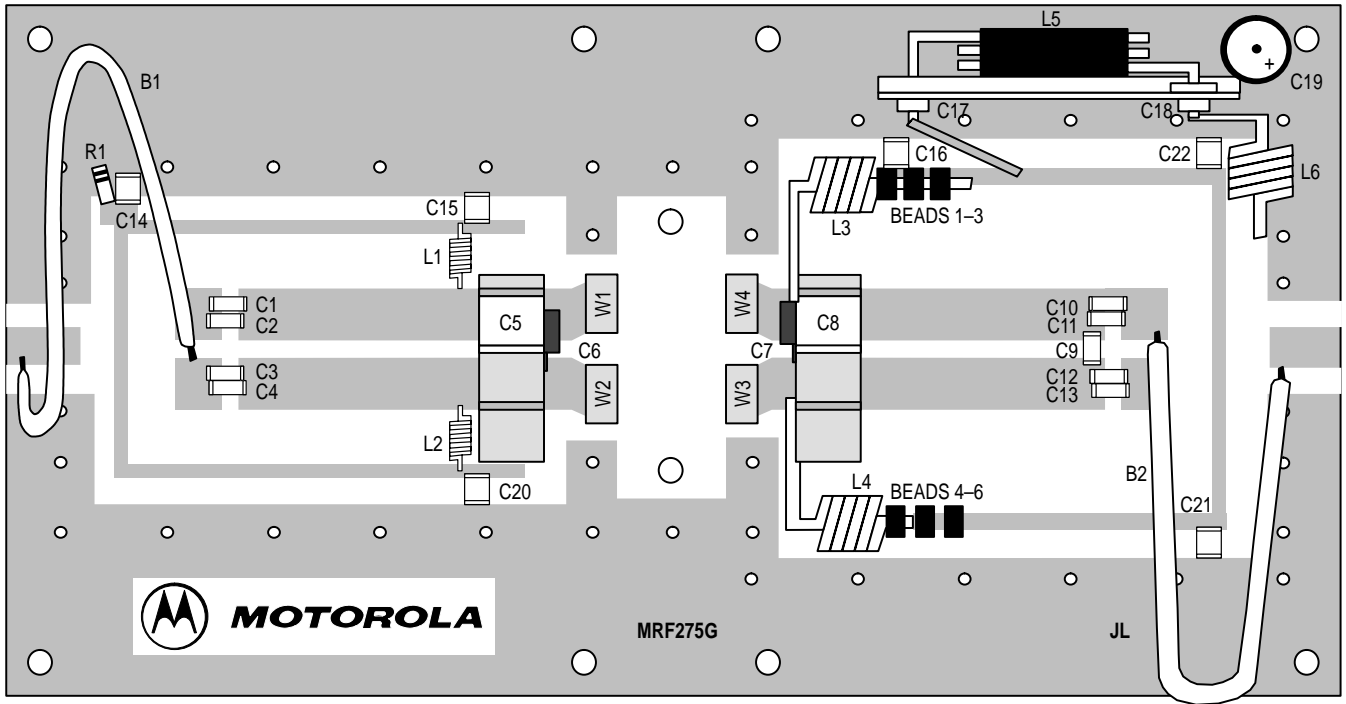


Figure 14. MRF275G Component Location (500 MHz)  
(Not to Scale)

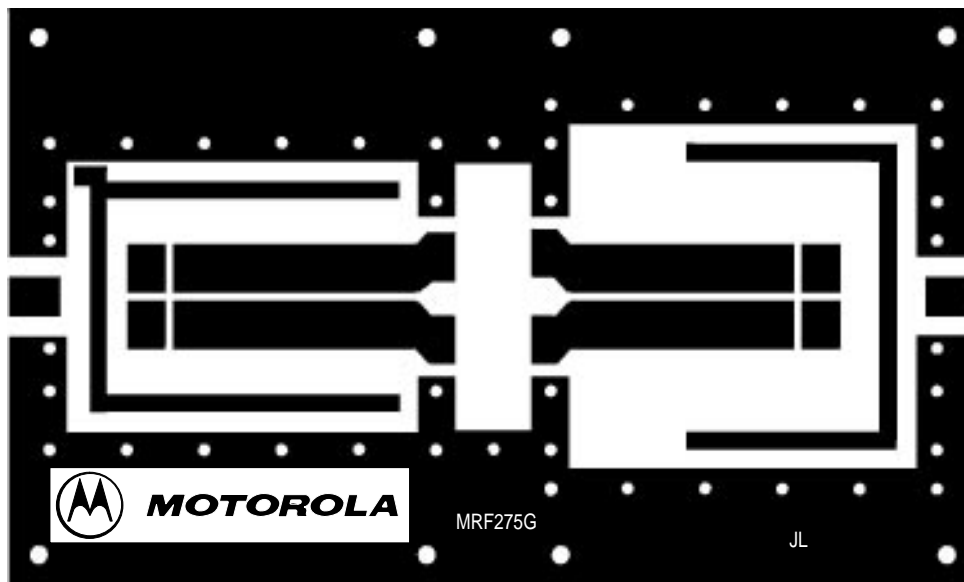


Figure 15. MRF275G Circuit Board Photo Master (500 MHz) Scale 1:1  
(Reduced 25% in printed data book, DL110/D)

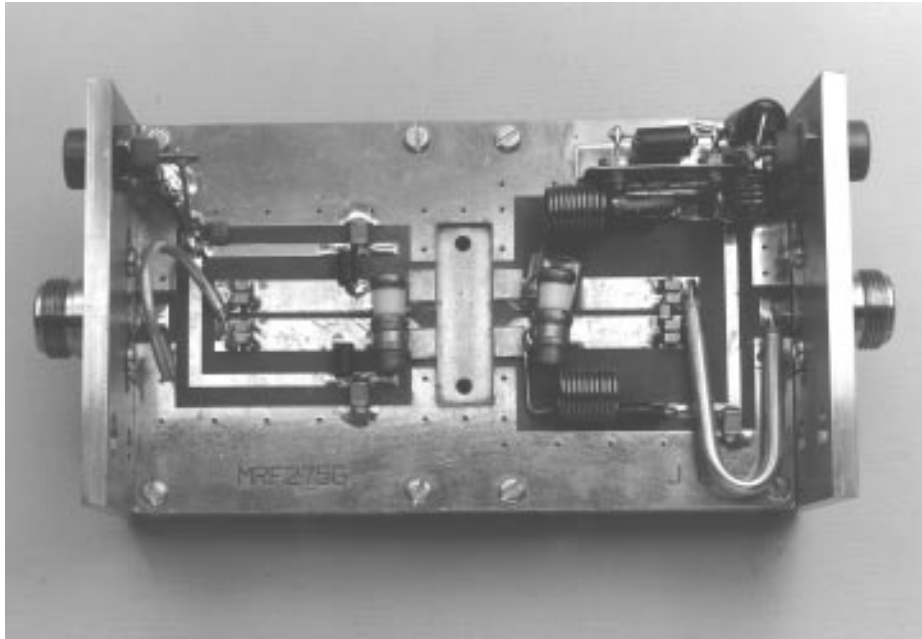


Figure 16. MRF275G Test Fixture

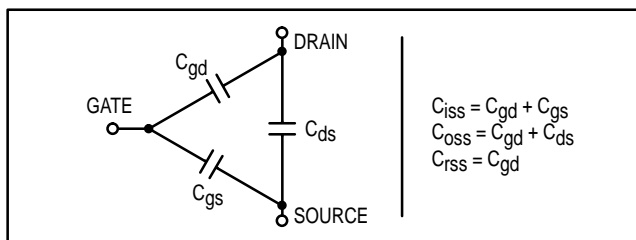
## RF POWER MOSFET CONSIDERATIONS

### MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain ( $C_{gd}$ ), and gate-to-source ( $C_{gs}$ ). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain-to-source ( $C_{ds}$ ).

These capacitances are characterized as input ( $C_{iSS}$ ), output ( $C_{oSS}$ ) and reverse transfer ( $C_{rSS}$ ) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The  $C_{iSS}$  can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



The  $C_{iSS}$  given in the electrical characteristics table was measured using method 2 above. It should be noted that  $C_{iSS}$ ,  $C_{oSS}$ ,  $C_{rSS}$  are measured at zero drain current and are

provided for general information about the device. They are not RF design parameters and no attempt should be made to use them as such.

### LINEARITY AND GAIN CHARACTERISTICS

In addition to the typical IMD and power gain, data presented in Figure 3 may give the designer additional information on the capabilities of this device. The graph represents the small signal unity current gain frequency at a given drain current level. This is equivalent to  $f_T$  for bipolar transistors. Since this test is performed at a fast sweep speed, heating of the device does not occur. Thus, in normal use, the higher temperatures may degrade these characteristics to some extent.

### DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full-on condition. This on-resistance,  $V_{DS(on)}$ , occurs in the linear region of the output characteristic and is specified under specific test conditions for gate-source voltage and drain current. For MOSFETs,  $V_{DS(on)}$  has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

### GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of  $10^9$  ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate-to-source threshold voltage,  $V_{GS(th)}$ .

**Gate Voltage Rating** — Never exceed the gate voltage rating (or any of the maximum ratings on the front page). Exceeding the rated  $V_{GS}$  can result in permanent damage to the oxide layer in the gate region.

**Gate Termination** — The gates of this device are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

**Gate Protection** — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

#### HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with grounded equipment.

#### DESIGN CONSIDERATIONS

The MRF275G is a RF power N-channel enhancement mode field-effect transistor (FETs) designed for HF, VHF and UHF power amplifier applications. Motorola RF MOSFETs feature a vertical structure with a planar design.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

#### DC BIAS

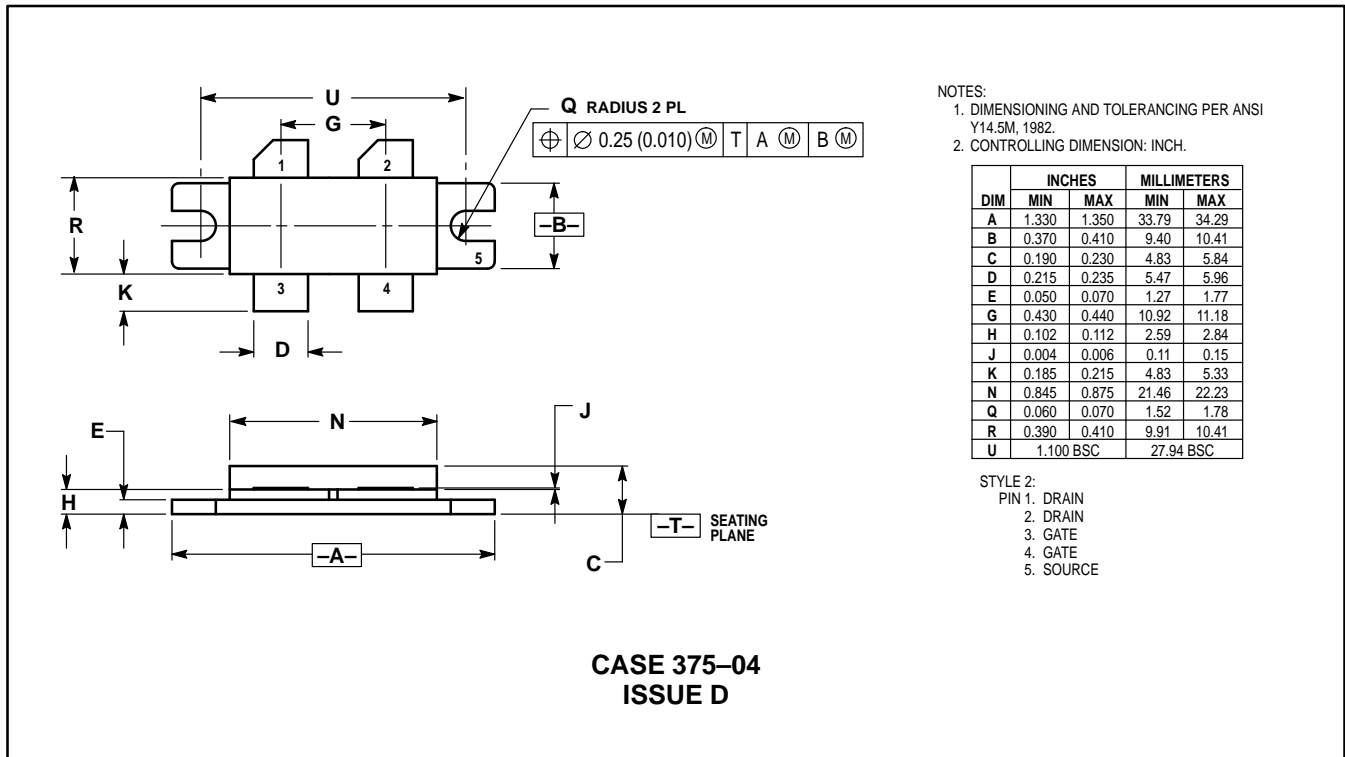
The MRF275G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current ( $I_{DQ}$ ) is not critical for many applications. The MRF275G was characterized at  $I_{DQ} = 100$  mA, each side, which is the suggested minimum value of  $I_{DQ}$ . For special applications such as linear amplification,  $I_{DQ}$  may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

#### GAIN CONTROL

Power output of the MRF275G may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

## PACKAGE DIMENSIONS



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.330	1.350	33.79	34.29
B	0.370	0.410	9.40	10.41
C	0.190	0.230	4.83	5.84
D	0.215	0.235	5.47	5.96
E	0.050	0.070	1.27	1.77
G	0.430	0.440	10.92	11.18
H	0.102	0.112	2.59	2.84
J	0.004	0.006	0.11	0.15
K	0.185	0.215	4.83	5.33
N	0.845	0.875	21.46	22.23
Q	0.060	0.070	1.52	1.78
R	0.390	0.410	9.91	10.41
U	1.100 BSC		27.94 BSC	

- STYLE 2:  
 PIN 1. DRAIN  
 2. DRAIN  
 3. GATE  
 4. GATE  
 5. SOURCE

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