

The RF Sub-Micron MOSFET Line

RF Power Field Effect Transistors

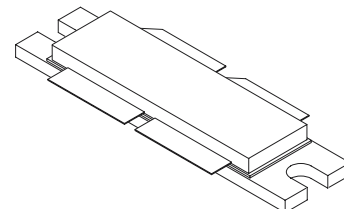
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

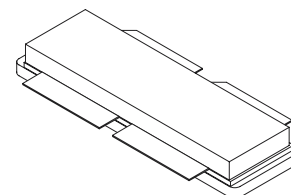
- Typical CDMA Performance @ 880 MHz, 26 Volts, $I_{DQ} = 2 \times 700$ mA
IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
Output Power — 40 Watts
Power Gain — 17 dB
Efficiency — 26%
Adjacent Channel Power —
750 kHz: -45.0 dBc @ 30 kHz BW
1.98 MHz: -60.0 dBc @ 30 kHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 170 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

MRF9180
MRF9180S

880 MHz, 170 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 375D-04, STYLE 1
NI-1230
MRF9180



CASE 375E-03, STYLE 1
NI-1230S
MRF9180S

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	388 2.22	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +200	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.45	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 300\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	2	2.9	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 700\text{ mAdc}$)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 2\text{ Adc}$)	$V_{DS(on)}$	—	0.19	0.5	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 6\text{ Adc}$)	g_{fs}	—	6	—	S
DYNAMIC CHARACTERISTICS (1)					
Output Capacitance ($V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	77	—	pF
Reverse Transfer Capacitance ($V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	3.8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2)					
Two–Tone Common–Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W PEP}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	G_{ps}	16	17.5	—	dB
Two–Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W PEP}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	η	35	39	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W PEP}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	IMD	—	–31	–28	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W PEP}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	IRL	—	–15	–9	dB
Two–Tone Common–Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W PEP}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	G_{ps}	—	17.5	—	dB
Two–Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W PEP}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	η	—	38.5	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W PEP}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	IMD	—	–31	—	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W PEP}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	IRL	—	–13	—	dB
Power Output, 1 dB Compression Point ($V_{DD} = 26\text{ Vdc}$, CW, $I_{DQ} = 2 \times 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	P_{1dB}	—	170	—	W

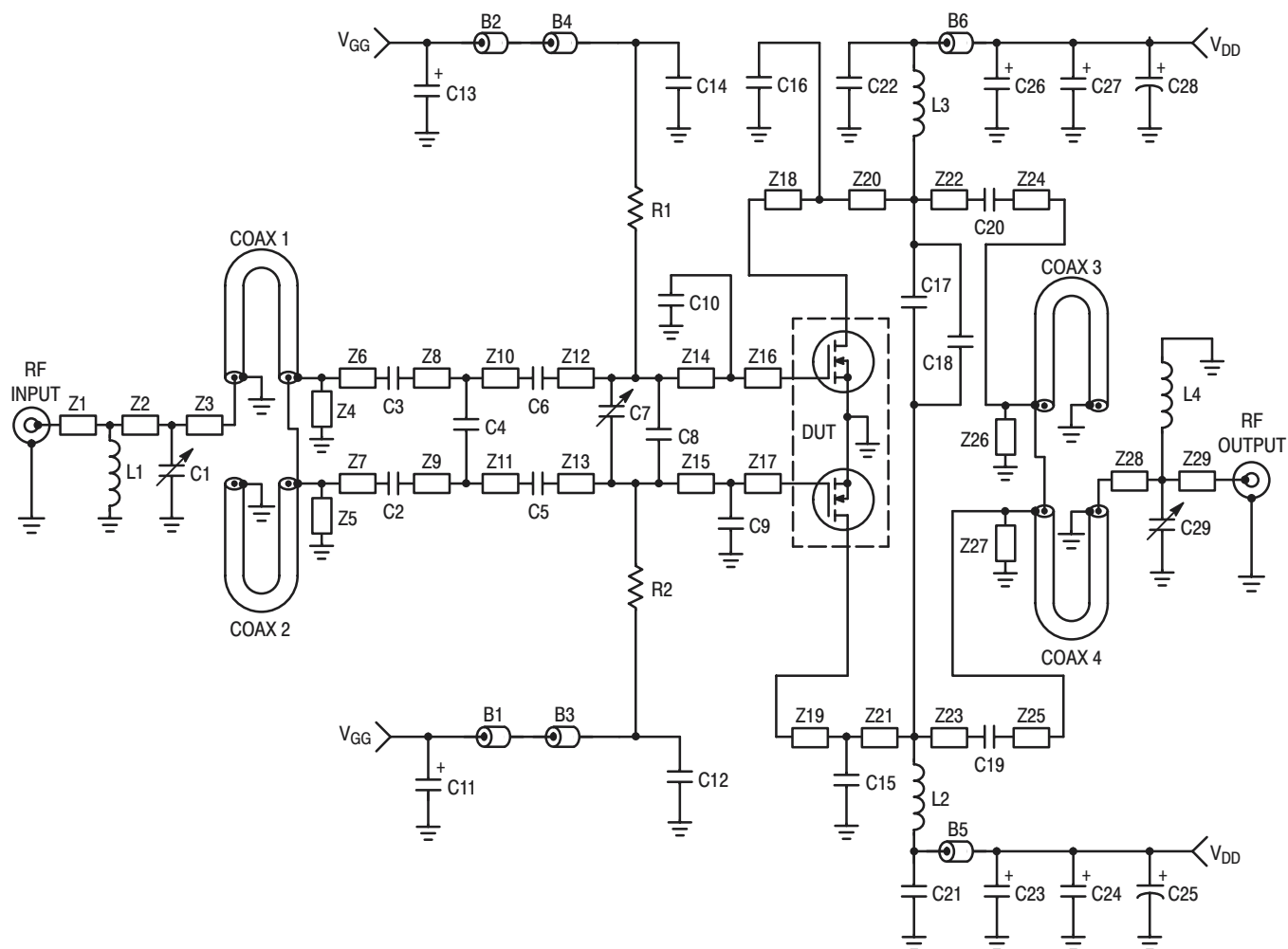
(1) Each side of device measured separately.

(2) Device measured in push–pull configuration.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2) (continued)					
Common–Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W CW}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	G_{ps}	—	16.5	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W CW}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	η	—	55	—	%
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 170\text{ W CW}$, $I_{DQ} = 2 \times 700\text{ mA}$, $f = 880\text{ MHz}$, $VSWR = 10:1$, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(2) Device measured in push–pull configuration.



B1, B2, B5, B6	Long Ferrite Beads, Surface Mount	Z1	0.420" x 0.080" Microstrip
B3, B4	Short Ferrite Beads, Surface Mount	Z2	0.190" x 0.080" Microstrip
C1	0.6–4.5 pF Variable Capacitor	Z3	0.097" x 0.080" Microstrip
C2, C3, C5, C6, C12, C14, C19, C20, C21, C22	47 pF Chip Capacitors, B Case	Z4, Z5, Z26, Z27	2.170" x 0.080" Microstrip
C4, C9, C10, C15, C16	12 pF Chip Capacitors, B Case	Z6, Z7	0.075" x 0.080" Microstrip
C7	0.8–9.1 pF Variable Capacitor	Z8, Z9	0.088" x 0.220" Microstrip
C8	7.5 pF Chip Capacitor, B Case	Z10, Z11	0.088" x 0.220" Microstrip
C11, C13	10 μ F, 35 V Tantalum Surface Mount Chip Capacitors	Z12, Z13	0.460" x 0.220" Microstrip
C17	3.6 pF Chip Capacitor, B Case	Z14, Z15	0.685" x 0.625" Microstrip
C18	5.1 pF Chip Capacitor, B Case	Z16, Z17	0.055" x 0.625" Microstrip
C23, C24, C26, C27	22 μ F, 35 V Tantalum Surface Mount Chip Capacitors	Z18, Z19	0.055" x 0.632" Microstrip
C25, C28	220 μ F, 50 V Electrolytic Capacitors	Z20, Z21	0.685" x 0.632" Microstrip
C29	0.4–2.5 pF Variable Capacitor	Z22, Z23	0.732" x 0.080" Microstrip
Coax1, Coax2	25 Ω , Semi Rigid Coax, 70 mil OD, 1.05" Long	Z24, Z25	0.060" x 0.080" Microstrip
Coax3, Coax4	50 Ω , Semi Rigid Coax, 85 mil OD, 1.05" Long	Z28	0.230" x 0.080" Microstrip
L1, L2, L3	18.5 nH Mini Spring Inductors, Coilcraft	Z29	0.460" x 0.080" Microstrip
L4	12.5 nH Mini Spring Inductor, Coilcraft	Board	30 mil Teflon [®] , $\epsilon_r = 2.55$,
R1, R2	510 Ω , 1/10 W Chip Resistors	Material	Copper Clad, 2 oz Cu

Figure 1. 880 MHz Broadband Test Circuit Schematic

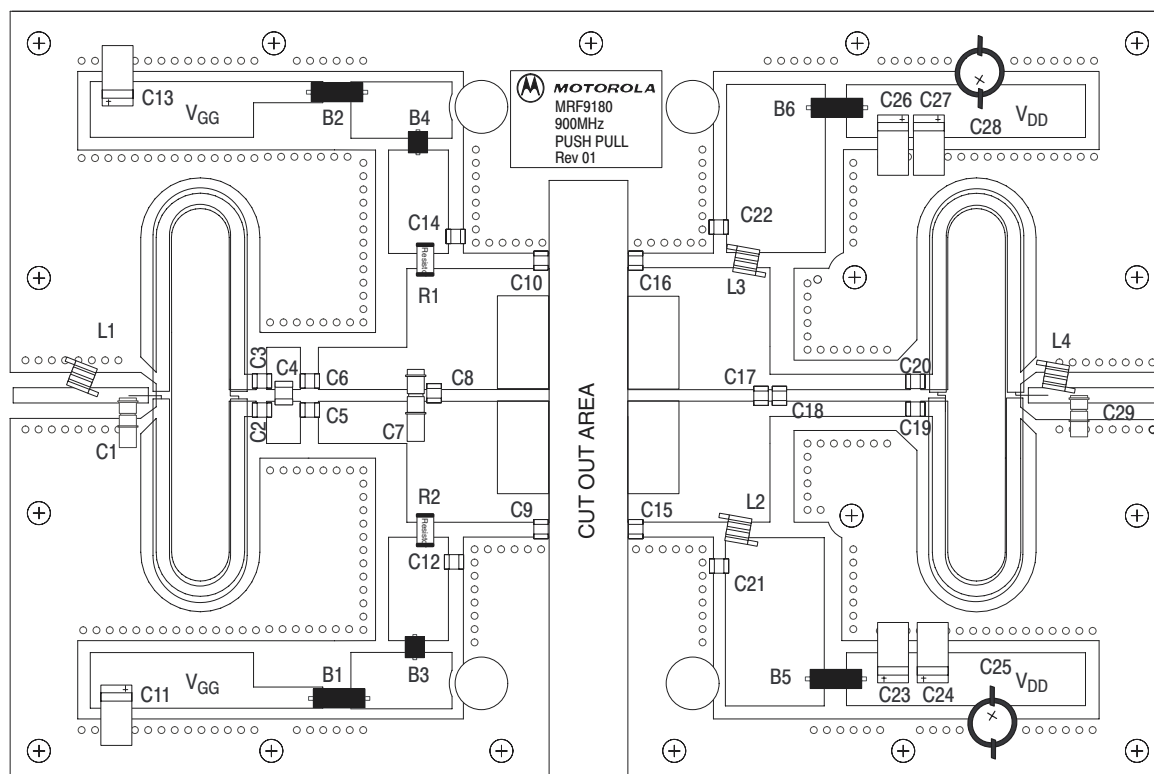


Figure 2. 880 MHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

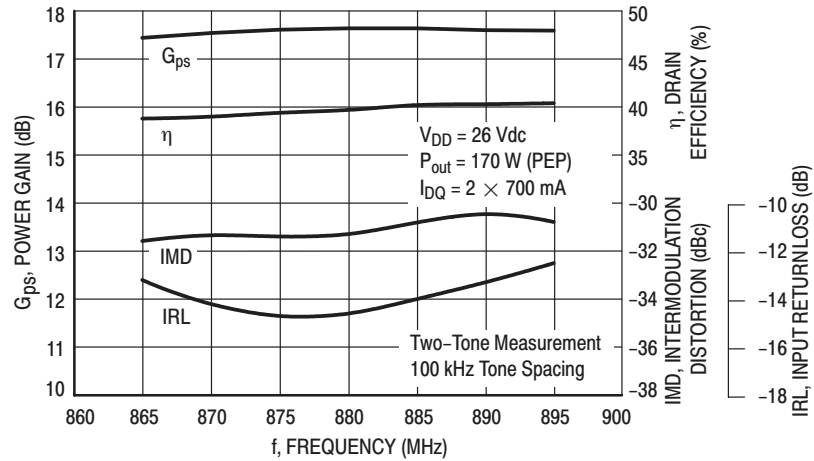


Figure 3. Class AB Broadband Circuit Performance

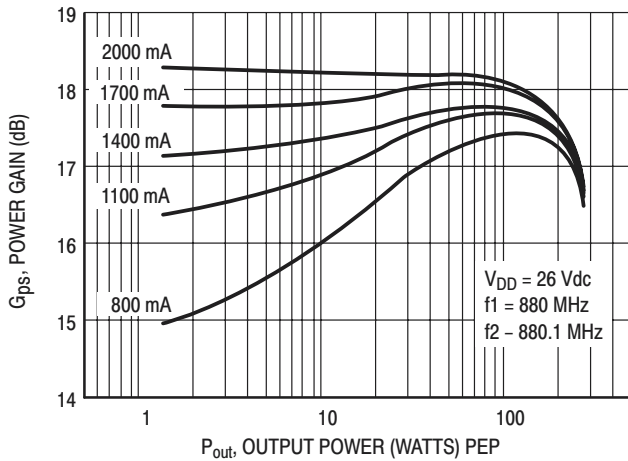


Figure 4. Power Gain versus Output Power

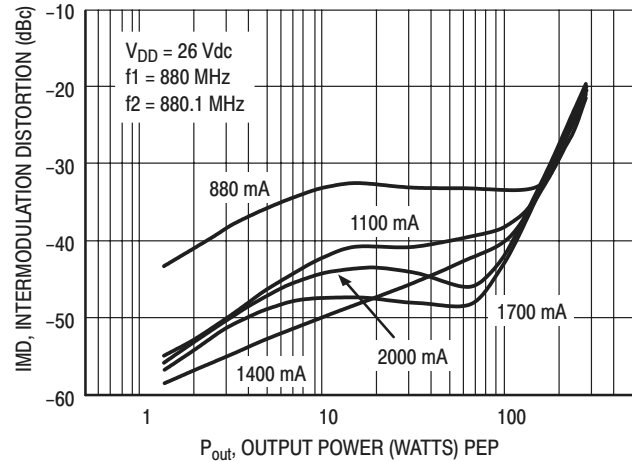


Figure 5. Intermodulation Distortion versus Output Power

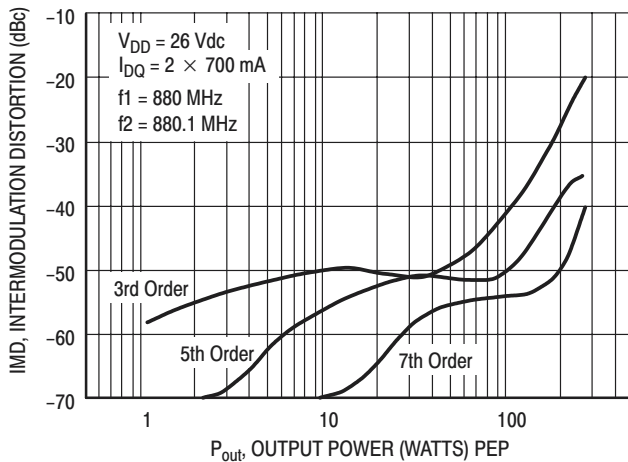


Figure 6. Intermodulation Distortion Products versus Output Power

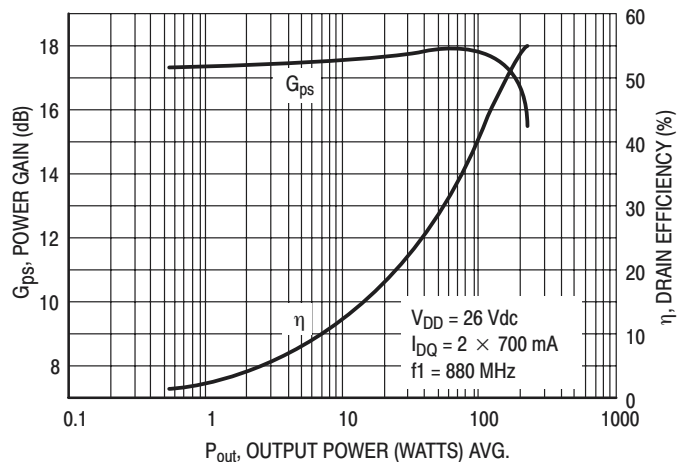


Figure 7. Power Gain and Efficiency versus Output Power

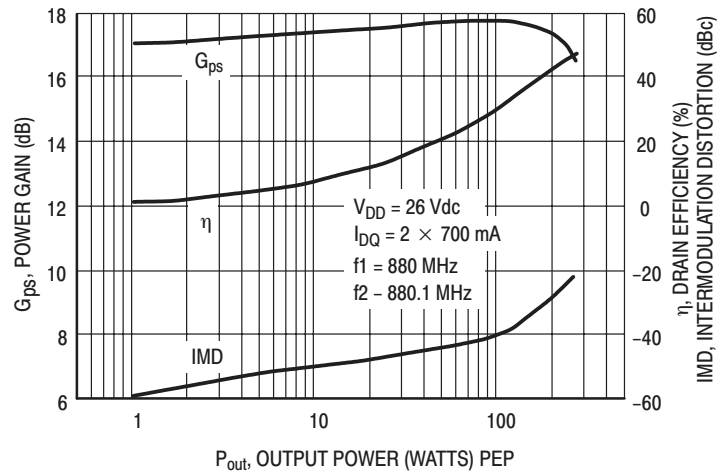


Figure 8. Power Gain, Efficiency and IMD versus Output Power

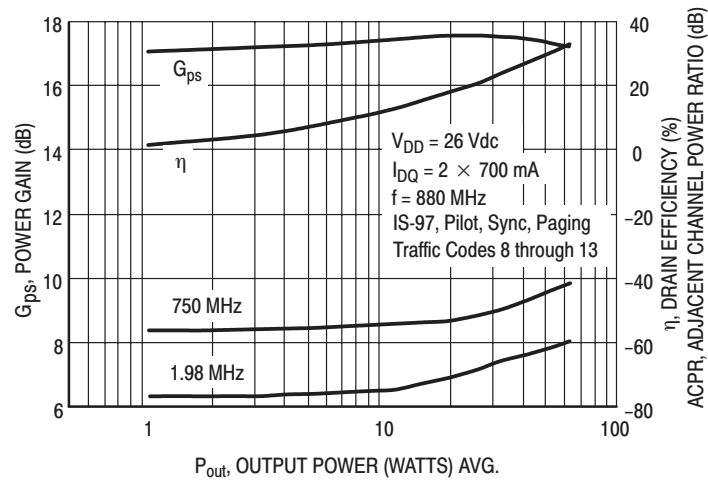
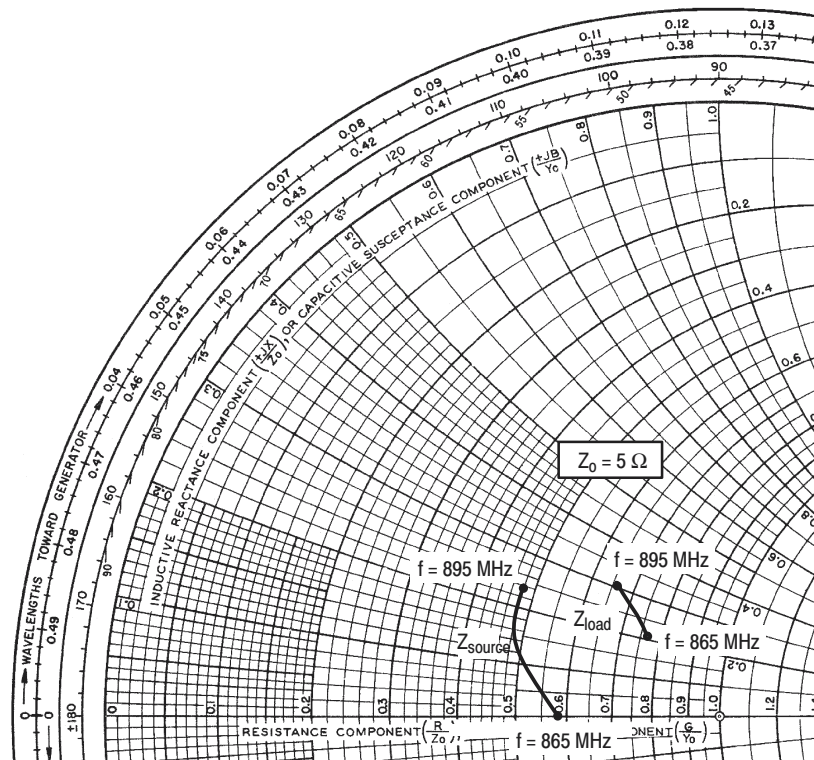


Figure 9. Power Gain, Efficiency and ACPR versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 2 \times 700 \text{ mA}$, $P_{\text{out}} = 170 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
865	$2.95 + j0.00$	$3.83 + j1.02$
880	$2.48 + j0.67$	$3.55 + j1.38$
895	$2.44 + j1.18$	$3.34 + j1.51$

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

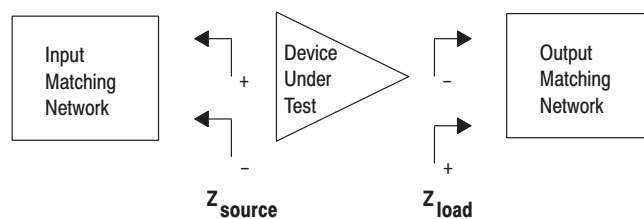
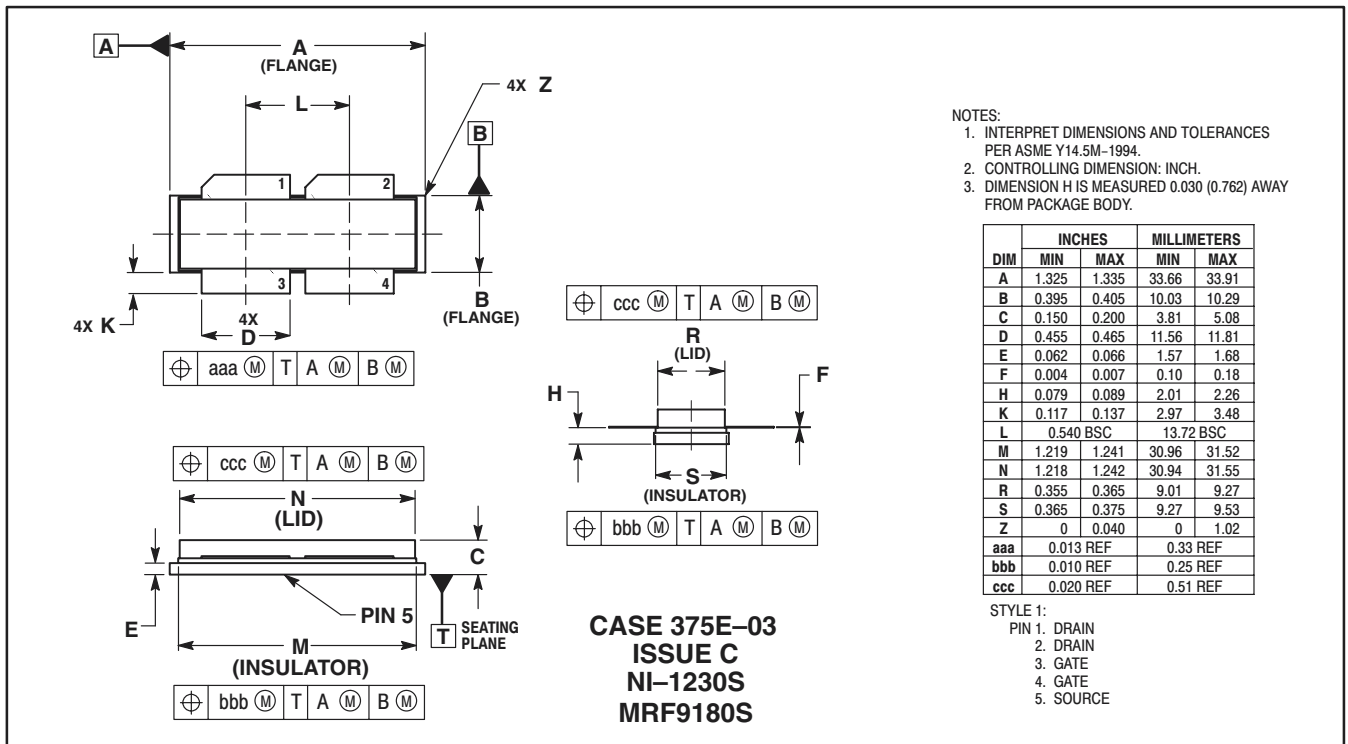
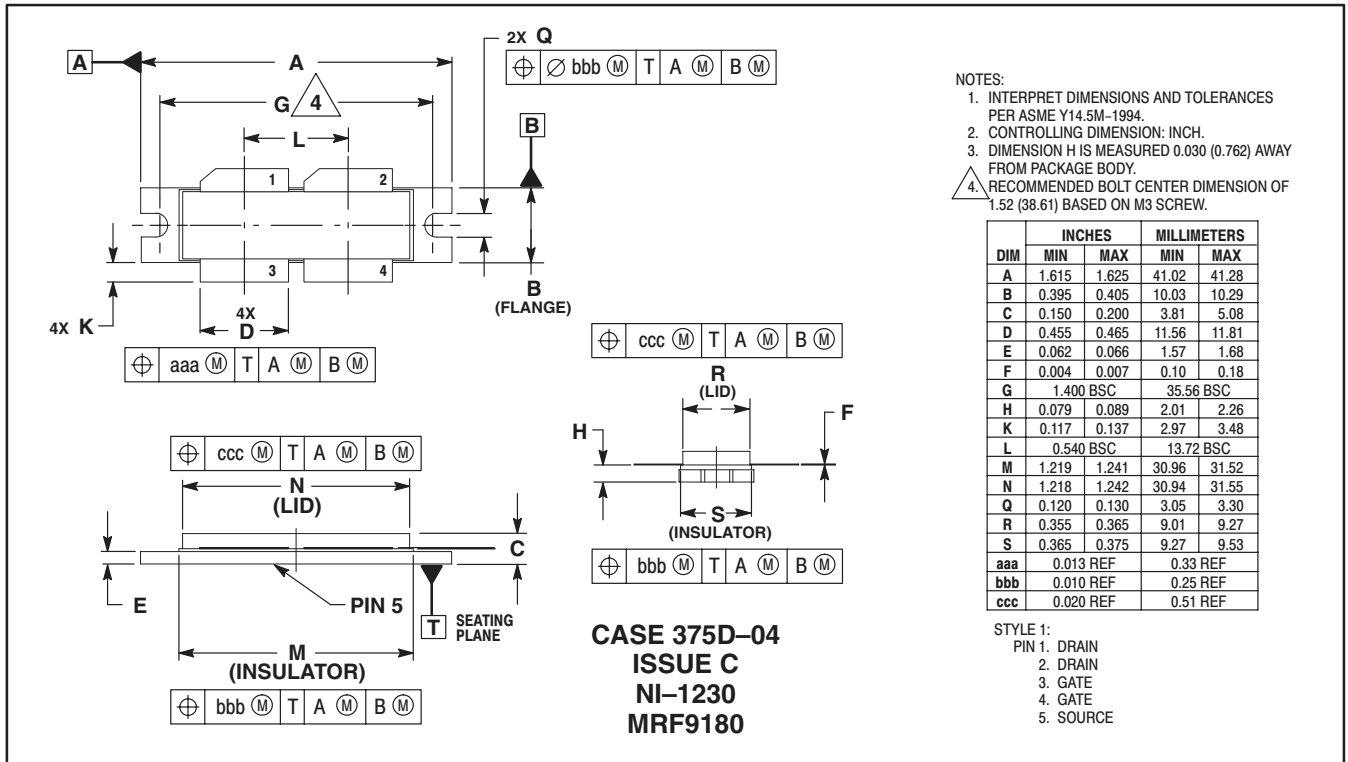


Figure 10. Series Equivalent Input and Output Impedance

NOTES

NOTES

PACKAGE DIMENSIONS



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How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140 or 1-800-441-2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3-20-1, Minami-Azabu. Minato-ku, Tokyo 106-8573 Japan. 81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852-26668334

Technical Information Center: 1-800-521-6274

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