MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTD2955E

Motorola Preferred Device

Designer's Data Sheet

Power Field Effect Transistor

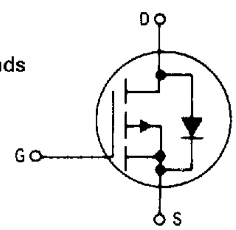
P-Channel Enhancement-Mode Silicon Gate DPAK for Surface Mount or Insertion Mount

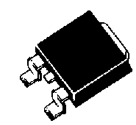
TMOS POWER FET
12 AMPERES
$R_{DS(on)}$ = 0.3 OHM
60 VOLTS

3

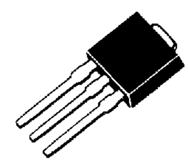
This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $R_{DS(on)}$ — 0.3 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4.0 V max
- Surface Mount Package Available on 16 mm Tape
- Available With Long Leads, Add -1 Suffix





CASE 369A-10
MTD2955E



CASE 369-06
MTD2955E-1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 26	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 0.01	Watts W/°C
Total Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.67	°C/W
— Junction to Ambient — Junction to Ambient (1)	$R_{\theta JA}$	100 71.4	

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

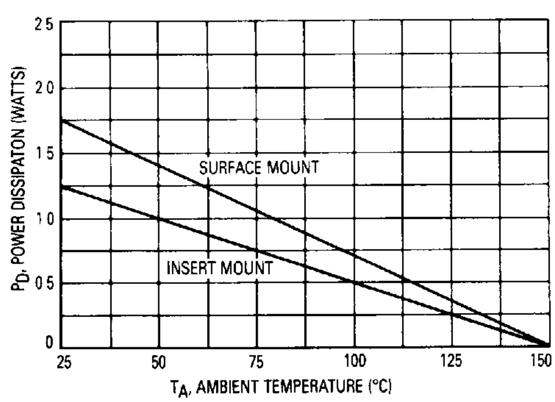
Preferred device is a Motorola recommended choice for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	10	μAdc
(T_J = 125°C)			—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)		$V_{GS(th)}$	2.0	4 5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$R_{DS(on)}$	—	0.3	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 12 Adc)		$V_{DS(on)}$	—	3.9	Vdc
(I_D = 6.0 Adc, T_J = 100°C)			—	3.2	
Forward Transconductance (V_{DS} = 10 V, I_D = 6.0 A)		g_{FS}	3 0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz) See Figure 13	C_{iss}	600 (Typ)	—	pF
Output Capacitance		C_{oss}	300 (Typ)	—	
Reverse Transfer Capacitance		C_{rss}	135 (Typ)	—	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 6.0 A, R_g = 50 ohms) See Figures 10, 14 and 15	$t_{d(on)}$	10 (Typ)	—	ns
Rise Time		t_r	75 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	75 (Typ)	—	
Fall Time		t_f	50 (Typ)	—	
Total Gate Charge	(V_{DS} = 48 V, I_D = 12 A, V_{GS} = 10 V) See Figure 12	Q_g	26 (Typ)	45	nC
Gate-Source Charge		Q_{gs}	7 (Typ)	—	
Gate-Drain Charge		Q_{gd}	15 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	I_S = 12 A, V_{GS} = 0	V_{SD}	3 0 (Typ)	3.8	Vdc
Forward Turn-On Time	I_S = 12 A, dI_S/dt = 100 A/μs, V_R = 30 V	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	110 (Typ)	—	ns

*Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

Figure 1. Power Derating



TYPICAL ELECTRICAL CHARACTERISTICS

Figure 2. On-Region Characteristics

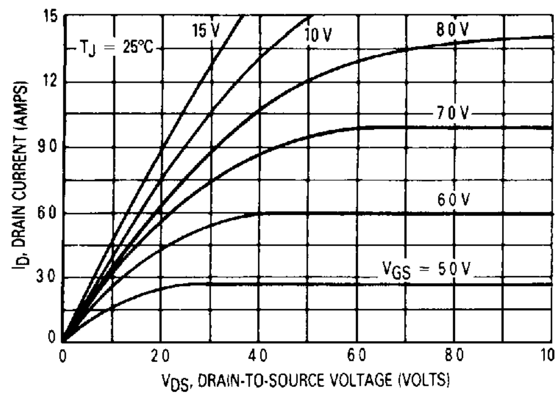


Figure 3. Gate Threshold Variation With Temperature

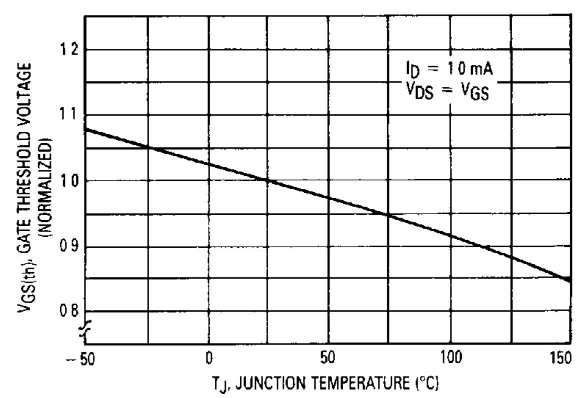


Figure 4. Transfer Characteristics

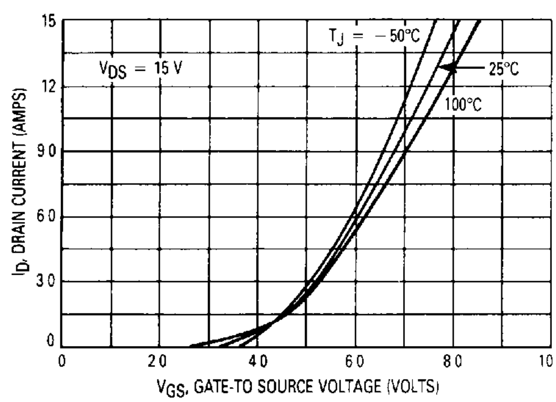


Figure 5. Breakdown Voltage Variation With Temperature

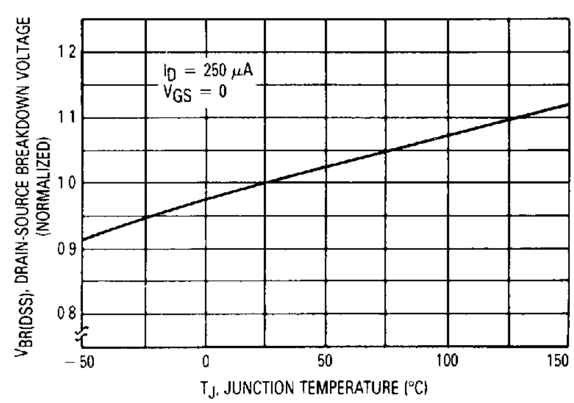


Figure 6. On-Resistance Variation With Drain Current

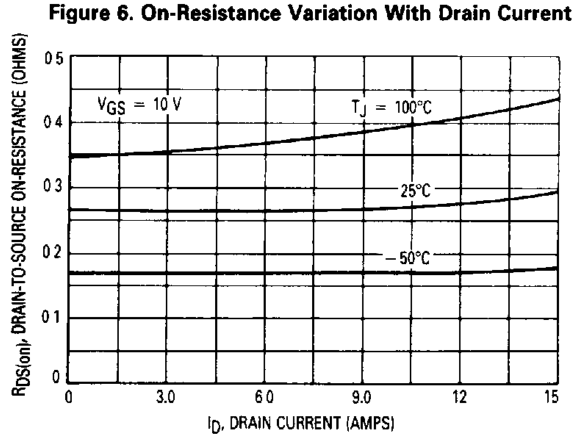


Figure 7. On-Resistance Variation With Temperature

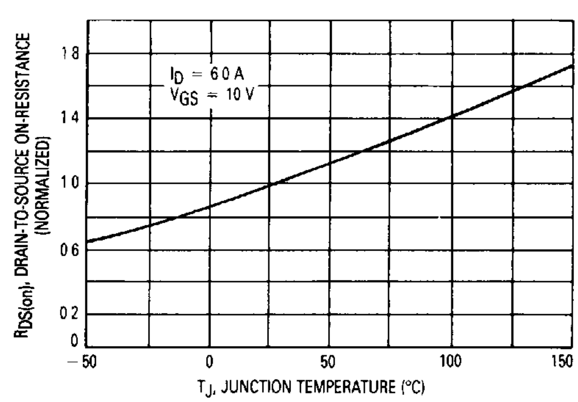


Figure 8. Maximum Rated Forward Biased Safe Operating Area

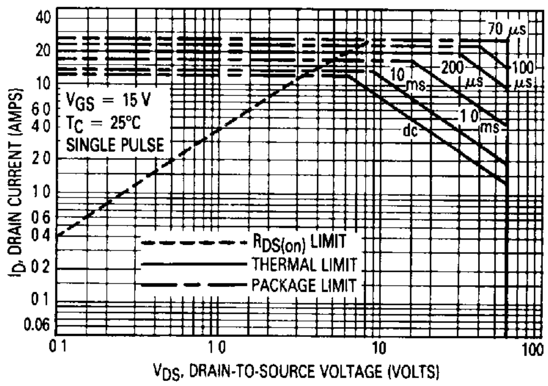
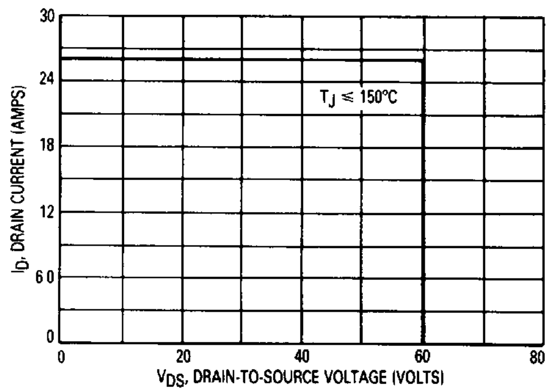


Figure 9. Maximum Rated Switching Safe Operating Area



3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 10. Resistive Switching Time versus Gate Resistance

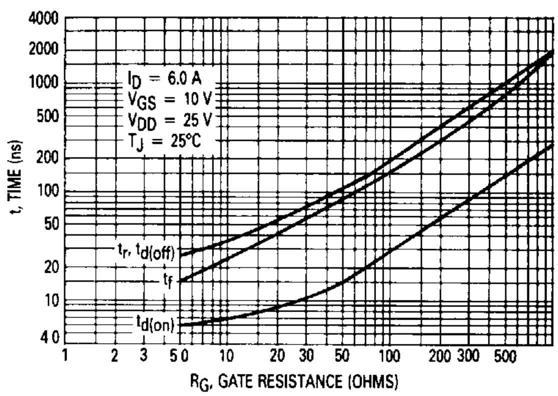


Figure 11. Thermal Response

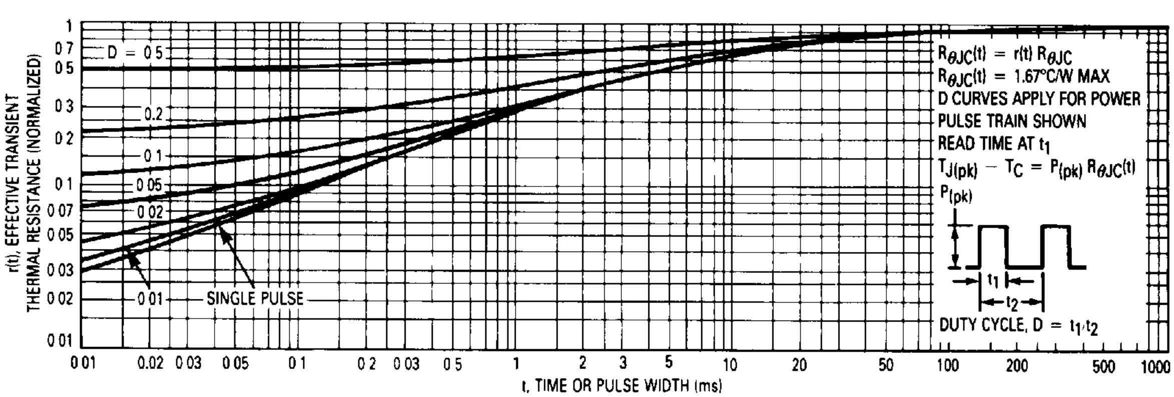


Figure 12. Gate Charge versus Gate-To-Charge Voltage

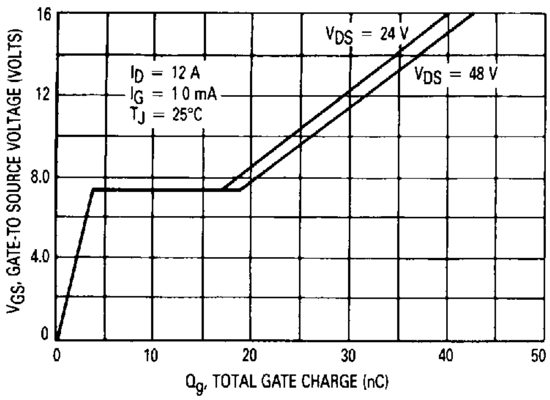
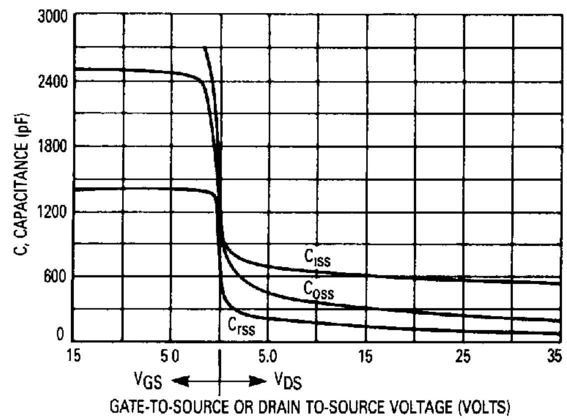


Figure 13. Capacitance Variation With Voltage



RESISTIVE SWITCHING

Figure 14. Switching Test Circuit

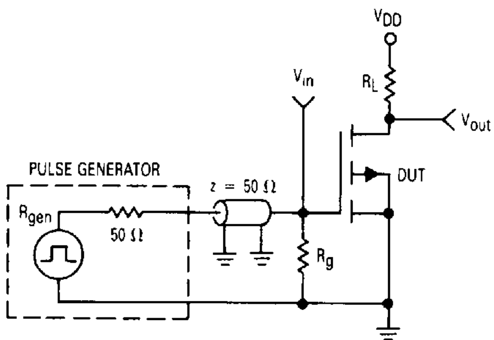


Figure 15. Switching Waveforms