

T-39-15

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Designer's Data Sheet
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

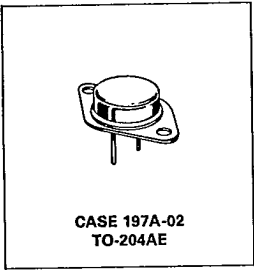
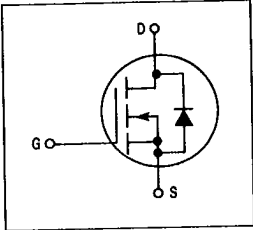
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTM15N45
MTM15N50

TMOS POWER FETs
15 AMPERES
 $r_{DS(on)} = 0.4 \text{ OHM}$
450 and 500 VOLTS



MAXIMUM RATINGS

Rating	Symbol	MTM		Unit
		15N45	15N50	
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	450	500	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50 \mu s$)	V_{GS}	± 20		Vdc
	V_{GSM}	± 40		Vpk
Drain Current — Continuous — Pulsed	I_D	15		Adc
	I_{DM}	65		
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	250		Watts
		2		$W/^\circ C$
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		$^\circ C$

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$	0.5	$^\circ C/W$
	$R_{\theta JA}$	30	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	$^\circ C$

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 0.25\text{ mA}$)	$V_{(BR)DSS}$	450 500	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}$, $V_{GS} = 0$) ($V_{DS} = 0.8 \text{ Rated } V_{DSS}$, $V_{GS} = 0$, $T_J = 125^\circ\text{C}$)	I_{DSS}	—	0.2 1	mAdc
Gate-Body Leakage Current, Forward ($V_{GSF} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 1\text{ mA}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 7.5\text{ Adc}$)	$r_{DS(on)}$	—	0.4	Ohm
Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 7.5\text{ Adc}$) ($I_D = 15\text{ Adc}$, $T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	—	6 5.8	Vdc
Forward Transconductance ($V_{DS} = 15\text{ V}$, $I_D = 7.5\text{ A}$)	g_{FS}	4	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz}$) See Figure 11	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	500	
Reverse Transfer Capacitance		C_{rss}	—	200	

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	$(V_{DD} = 25\text{ V}$, $I_D = 0.5 \text{ Rated } I_D$ $R_{gen} = 50\text{ ohms}$) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	180	
Turn-Off Delay Time		$t_{d(off)}$	—	450	
Fall Time		t_f	—	180	
Total Gate Charge	$(V_{DS} = 0.8 \text{ Rated } V_{DSS}$, $I_D = \text{Rated } I_D$, $V_{GS} = 10\text{ V}$) See Figure 12	Q_g	110 (Typ)	160	nC
Gate-Source Charge		Q_{gs}	50 (Typ)	—	
Gate-Drain Charge		Q_{gd}	60 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	$(I_S = \text{Rated } I_D$ $V_{GS} = 0)$	V_{SD}	1.1 (Typ)	1.4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	1200 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25" from the package to the source bond pad)	L_s	12.5 (Typ)	—	

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

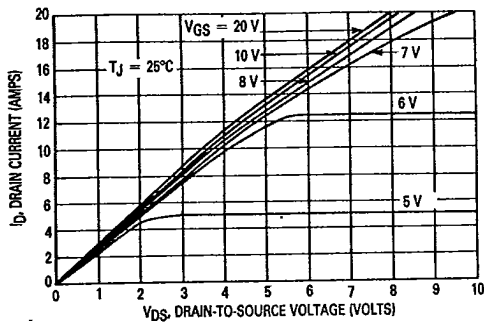


Figure 1. On-Region Characteristics

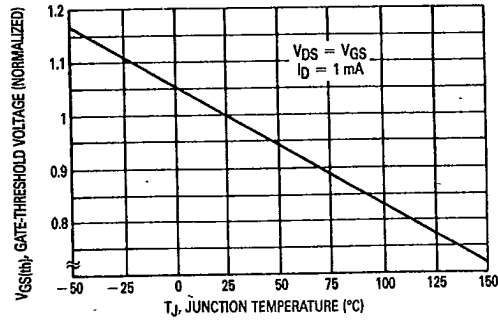


Figure 2. Gate-Threshold Voltage Variation With Temperature

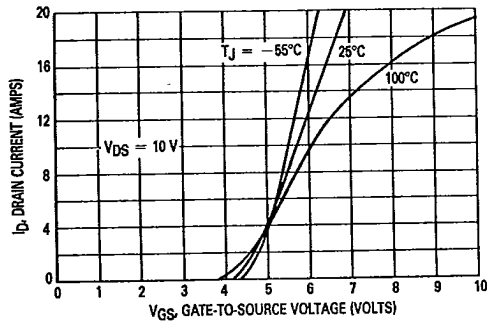


Figure 3. Transfer Characteristics

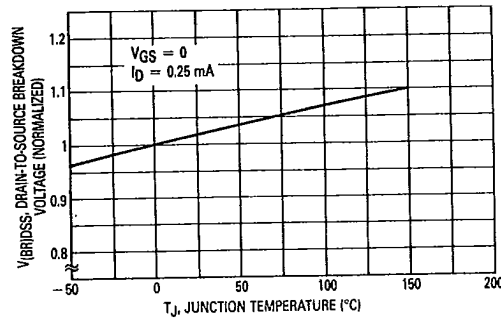


Figure 4. Breakdown Voltage Variation With Temperature

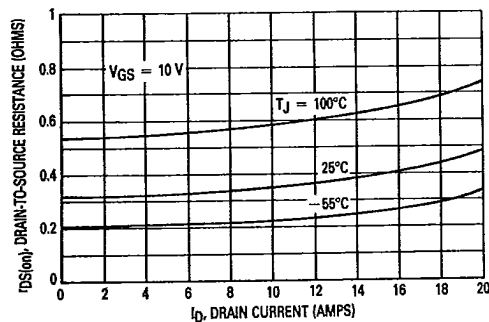


Figure 5. On-Resistance versus Drain Current

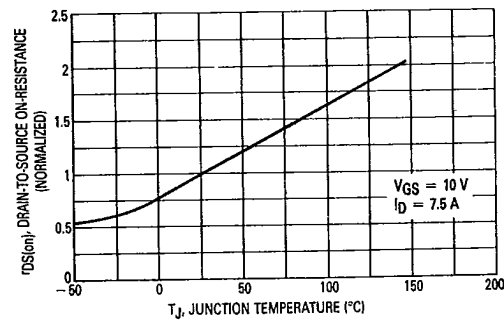


Figure 6. On-Resistance Variation With Temperature

MOTOROLA TMOS POWER MOSFET DATA

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SAFE OPERATING AREA INFORMATION

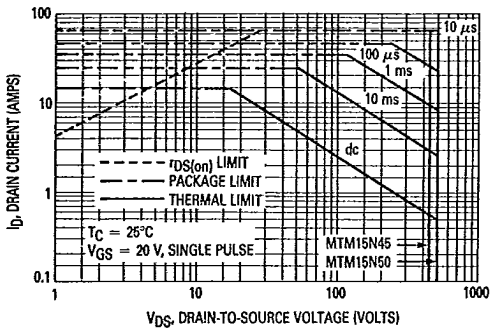


Figure 7. Maximum Rated Forward Biased Safe Operating Area

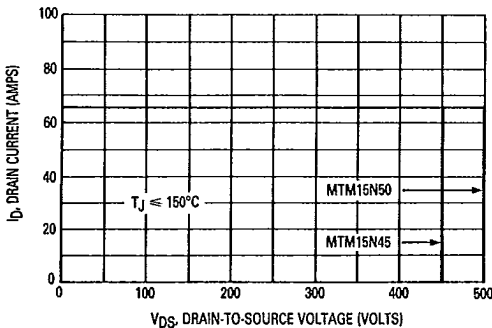


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, V(BR)DSS. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

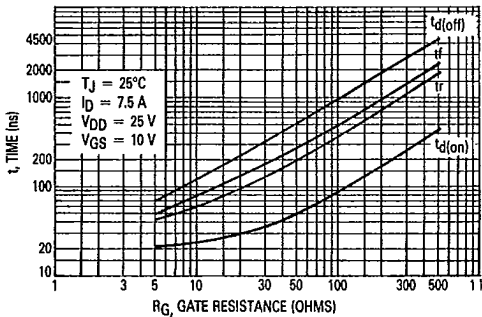


Figure 9. Resistive Switching Time Variation versus Gate Resistance

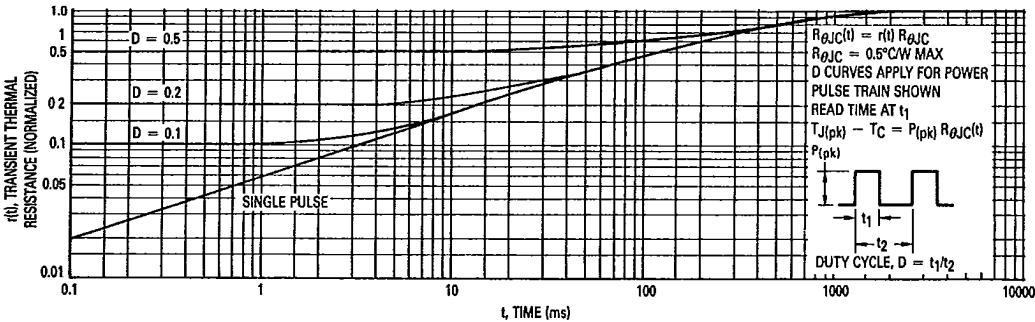


Figure 10. Thermal Response

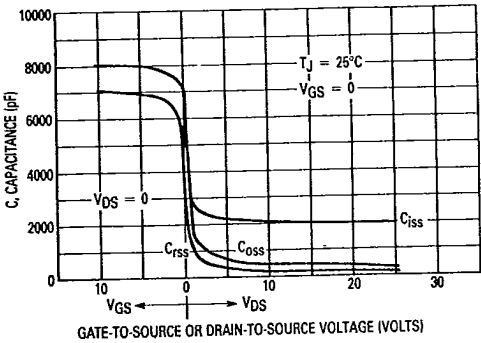


Figure 11. Capacitance Variation

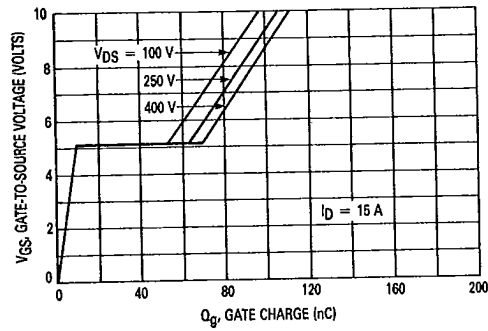


Figure 12. Gate Charge versus Gate-to-Source Voltage

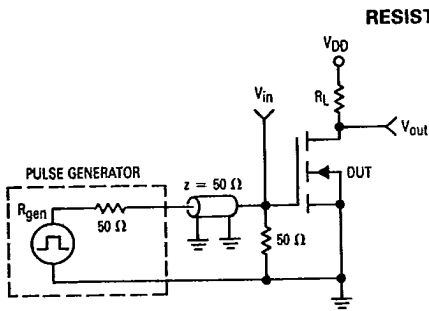


Figure 13. Switching Test Circuit

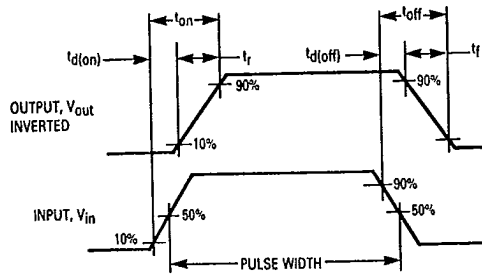
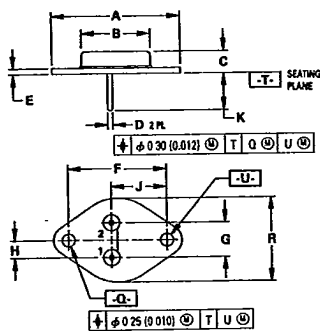


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

CASE 197A-02
TO-204AE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	28.35	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	8.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
L	3.84	4.19	0.151	0.165
M	25.15	26.67	0.990	1.050
N	3.84	4.19	0.151	0.165