

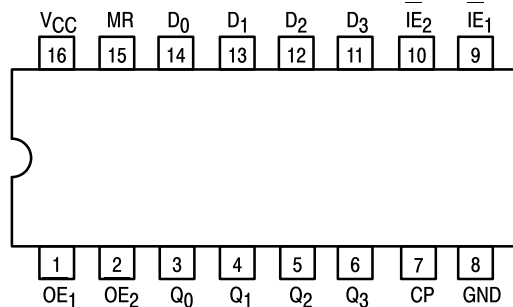


4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

The SN54/74LS173A is a high-speed 4-Bit Register featuring 3-state outputs for use in bus-organized systems. The clock is fully edge-triggered allowing either a load from the D inputs or a hold (retain register contents) depending on the state of the Input Enable Lines ($\overline{IE_1}$, $\overline{IE_2}$). A HIGH on either Output Enable line ($\overline{OE_1}$, $\overline{OE_2}$) brings the output to a high impedance state without affecting the actual register contents. A HIGH on the Master Reset ($\overline{MR}$) input resets the Register regardless of the state of the Clock (CP), the Output Enable ($\overline{OE_1}$, $\overline{OE_2}$) or the Input Enable ($\overline{IE_1}$, $\overline{IE_2}$) lines.

- Fully Edge-Triggered
- 3-State Outputs
- Gated Input and Output Enables
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

$\overline{D_0}-\overline{D_3}$	Data Inputs
$\overline{IE_1}-\overline{IE_2}$	Input Enable (Active LOW)
$\overline{OE_1}-\overline{OE_2}$	Output Enable (Active LOW) Inputs
CP	Clock Pulse (Active HIGH Going Edge) Input
MR	Master Reset Input (Active HIGH)
Q_0-Q_3	Outputs (Note b)

LOADING (Note a)

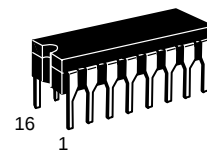
	HIGH	LOW
$\overline{D_0}-\overline{D_3}$	0.5 U.L.	0.25 U.L.
$\overline{IE_1}-\overline{IE_2}$	0.5 U.L.	0.25 U.L.
$\overline{OE_1}-\overline{OE_2}$	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
Q_0-Q_3	65 (25) U.L.	15 (7.5) U.L.

NOTES:

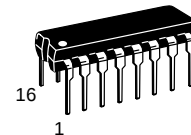
- a. 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS173A

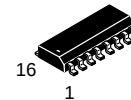
4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

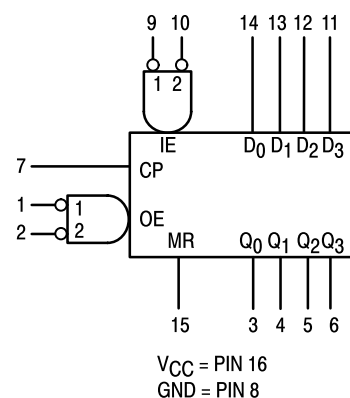


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

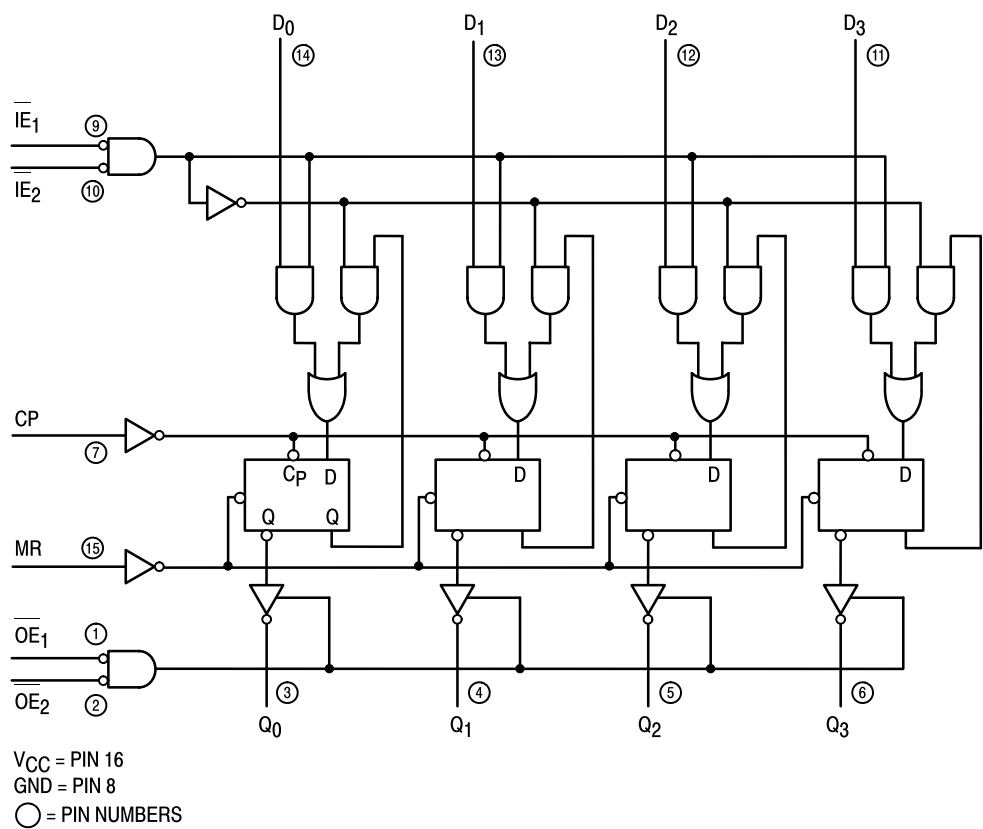
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



SN54/74LS173A

LOGIC DIAGRAM



TRUTH TABLE

MR	CP	IE1	IE2	Dn	Qn
H	x	x	x	x	L
L	L	x	x	x	Qn
L	↗	H	x	x	Qn
L	↗	x	H	x	Qn
L	↗	L	L	L	L
L	↗	L	L	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

When either OE1, or OE2 are HIGH, the output is in the off state (High Impedance); however this does not affect the contents or sequential operation of the register.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
IOH	Output Current — High	54 74			-1.0 -2.6	mA
IOL	Output Current — Low	54 74			12 24	mA

SN54/74LS173A

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V _{CC} = MIN, I _{IN} = −18 mA	
V _{OH}	Output HIGH Voltage	54	2.4	3.4		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	3.1		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _O = 2.7 V	
I _{OZL}	Output Off Current LOW				−20	μA	V _{CC} = MAX, V _O = 0.4 V	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				−0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		−30		−130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				30	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
f_{MAX}	Maximum Input Clock Frequency		30	50		MHz	$V_{CC} = 5.0 \text{ V}$ $C_L = 45 \text{ pF}$ $R_L = 667 \Omega$	
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			17 22	25 30	ns		
t_{PHL}	Propagation Delay, MR to Output			26	35	ns		
t_{PZH} t_{PZL}	Output Enable Time			15 18	23 27	ns		
t_{PLZ} t_{PHZ}	Output Disable Time			11 11	17 17	ns	$C_L = 5.0 \text{ pF}$, $R_L = 667 \Omega$	

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t_W	Clock or MR Pulse Width		20			ns	$V_{CC} = 5.0 \text{ V}$	
t_S	Data Enable Setup Time		35			ns		
t_S	Data Setup Time		17			ns		
t_h	Hold Time, Any Input		0			ns		
t_{rec}	Recovery Time		10			ns		

SN54/74LS173A

AC WAVEFORMS

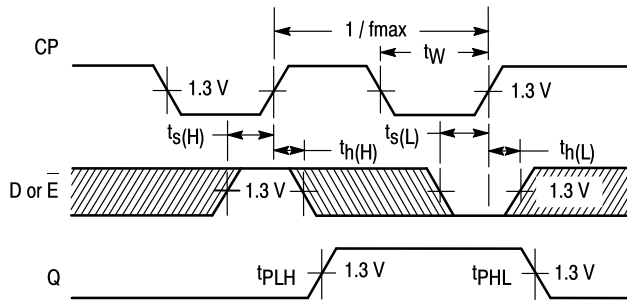


Figure 1

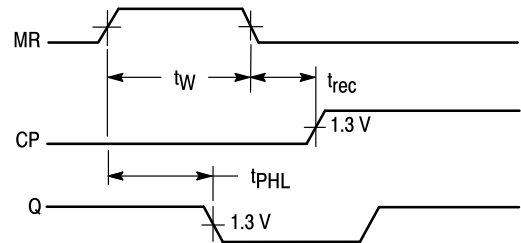


Figure 2

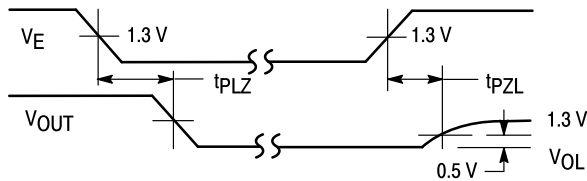


Figure 3

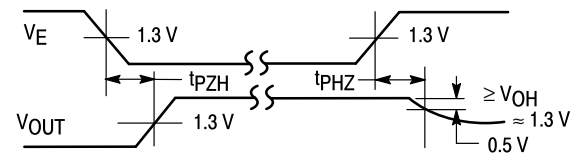
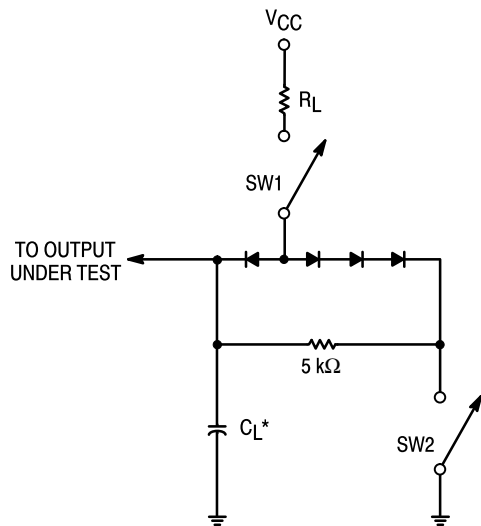


Figure 4

AC LOAD CIRCUIT



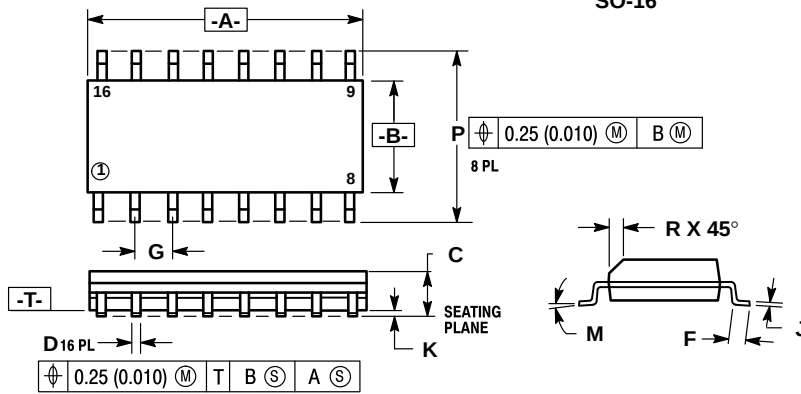
* Includes Jig and Probe Capacitance.

Figure 5

SWITCH POSITIONS

SYMBOL	SW1	SW2
tPZH	Open	Closed
tPZL	Closed	Open
tPLZ	Closed	Closed
tPHZ	Closed	Closed

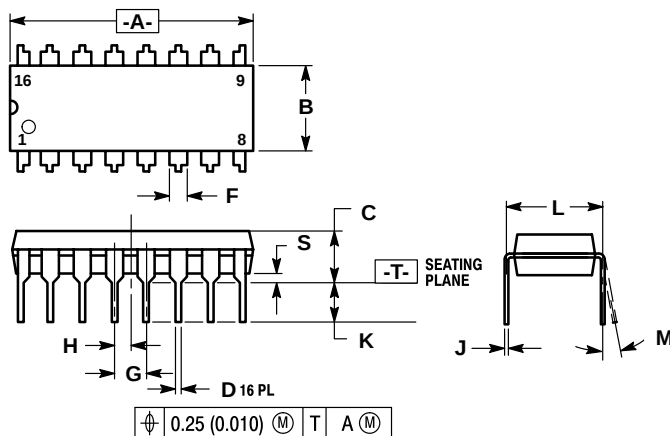
Case 751B-03 D Suffix
16-Pin Plastic
SO-16



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

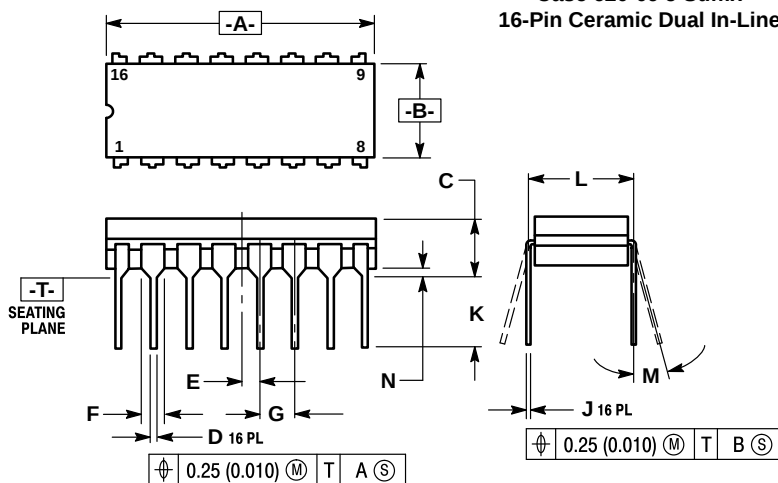
Case 648-08 N Suffix
16-Pin Plastic



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.
 6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

Case 620-09 J Suffix
16-Pin Ceramic Dual In-Line



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
 5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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