National Semiconductor

F100136
4-Stage Counter/Shift Register

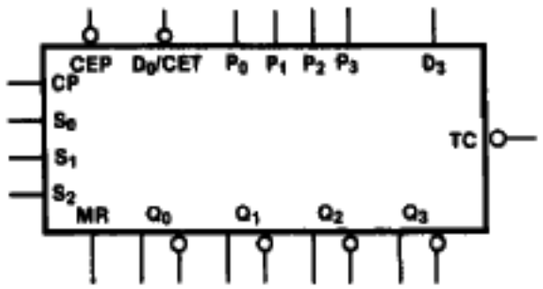
General Description

The F100136 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (S_n) inputs determine the mode of operation, as shown in the Function Select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multistage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (D_0) input for shift-up operation. For shift-down operation, D_3 is the Serial Data input. In counting operations the Terminal Count ($\overline{TC}$) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the $D_0/\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multistage counting or shift-up operation. The individual Preset (P_n) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 50 kΩ pull-down resistors.

Refer to the F100336 datasheet for:
- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (−4.2V to −5.7V)

Ordering Code: See Section 8

Logic Symbol

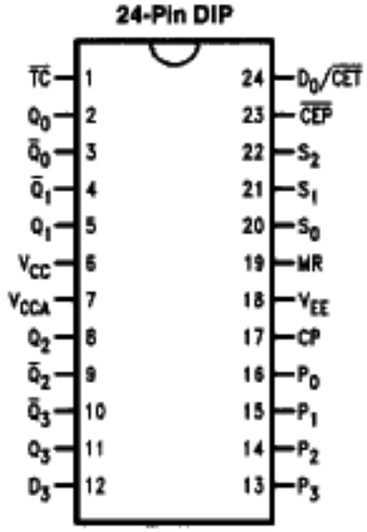


TL/F/9855–3

Pin Names	Description
CP	Clock Pulse Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$D_0/\overline{CET}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
S_0–S_2	Select Inputs
MR	Master Reset Input
P_0–P_3	Preset Inputs
D_3	Serial Data Input
$\overline{TC}$	Terminal Count Output
Q_0–Q_3	Data Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complementary Data Outputs

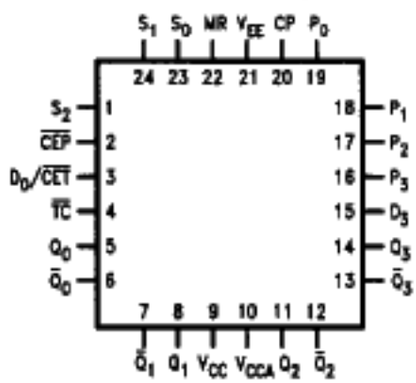
Connection Diagrams

24-Pin DIP



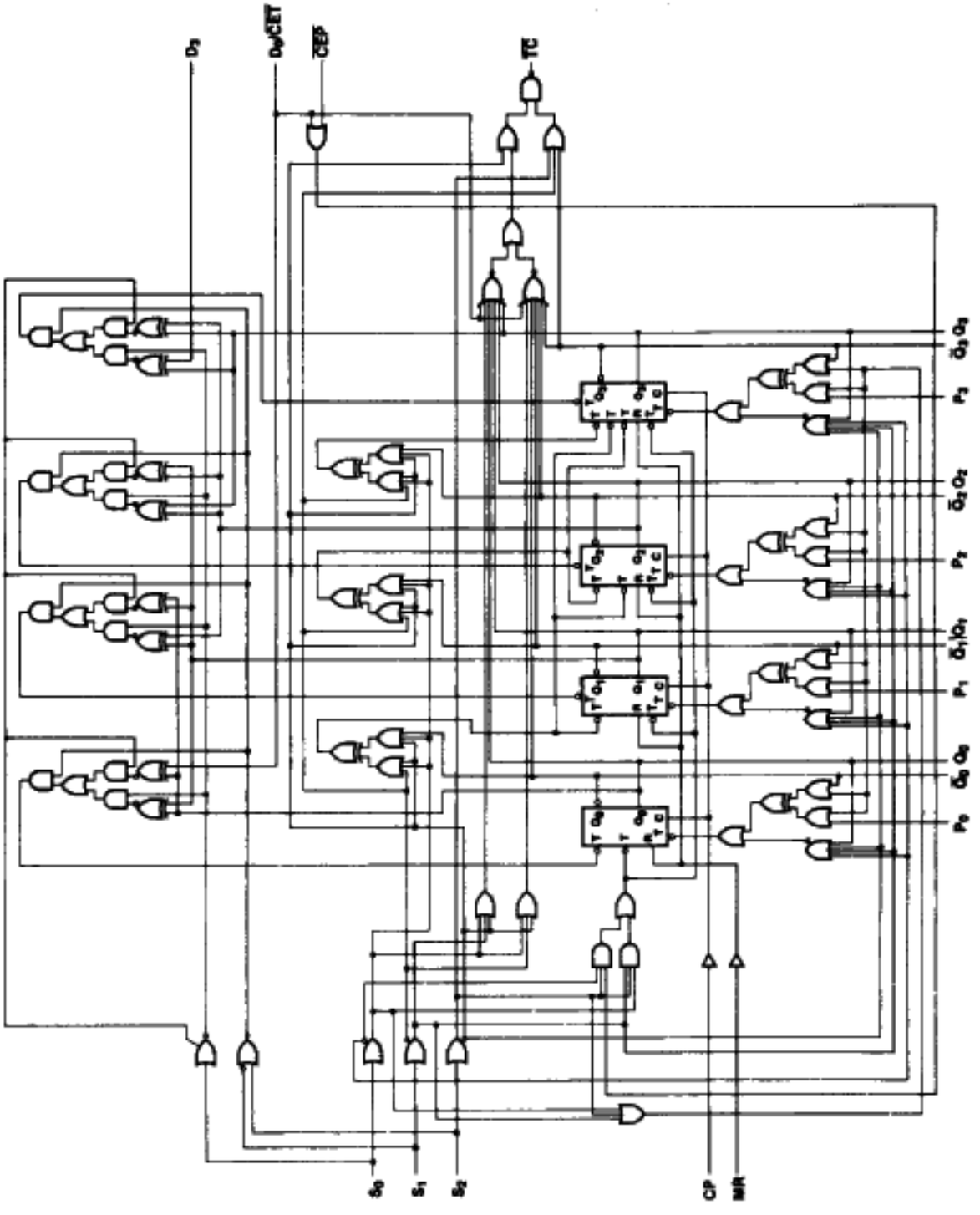
TL/F/9855–1

24-Pin Quad Cerpak



TL/F/9855–2

Logic Diagram



TL/F/9855–5

Function Select Table

S_2	S_1	S_0	Function
L	L	L	Parallel Load
L	L	H	Complement
L	H	L	Shift Left
L	H	H	Shift Right
H	L	L	Count Down
H	L	H	Clear
H	H	L	Count Up
H	H	H	Hold

Truth Table

Q_0 = LSB

Inputs								Outputs					
MR	S_2	S_1	S_0	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_3	Q_2	Q_1	Q_0	$\overline{TC}$	Mode
L	L	L	L	X	X	X	↗	P_3	P_2	P_1	P_0	L	Preset (Parallel Load)
L	L	L	H	X	X	X	↗	$\overline{Q}_3$	$\overline{Q}_2$	$\overline{Q}_1$	$\overline{Q}_0$	L	Invert
L	L	H	L	X	X	X	↗	D_3	Q_3	Q_2	D_1	D_3	Shift Left
L	L	H	H	X	X	X	↗	Q_2	Q_1	Q_0	D_0	Q_3*	Shift Right
L	H	L	L	L	L	X	↗	(Q_{0-3}) minus 1				①	Count Down
L	H	L	L	H	L	X	X	Q_3	Q_2	Q_1	Q_0	①	Count Down with $\overline{CEP}$ not active
L	H	L	L	X	H	X	X	Q_3	Q_2	Q_1	Q_0	H	Count Down with $\overline{CET}$ not active
L	H	L	H	X	X	X	↗	L	L	L	L	H	Clear
L	H	H	L	L	L	X	↗	(Q_{0-3}) plus 1				②	Count Up
L	H	H	L	H	L	X	X	Q_3	Q_2	Q_1	Q_0	②	Count Up with $\overline{CEP}$ not active
L	H	H	L	X	H	X	X	Q_3	Q_2	Q_1	Q_0	H	Count Up with $\overline{CET}$ not active
L	H	H	H	X	X	X	X	Q_3	Q_2	Q_1	Q_0	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

① = L if Q_0–Q_3 = LLLL
H if Q_0–Q_3 ≠ LLLL

② = L if Q_0–Q_3 = HHHH
H if Q_0–Q_3 ≠ HHHH

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

↗ = LOW-to-HIGH Transition

*Before the clock, $\overline{TC}$ is Q_3
After the clock, $\overline{TC}$ is Q_2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current					
	P_n, S_n			180		
	$\overline{CEP}$			200		
	MR			240	μA	V_{IN} = $V_{IH\ (Max)}$
	D_3			280		
	CP			390		
	$D_0/\overline{CET}$			530		
I_{EE}	Power Supply Current	−283	−195	−136	mA	Inputs Open

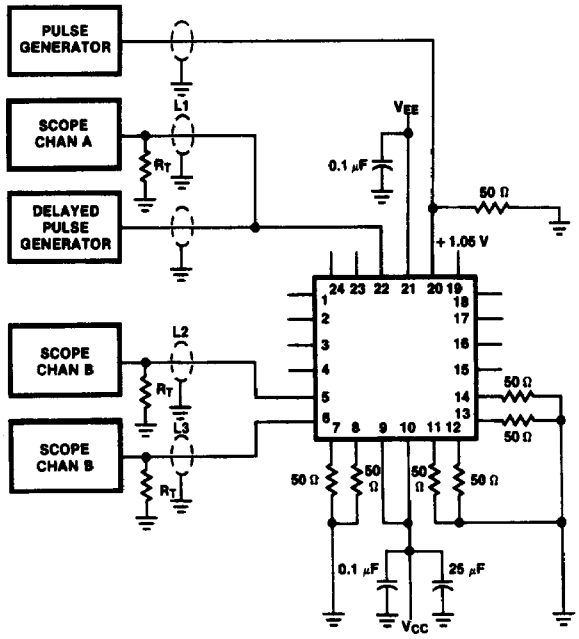
Ceramic Dual-In-Line Package AC Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{shift}	Shift Frequency	250		250		250		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	0.85	2.10	0.85	2.10	0.85	2.25	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	1.90	4.80	1.90	4.60	1.90	5.20	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.20	2.95	1.35	2.95	1.20	3.10	ns	*Figures 1* and *4*
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	2.20	4.80	2.20	4.80	2.20	5.30	ns	
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.40	3.20	1.40	3.20	1.40	3.50	ns	*Figures 1* and *5*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	0.90	3.80	1.00	3.80	1.00	4.30	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	*Figures 1* and *3*
t_s	Setup Time								
	D_3	1.20		1.20		1.20			
	P_n	1.70		1.70		1.70			
	$D_0/\overline{CET}$, $\overline{CEP}$	1.45		1.45		1.45		ns	*Figure 6*
	S_n	3.30		3.30		3.30			
	MR (Release Time)	2.60		2.60		2.60			
t_h	Hold Time								
	D_3	0.20		0.20		0.20			
	P_n	0.10		0.10		0.10		ns	*Figure 6*
	$D_0/\overline{CET}$, $\overline{CEP}$	0.20		0.20		0.20			
	S_n	−0.90		−0.90		−0.90			
$t_{pw}(H)$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{shift}	Shift Frequency	250		250		250		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	0.85	1.90	0.85	1.90	0.85	2.05	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	1.90	4.60	1.90	4.40	1.90	5.00	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.20	2.75	1.35	2.75	1.20	2.90	ns	*Figures 1* and *4*
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	2.20	4.60	2.20	4.60	2.20	5.10	ns	
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.40	3.00	1.40	3.00	1.40	3.30	ns	*Figures 1* and *5*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	0.90	3.60	1.00	3.60	1.00	4.10	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	*Figures 1* and *3*
t_s	Setup Time							ns	*Figure 6*
	D_3	1.10		1.10		1.10			
	P_n	1.60		1.60		1.60			
	$D_0/\overline{CET}$, $\overline{CEP}$	1.35		1.35		1.35			
	S_n	3.20		3.20		3.20			
	MR (Release Time)	2.50		2.50		2.50			
t_h	Hold Time							ns	*Figure 6*
	D_3	0.10		0.10		0.10			
	P_n	0		0		0			
	$D_0/\overline{CET}$, $\overline{CEP}$	0.10		0.10		0.10			
	S_n	−1.00		−1.00		−1.00			
$t_{pw}(H)$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1, L2 and L3 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 µF from GND to V_{CC} and V_{EE}

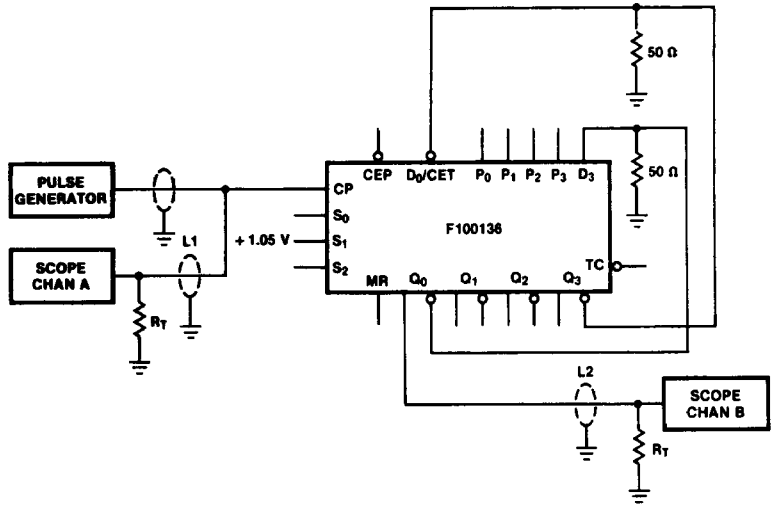
All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak;
for DIP see logic symbol

TL/F/9855–6

FIGURE 1. AC Test Circuit



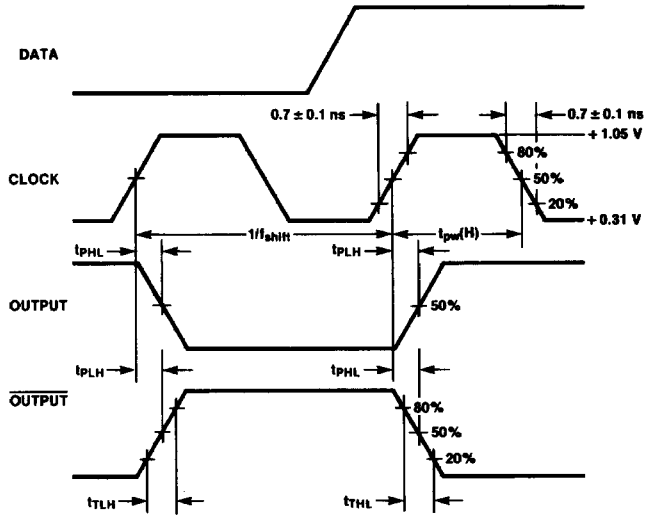
TL/F/9855–7

FIGURE 2. Shift Frequency Test Circuit (Shift Left)

Notes:

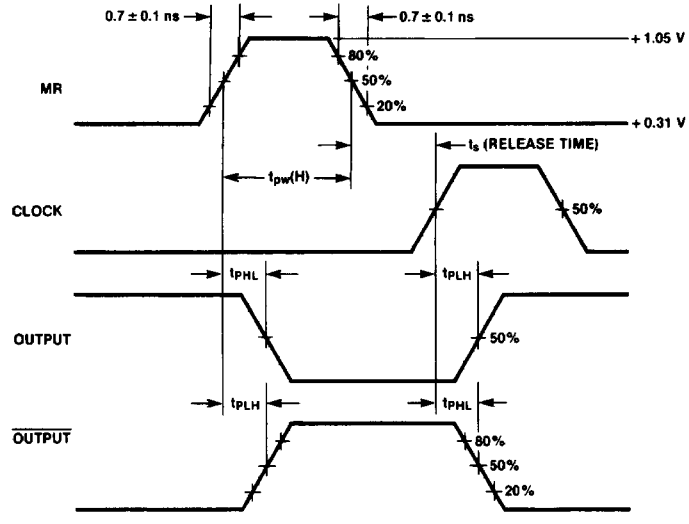
For shift right mode, +1.05V is applied at S_0.

The feedback path from output to input should be as short as possible.



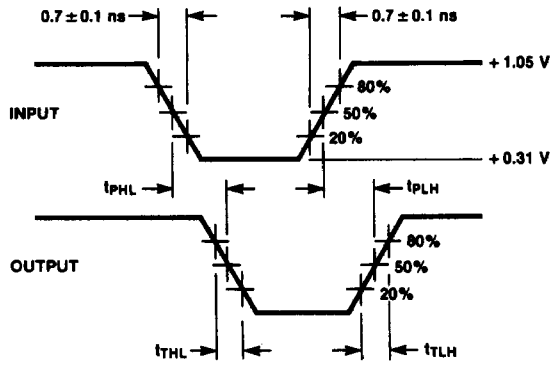
TL/F/9855–8

FIGURE 3. Propagation Delay (Clock) and Transition Times



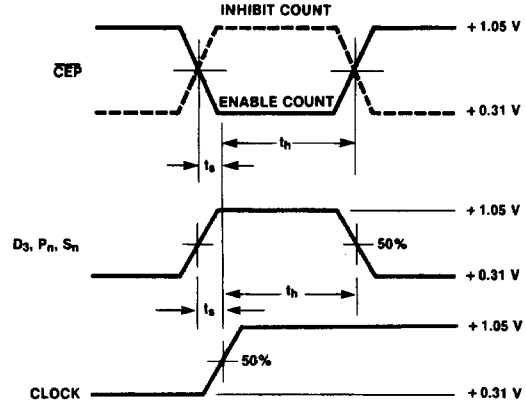
TL/F/9855–9

FIGURE 4. Propagation Delay (Reset)



TL/F/9855–10

FIGURE 5. Propagation Delay (Serial Data, Selects)



TL/F/9855–11

Notes:

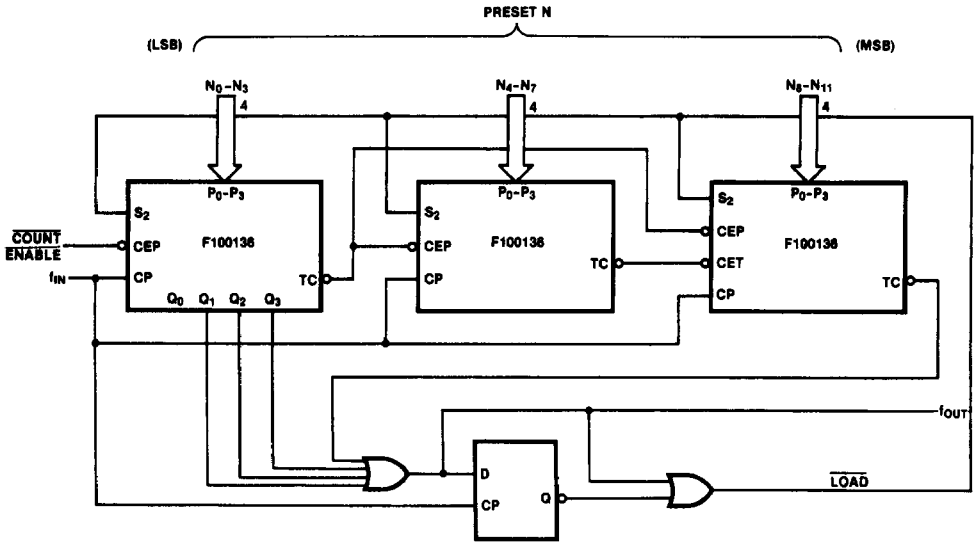
t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 6. Setup and Hold Time

Applications

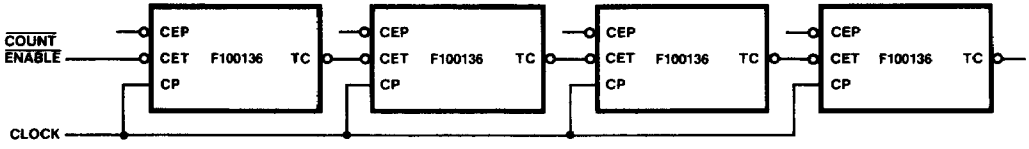
3-Stage Divider, Preset Count Down Mode



Note: If $S_0 = S_1 = S_2$ = LOW, then T_C = LOW

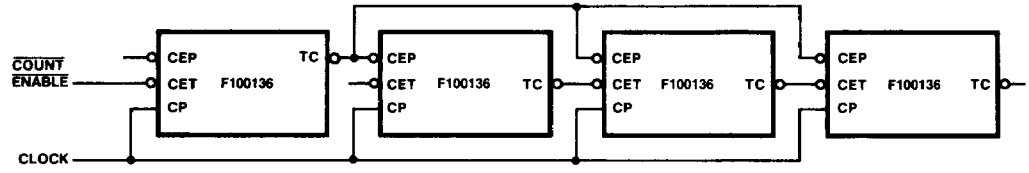
TL/F/9855–12

Slow Expansion Scheme



TL/F/9855–13

Fast Expansion Scheme



TL/F/9855–15