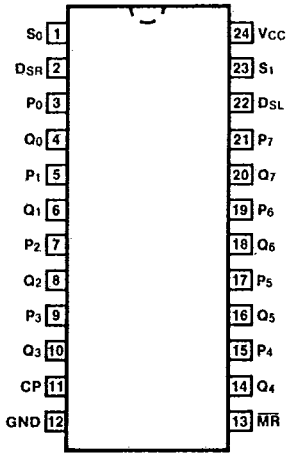
54/74198

8-BIT R/L SHIFT REGISTER

DESCRIPTION — The '198 features synchronous parallel load, hold, shift right and shift left modes, as determined by the Select (S_0, S_1) inputs. State changes are initiated by the rising edge of the clock. An asynchronous Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register. The '198 is useful for serial-serial, serial-parallel, parallel-serial and parallel-parallel register transfers.

- **PARALLEL IN/PARALLEL OUT**
- **SYNCHRONOUS PARALLEL LOAD**
- **SHIFT RIGHT AND SHIFT LEFT CAPABILITY**
- **ASYNCHRONOUS OVERRIDING CLEAR**

CONNECTION DIAGRAM
PINOUT A



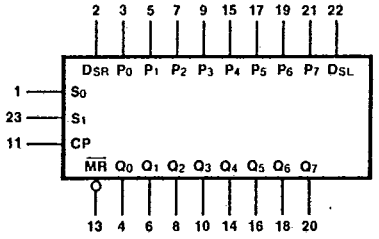
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74198PC		9N
Ceramic DIP (D)	A	74198DC	54198DM	6N
Flatpak (F)	A	74198FC	54198FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
S_0, S_1	Mode Select Inputs	1.0/1.0
P_0 — P_7	Parallel Data Inputs	1.0/1.0
D_{SR}	Serial Data Input (Shift Right)	1.0/1.0
D_{SL}	Serial Data Input (Shift Left)	1.0/1.0
$\overline{CP}$	Clock Pulse Input (Active Rising Edge)	1.0/1.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0
Q_0 — Q_7	Flip-flop Outputs	20/10

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

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FUNCTIONAL DESCRIPTION — The '198 contains eight edge-triggered D-type flip-flops and the interstage gating required to perform synchronous parallel load, shift right, and shift left operations. Serial data enters at D_{SR} for shift right and at D_{SL} for shift left operations. Parallel data is applied to the $P_0 - P_7$ inputs. State changes are initiated by the rising edge of the clock. The D_{SR}, D_{SL} and $P_0 - P_7$ inputs can change when the clock is in either state, provided only that the recommended setup and hold times are observed.

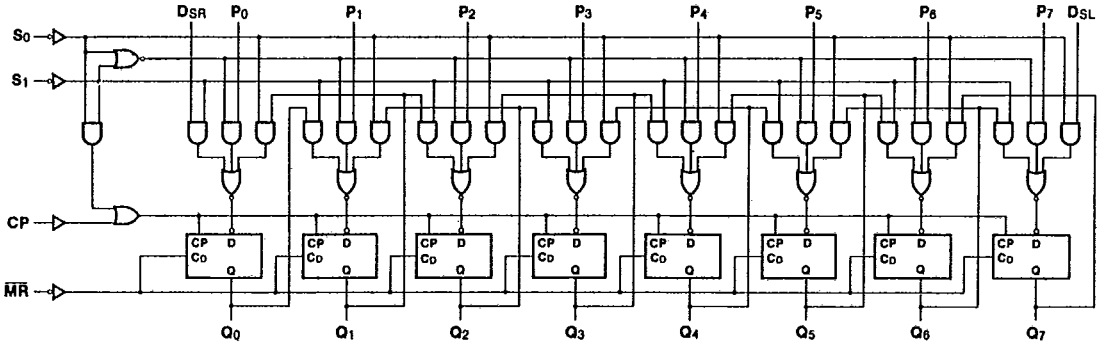
The operating mode is determined by S_0 and S_1, as shown in the Mode Select Table. Clocking of the flip-flops is inhibited when both S_0 and S_1 are LOW. To avoid inadvertently clocking the register, the Select inputs should only be changed while CP is HIGH. A LOW signal on $\overline{MR}$ overrides all other inputs and forces the outputs LOW.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{MR}$	CP	S_0*	S_1*	
L	X	X	X	Asynchronous Reset; Outputs = LOW
H	↗	H	H	Parallel Load; $P_n \rightarrow Q_n$
H	↗	L	H	Shift Right; $D_{SR} \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	↗	H	L	Shift Left; $D_{SL} \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	X	L	L	Hold

*Select inputs should be changed only while CP is HIGH
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XC		116	mA	V_{CC} = Max; S_0, S_1 = 4.5 V
		XM		104		CP = ⊓ ; $\overline{MR}$, P_n = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω Min	54/74 Max	UNITS	CONDITIONS
f_{max}	Maximum Shift Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		26 30	ns	Figs. 3-1, 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		35	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n, D_{SL}, D_{SR} to CP	20 20		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n, D_{SL}, D_{SR} to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW S_0 or S_1 to CP	30 30		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW S_0 or S_1 to CP	0 0		ns	
t_w (H)	CP Pulse Width HIGH	20		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-16

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