National Semiconductor

MICROCIRCUIT DATA SHEET

MRLM111-X-RH REV 0E1

Original Creation Date: 04/20/00
Last Update Date: 06/11/04
Last Major Revision Date: 04/20/00

VOLTAGE COMPARATOR: ALSO AVAILABLE GUARANTEED TO 30k rd(Si) TESTED TO MIL-STD-883, METHOD 1019

General Description

The LM111, is a voltage comparator that has input currents nearly a thousand times lower than devices such as the LM106 and LM710. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 50V at currents as high as 50mA.

Both the inputs and the outputs of the LM111, can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

Industry Part Number

LM111

Prime Die

LM111

Controlling Document

SEE FEATURES SECTION

NS Part Numbers

LM111HPQMLV
LM111J-8PQMLV
LM111WGPQMLV
LM111WPQMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55

Features

- Low Input Bias Current.
- Low Input Offset Current.
- Wide Differential Input Voltage.
- Power Supply Voltage, Single 5V to ±15V.
- Offset Voltage Null Capability.
- Strobe Capability

CONTROLLING DOCUMENTS:

LM111HPQMLV	5962P0052401VGA
LM111J-8PQMLV	5962P0052401VPA
LM111WGPQMLV	5962P0052401VZA
LM111WPQMLV	5962P0052401VHA

(Absolute Maximum Ratings)

(Note 1)

Positive Supply Voltage		+30.0V
Negative Supply Voltage		-30.0V
Total Supply Voltage		36V
Output to Negative Supply Voltage		50V
GND to Negative Supply Voltage		30V
Differential Input Voltage		±30V
Sink Current		50mA
Input Voltage (Note 2)		±15V
Power Dissipation (Note 3)		
8 Lead METAL CAN		330mW at 25 C
8 Lead CERDIP		400mW at 25 C
10 Lead CERPACK		330mW at 25 C
10 Lead CERAMIC SOIC		330mW at 25 C
Output Short Circuit Duration		10 sec.
Maximum Strobe Current		10mA
Operating Temperature Range		-55 C ≤ Ta ≤ +125 C
Thermal Resistance		
ThetaJA		
8 Lead METAL CAN	(Still Air @ 0.5W)	162 C/W
	(500LF/Min Air flow @ 0.5W)	92 C/W
8 Lead CERDIP	(Still Air @ 0.5W)	134 C/W
	(500LF/Min Air flow @ 0.5W)	76 C/W
10 Lead CERPACK	(Still Air @ 0.5W)	231 C/W
	(500LF/Min Air flow @ 0.5W)	153 C/W
10 Lead CERAMIC SOIC	(Still Air @ 0.5W)	231 C/W
	(500LF/Min Air flow @ 0.5W)	153 C/W
ThetaJC		
8 Lead METAL CAN		50 C/W
8 Lead CERDIP		21 C/W
10 Lead CERPACK		24 C/W
10 Lead CERAMIC SOIC		24 C/W
Storage Temperature Range		-65 C ≤ Ta ≤ +150 C
Maximum Junction Temperature		175 C
Lead Temperature (Soldering, 60 seconds)		300 C
Voltage at Strobe Pin		V+ -5V
Package Weight (Typical)		
8 Lead METAL CAN		965mg
8 Lead CERDIP		1100mg
10 Lead CERPACK		250mg
10 Lead CERAMIC SOIC		225mg

(Absolute Maximum Ratings) (Continued)

(Note 1)

ESD Rating (Note 4)	300V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: This rating applies for ±15V supplies. The positive input voltage limits is 30V above the negative supply. The negative input voltage limits is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 4: Human body model, 1.5k Ohms in series with 100pF.

Recommended Operating Conditions

Supply Voltage	Vcc = ±15Vdc
Operating Temperature Range	-55 C ≤ Ta ≤ +125 C

Electrical Characteristics

DC PARAMETERS: (SEE NOTE 8)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Vin = 0V, Rs = 50 Ohms			-3	+3	mV	1
					-4	+4	mV	2, 3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50 Ohms			-3	+3	mV	1
					-4	+4	mV	2, 3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50 Ohms			-3	+3	mV	1
					-4	+4	mV	2, 3
		+Vcc = +2.5V, -Vcc = -2.5V, Vin = 0V, Rs = 50 Ohms			-3	+3	mV	1
					-4	+4	mV	2, 3
Vio(R)	Raised Input Offset Voltage	Vin = 0V, Rs = 50 Ohms			-3	+3	mV	1
					-4.5	+4.5	mV	2, 3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50 Ohms			-3	+3	mV	1
					-4.5	+4.5	mV	2, 3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50 Ohms			-3	+3	mV	1
					-4.5	+4.5	mV	2, 3
Iio	Input Offset Current	Vin = 0V, Rs = 50K Ohms			-10	+10	nA	1, 2
					-20	+20	nA	3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-10	+10	nA	1, 2
					-20	+20	nA	3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-10	+10	nA	1, 2
					-20	+20	nA	3
Iio(R)	Raised Input Offset Current	Vin = 0V, Rs = 50K Ohms			-25	+25	nA	1, 2
					-50	+50	nA	3
Iib+	Input Bias Current	Vin = 0V, Rs = 50K Ohms			-100	0.1	nA	1, 2
					-150	0.1	nA	3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-150	0.1	nA	1, 2
					-200	0.1	nA	3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-150	0.1	nA	1, 2
					-200	0.1	nA	3

Electrical Characteristics

DC PARAMETERS: (SEE NOTE 8) (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iib-	Input Bias Current	Vin = 0V, Rs = 50K Ohms			-100	0.1	nA	1, 2
					-150	0.1	nA	3
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-150	0.1	nA	1, 2
					-200	0.1	nA	3
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-150	0.1	nA	1, 2
					-200	0.1	nA	3
Vo(STB)	Collector Output Voltage (ST)	Vin+ = Gnd, Vin- = 15V, Istb = -3mA, Rs = 50 Ohms	1		14		V	1, 2, 3
CMR	Common Mode Rejection	-28V≤-Vcc≤-0.5V, Rs=50 Ohms, 2V≤+Vcc≤29.5V, Rs=50 Ohms, -14.5V≤Vcm≤13V,Rs=50 Ohms			80		dB	1, 2, 3
Vol	Low Level Output Voltage	+Vcc = 4.5V, -Vcc = Gnd, Iout = 8mA, ±Vin = 0.5V, Vid = -6mV				0.4	V	1, 2, 3
		+Vcc = 4.5V, -Vcc = Gnd, Iout = 8mA, ±Vin = 3V, Vid = -6mV				0.4	V	1, 2, 3
		Iout = 50mA, ±Vin = 13V, Vid = -5mV				1.5	V	1, 2, 3
		Iout = 50mA, ±Vin = -14V, Vid = -5mV				1.5	V	1, 2, 3
Icex	Output Leakage Current	+Vcc = 18V, -Vcc = -18V, Vout = 32V			-1	10	nA	1
					-1	500	nA	2
Ii	Input Leakage Current	+Vcc = 18V, -Vcc = -18V, +Vin = +12V, -Vin = -17V	7		-5	500	nA	1, 2, 3
		+Vcc = 18V, -Vcc = -18V, +Vin = -17V, -Vin = +12V	7		-5	500	nA	1, 2, 3
Icc+	Power Supply Current					6	mA	1, 2
						7	mA	3
Icc-	Power Supply Current				-5		mA	1, 2
					-6		mA	3
Delta Vio/Delta T	Temperature Coefficient Input Offset Voltage	25 C ≤ T ≤ 125 C			-25	25	uV/ C	2
		-55 C ≤ T ≤ 25 C			-25	25	uV/ C	3
Delta Iio/Delta T	Temperature Coefficient Input Offset Current	25 C ≤ T ≤ 125 C			-100	100	pA/ C	2
		-55 C ≤ T ≤ 25 C			-200	200	pA/ C	3

Electrical Characteristics

DC PARAMETERS: (SEE NOTE 8) (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ios	Short Circuit Current	Vout = 5V, t ≤ 10mS, Vin- = 0.1V, Vin+ = 0V	3, 5			200	mA	1
			3, 5			150	mA	2
			3, 5			250	mA	3
Vio(adj)+	Input Offset Voltage (Adjustment)	Vout = 0V, Vin = 0V, Rs = 50 Ohms	3		5		mV	1
Vio(adj)-	Input Offset Voltage (Adjustment)	Vout = 0V, Vin = 0V, Rs = 50 Ohms	3			-5	mV	1
Ave+	Voltage Gain (Emitter)	Rl = 600 Ohms	3, 6		10		V/mV	4
			3, 6		8		V/mV	5, 6
Ave-	Voltage Gain (Emitter)	Rl = 600 Ohms	3, 6		10		V/mV	4
			3, 6		8		V/mV	5, 6

AC PARAMETERS: (SEE NOTE 8)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: ±Vcc = ±15V, Vcm = 0

trLHC	Response Time (Collector Output)	Vod(Overdrive) = -5mV, Cl = 50pF, Vin = -100mV	4			300	nS	7, 8B
			4			640	nS	8A
trHLC	Response Time (Collector Output)	Vod(Overdrive) = 5mV, Cl = 50pF, Vin = 100mV	4			300	nS	7, 8B
			4			500	nS	8A

Electrical Characteristics

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: ±Vcc = ±15V, Vcm = 0V. "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only".

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Vin = 0V, Rs = 50 Ohms			-0.5	0.5	mV	1
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50 Ohms			-0.5	0.5	mV	1
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50 Ohms			-0.5	0.5	mV	1
Iib+	Input Bias Current	Vin = 0V, Rs = 50K Ohms			-12.5	12.5	nA	1
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-12.5	12.5	nA	1
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-12.5	12.5	nA	1
Iib-	Input Bias Current	Vin = 0V, Rs = 50K Ohms			-12.5	12.5	nA	1
		+Vcc = 29.5V, -Vcc = -0.5V, Vin = 0V, Vcm = -14.5V, Rs = 50K Ohms			-12.5	12.5	nA	1
		+Vcc = 2V, -Vcc = -28V, Vin = 0V, Vcm = +13V, Rs = 50K Ohms			-12.5	12.5	nA	1
Icex	Output Leakage Current	+Vcc = 18V, -Vcc = -18V, Vout = 32V			-5	5	nA	1

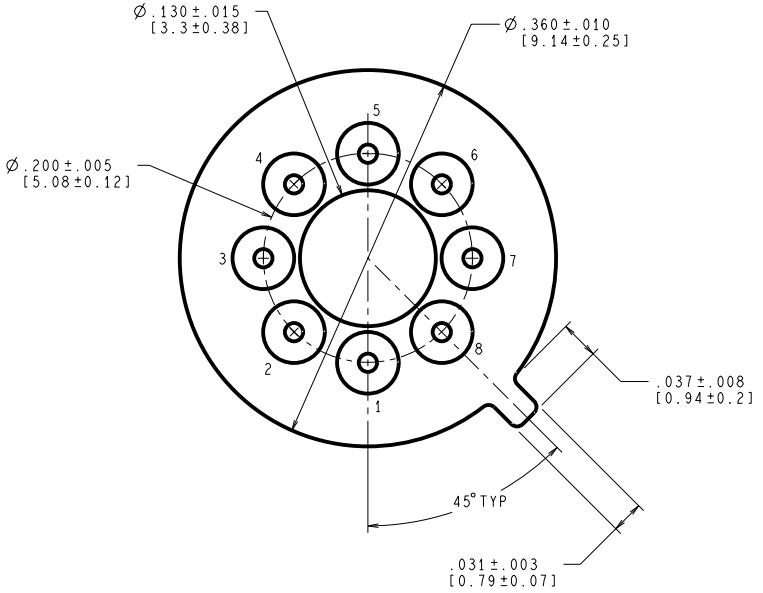
Note 1: Istb = -2mA at -55 C.
Note 2: Calculated parameter.
Note 3: Use DC tape for Ios and Vio(adj), Ave+ and Ave- as indicated in TAPE NAME section of this JRETS.
Note 4: Uses AC tape and hardware.
Note 5: Actual min. limit used is 5mA due to test setup.
Note 6: Datalog reading in K = V/mV.
Note 7: Vid is voltage difference between inputs.
Note 8: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiaton end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019.5, Condition A.

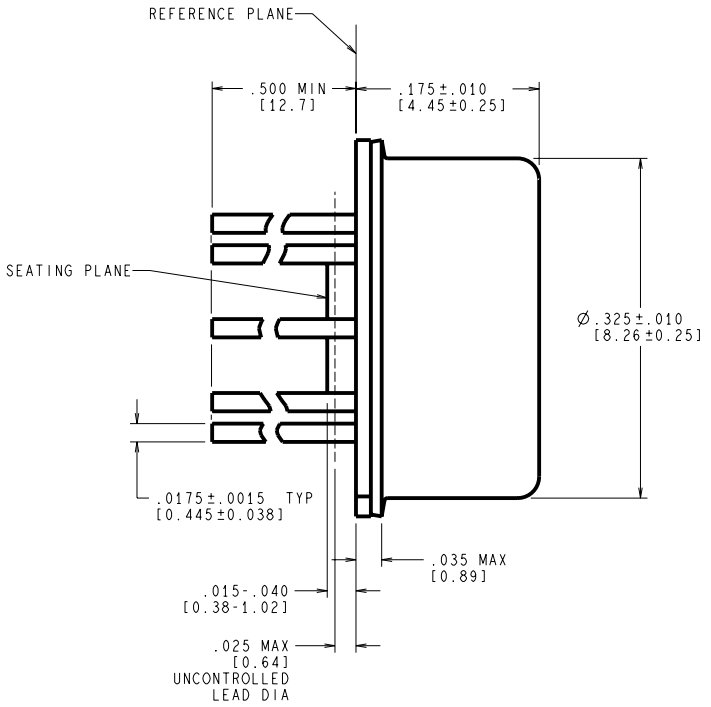
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05172HRB2	METAL CAN (H), TO-99, 8LD .200 DIA P.C. (B/I CKT)
05174HRC2	CERPACK (W), 10 LEAD (B/I CKT)
05284HRC2	METAL CAN (H), TO-99, 3LD .200 DIA P.C. (B/I CKT)
05652HRA2	CERDIP (J), 8 LEAD (B/I CKT)
09569HRC2	CERPACK (W), 10 LEAD (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000264A	METAL CAN (H), 8 LEAD (PINOUT)
P000265A	CERDIP (J), 8 LEAD (PINOUT)
P000267A	CERPACK (W), 10 LEAD (PINOUT)
P000373A	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
W10ARG	CERPACK (W), 10 LEAD (P/P DWG)
WG10ARC	CERPACK (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

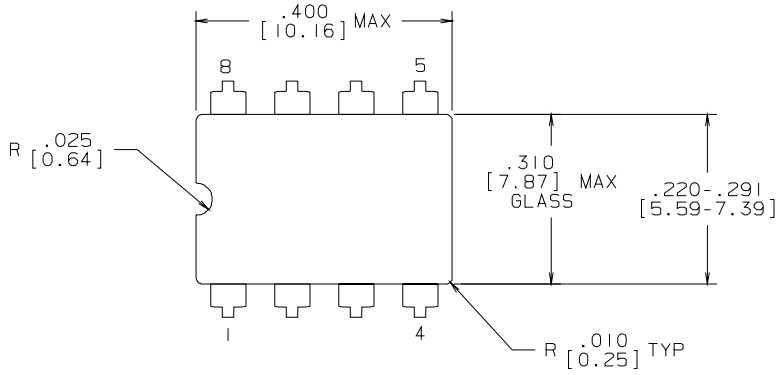
METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

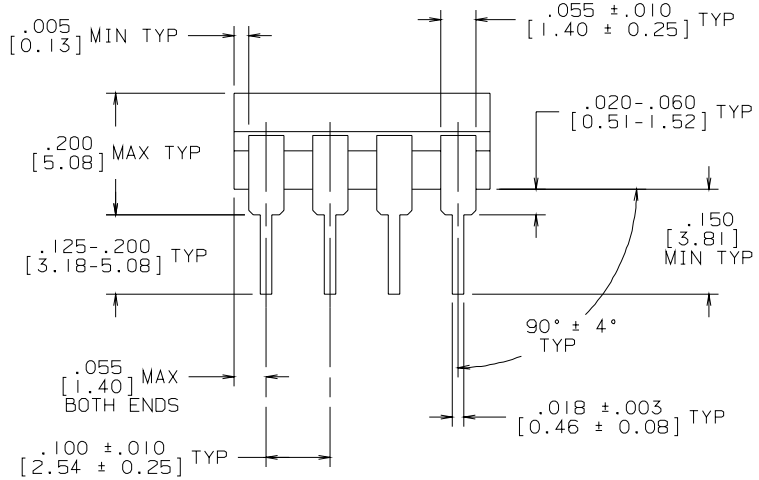
PROJECTION — INCH [MM]

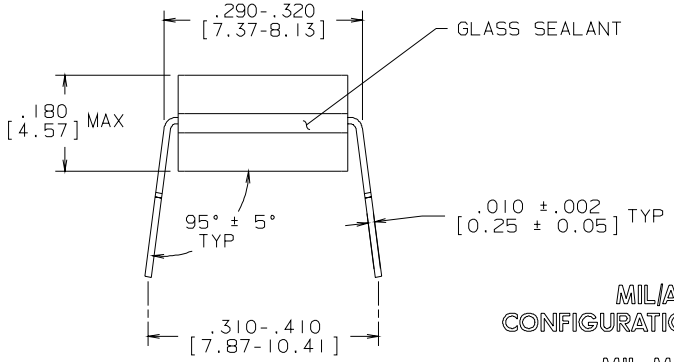
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

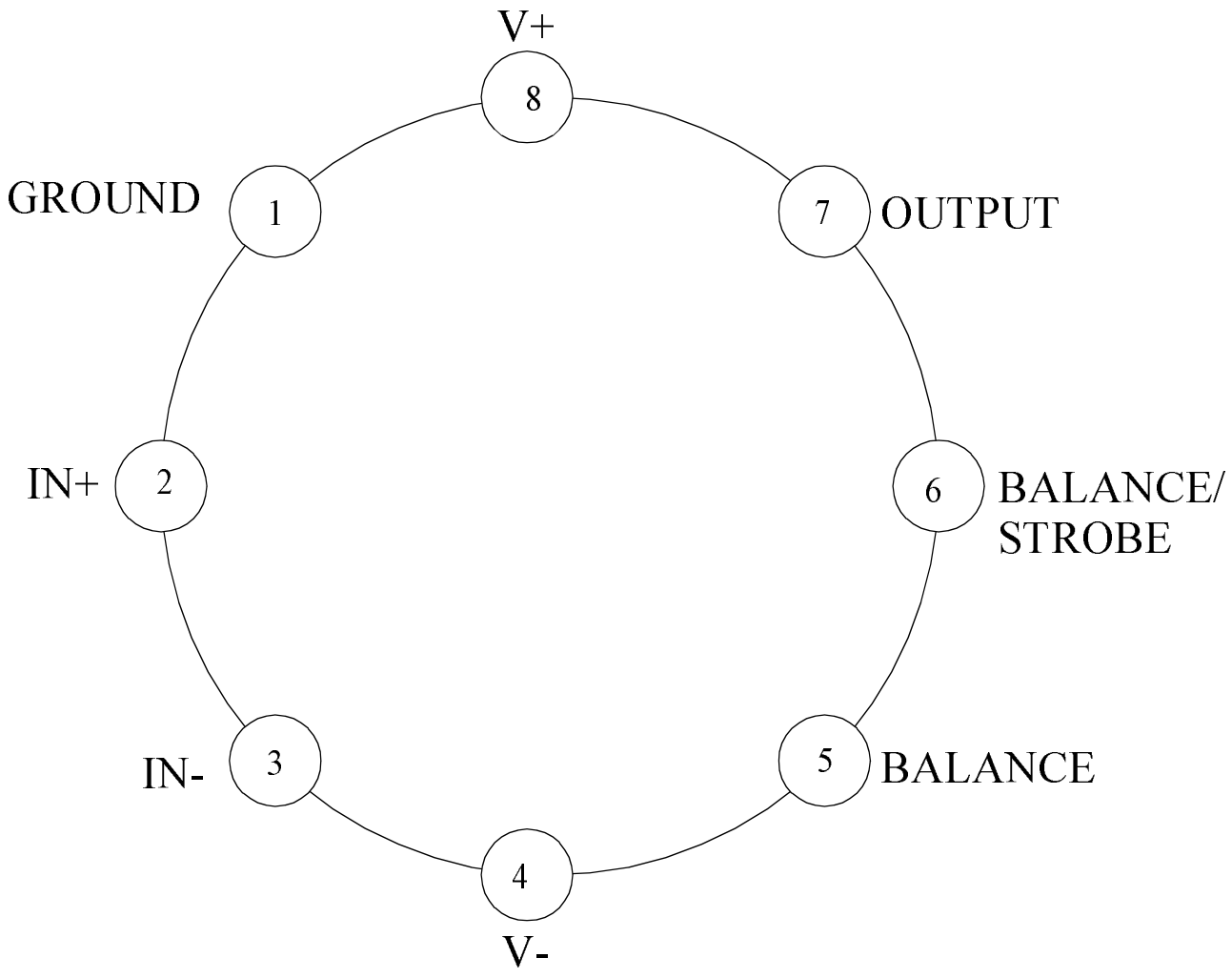
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM111H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000264A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

LM111J-8

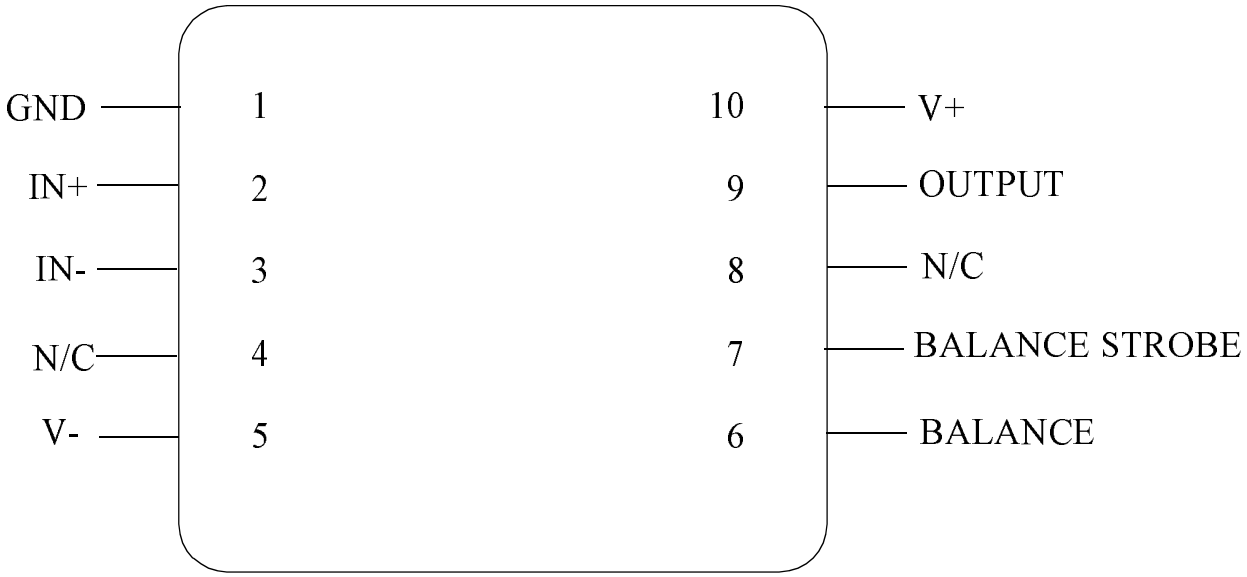
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000265A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM111W

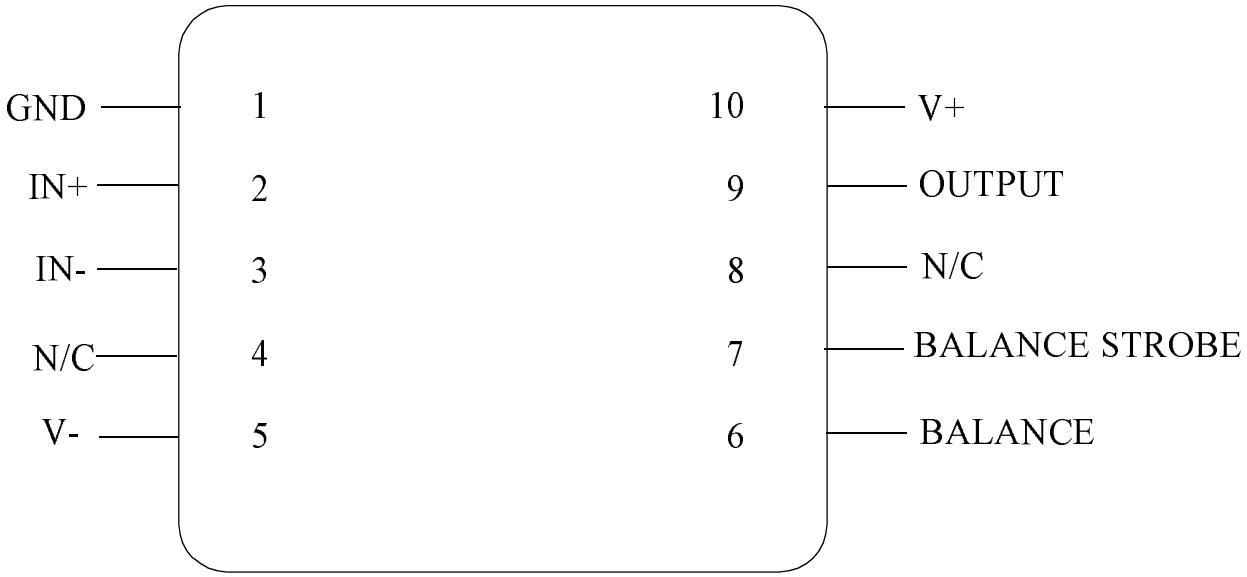
10 - LEAD CERPACK

CONNECTION DIAGRAM

TOP VIEW

P000267A

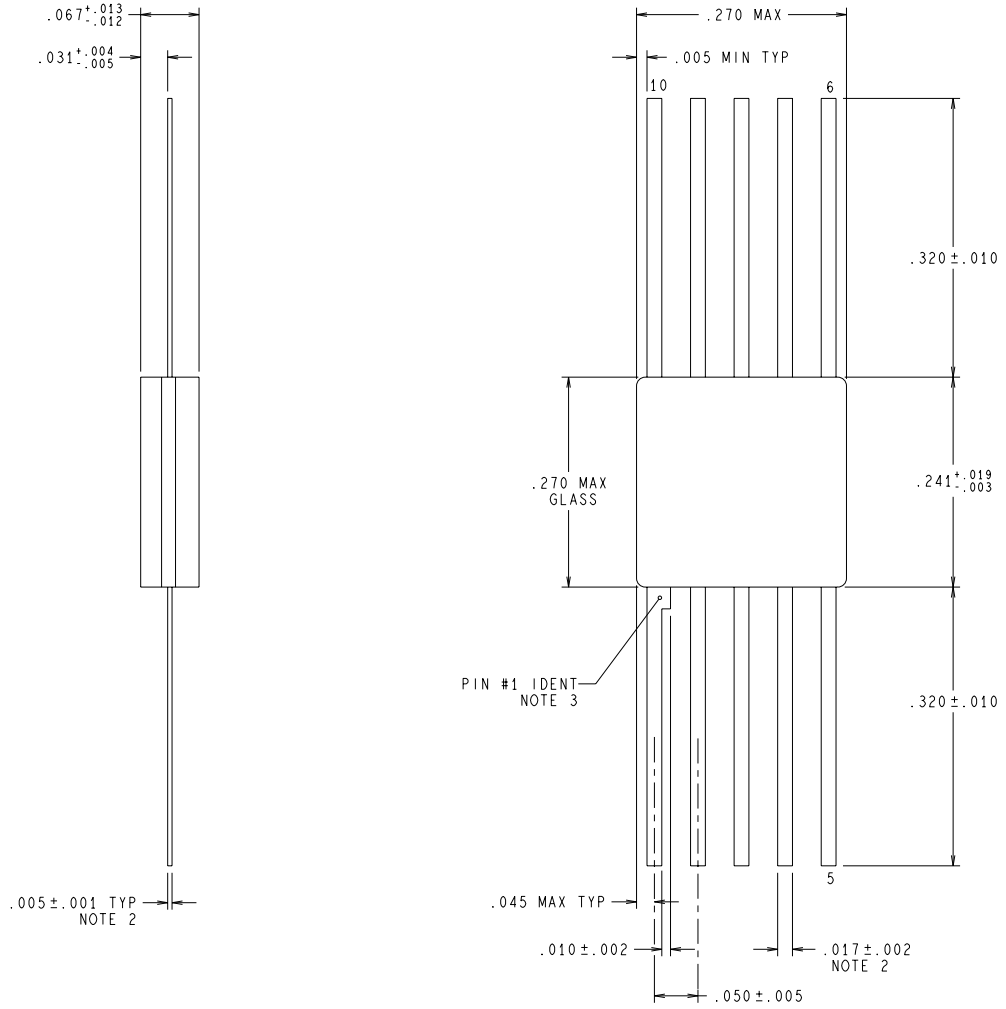
National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM111WG
10 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000373A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE AND REDRAW PER NEW STANDARD.	10510	07/28/94	DEG/AEP
G	.017±.002 WAS .017±.020.	10654	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-003, VARIATION AG, DATED 06/01/76.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

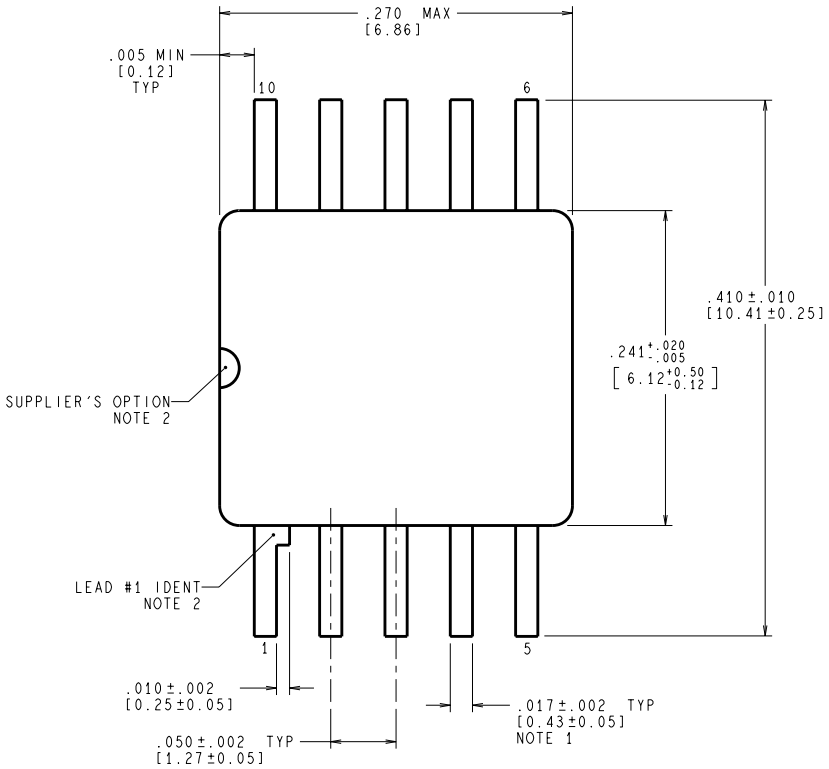
CERPACK, 10 LEAD

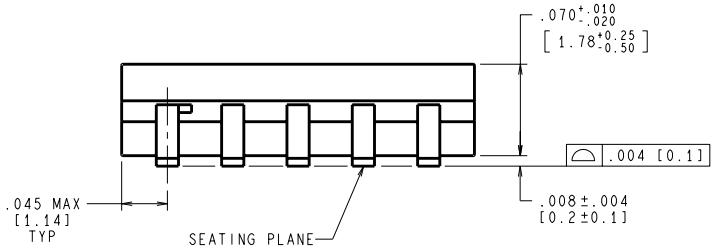
PROJECTION — INCH [MM]

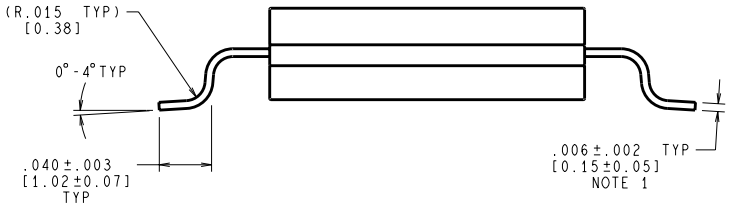
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W10A	G

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 10 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003685	05/22/00	Rose Malone	Initial MDS Release: MRLM111-X-RH, Rev. 0A0
0B0	M0003692	04/08/02	Rose Malone	Update MDS: MRLM111-X-RH, Rev. 0A0 to MRLM111-X-RH, Rev. 0B0. Typo in Recommended Operating Section.
0C0	M0003988	03/10/03	Rose Malone	Update MDS: MRLM111-X-RH, Rev. 0B0 to MRLM111-X-RH, Rev. 0C0. Deleted reference for the following NSID's from Main Table, Features Section and Graphics Section. LM111HPQML , LM111HPQMLV, LM111J-8PQML, LM111WGPQML product un-available.
0D1	M0004136	06/11/04	Rose Malone	Update MDS: MRLM111-X-RH, Rev. 0C0 to MRLM111-X-RH, Rev. 0D1. Added W package reference to Main Table, Features Section, Absolute Maximum Ratings Section and Graphics Section.
0E1	M0004387	06/11/04	Rose Malone	Update MDS: MRLM111-X-RH, Rev. 0D1 to REV. 0E1. Added to Main Table, Features Section, Absolute Maximum Ratings Section and Graphics Section information pertaining to NSID: LM111HPQMLV