

**MN54F14-X REV 2A0**

 Original Creation Date: 03/12/96  
 Last Update Date: 07/22/03  
 Last Major Revision Date: 06/02/03

**HEX INVERTER SCHMITT TRIGGER**
**General Description**

The F14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800 mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

**Industry Part Number**

54F14

**Prime Die**

M014

**NS Part Numbers**

 54F14DM-MLS  
 54F14DMQB.  
 54F14FMQB.  
 54F14LMQB.

**Controlling Document**

SEE FEATURES SECTION

**Processing**

MIL-STD-883, Method 5004

**Quality Conformance Inspection**

MIL-STD-883, Method 5005

Subgrp	Description	Temp ( °C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

**Features**

- Guaranteed 4000V minimum ESD protection

CONTROLLING DOCUMENTS:

54F14DMQB.	5962-8875201CA
54F14FMQB.	5962-8875201DA
54F14LMQB.	5962-88752012A

**(Absolute Maximum Ratings)**

(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Junction Temperature under Bias	-55 C to +175 C
Vcc Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0mA
Voltage Applied to Output in HIGH State (with Vcc=0V)	
Standard Output	-0.5V to Vcc
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated Iol(mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute Maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Commercial	0 C to +70 C
Military	-55 C to +125 C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## Electrical Characteristics

### DC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC: VCC 4.5V to 5.5V, Temp range: -55C to 125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input High Current	VCC=5.5V, VM=2.7V	1, 3	INPUTS		20	uA	1, 2, 3
IBVI	Input High Current	VCC=5.5V, VM=7.0V	1, 3	INPUTS		100	uA	1, 2, 3
IIL	Input LOW Current	VCC=5.5V, VM=0.5V	1, 3	INPUTS		-0.6	mA	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, VIH=2.0V, IOL=20mA	1, 3	OUTPUTS		0.5	V	1, 2, 3
VOH	Output HIGH Voltage	VCC=4.5V, VIL=0.7V, IOH=-1.0mA	1, 3	OUTPUTS	2.5		V	1, 2, 3
IOS	Short-Circuit Current	VCC=5.5V, VM=0.0V	1, 3	OUTPUTS	-60	-150	mA	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IM=-18mA	1, 3	INPUTS		-1.2	V	1, 2, 3
VT+	Positive-Going Threshold	VCC= 5.0V	1, 3	INPUTS	1.4	2.0	V	1, 2, 3
VT-	Negative-Going Threshold	VCC=5.0V	1, 3	INPUTS	0.7	1.1	V	1, 2, 3
VT	Hysteresis	VCC=5.0V	1, 3	INPUTS	0.3		V	1, 2, 3
ICCH	Supply Current	VCC=5.5V	1, 3	VCC		25	mA	1, 2, 3
ICCL	Supply Current	VCC=5.5V	1, 3	VCC		25	mA	1, 2, 3
ICEX	Output HIGH Leakage Current	VCC=5.5V, VINL=0.0V, VINH=5.5V, VM=5.5V	1, 3	OUTPUTS		250	uA	1, 2, 3

### AC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)  
AC: CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns SEE AC FIGS

tpLH	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C	2, 5	In to $\bar{O}$ n	4.0	11.0	ns	9
			2, 5	In to $\bar{O}$ n	4.0	13.0	ns	10, 11
tpHL	Propagation Delay	VCC=5.0V @25C, VCC=4.5V & 5.5V @-55/125C	2, 5	In to $\bar{O}$ n	3.5	8.0	ns	9
			2, 5	In to $\bar{O}$ n	3.5	10.0	ns	10, 11

Note 1: Screen tested 100% on each device at +25C, +125C & -55C temperature, subgroups A1, 2, 3, 7 & 8.

Note 2: Screen tested 100% on each device at +25C temperature only, subgroup A9.

**(Continued)**

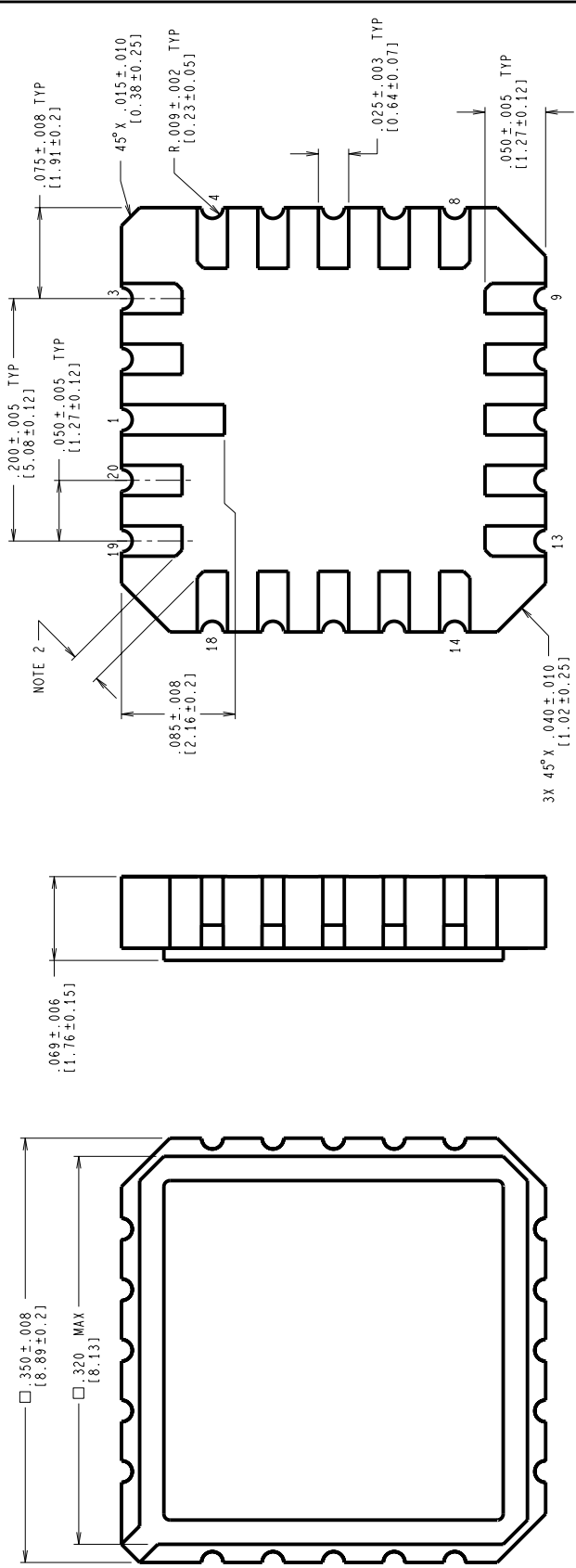
- Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C & -55C temperature, subgroups A1, 2, 3, 7 & 8.
- Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C subgroup A9, and at +125C & -55C temperature, subgroups 10 & 11.
- Note 5: Sample tested (Method 5005, table 1) on each MFG. lot at +25C, +125C & -55C, subgroups A9, A10 & A11.

## Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
W14BRN	CERPACK (W), 14 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
E	REVISE AND REDRAW	10005	02/10/94 DEG/

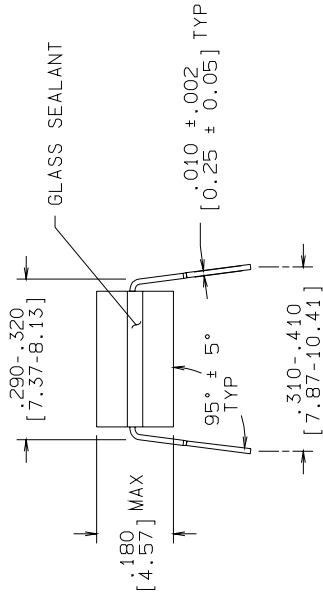
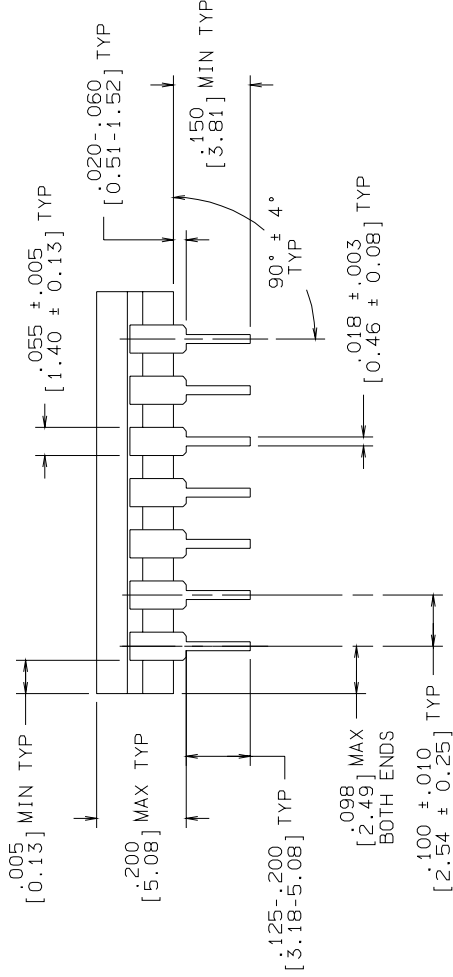
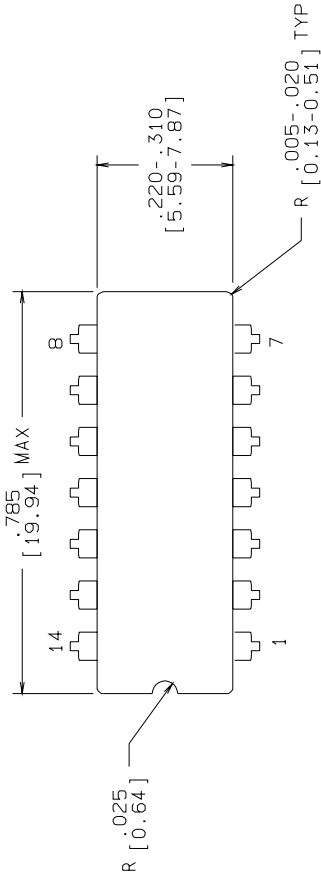


- NOTES: UNLESS OTHERWISE SPECIFIED.
- LEAD FINISH TO BE ONE OF THE FOLLOWING:
    - 50 MICRONS/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICRONS/1.27-8.89 MICROMETERS NICKEL.
    - SOLDER DIP. SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.
  - CORNER PADS MAY HAVE A  $45^\circ$  X  $0.20$  IN/  $0.51$  mm MAXIMUM CHAMFER TO ACCOMPLISH THE  $0.15$  IN/  $0.38$  mm DIMENSION.
  - REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS

<b>MIL/AERO</b> <b>CONFIGURATION CONTROL</b>		<b>NATIONAL SEMICONDUCTOR CORPORATION</b> <small>2300 Semiconductor Drive, Santa Clara, Ca. 95052-8090</small>	
		<b>LEADLESS CHIP CARRIER,</b> <b>TYPE C,</b> <b>20 TERMINAL</b>	
<b>APPROVALS</b> <small>DRN: Deane Gedy</small> <small>DFTG: CHK.</small> <small>ENGR: CHK.</small> <small>APPROVAL:</small>	<b>DATE</b> 02/10/94	<b>SCALE</b> N/A	<b>SIZE</b> C
	<b>DRAWING NUMBER</b> MKT-E20A	<b>REV</b> E	<b>SHEET</b> 1 of 1

R E V I S I O N S			
LTR	DESCRIPTION	E.C.N.	DATE
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93
			TL/



CONTROLLING DIMENSION: INCH

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICRONS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

MIL/AERO MIL-M-38510  
 CONFIGURATION CONTROL CONFIGURATION CONTROL

APPROVALS	DATE	APPROVALS	DATE
DRAWN: <b>T. LEQUANG</b>	09/15/93	NATIONAL SEMICONDUCTOR CORPORATION	
DFTG. CHK.		2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
ENGR. CHK.			
APPROVAL			
 PROJECTION INCH [MM]		SCALE	SIZE
		N/A	B
		DO NOT SCALE DRAWING	SHEET 1 OF 1
		DRAWING NUMBER	REV
		MKT-J14A	H
		CERDIP (J), 14 LEAD,	



**Revision History**

Rev	ECN #	Rel Date	Originator	Changes
1B0	M0004025	07/22/03	Rose Malone	Update MDS: MN54F14-X, Rev. 1A0 to MN54F14-X, Rev. 1B0. Updated NS Part Numbers on Main Table, Added Mkt Dwg.'s to Graphics Section.
2A0	M0004172	07/22/03	Rose Malone	Update MDS: MN54F14-X, Rev. 1B0 to 2A0. Changed DC Electrical Section, Parameter VT limit from 0.4V to 0.3V, typo error.