

MNDS96F173M-X REV 0A0

Original Creation Date: 01/25/96
Last Update Date: 01/30/96
Last Major Revision Date: 01/25/96

RS-485 DIFFERENTIAL LINE RECEIVER

General Description

The DS96F173 is a high speed quad differential line receiver designed to meet EIA Standard RS-485. The DS96F173 offers improved performance due to the use of state-of-the-art L-Fast bipolar technology. The L-Fast technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS96F173 features lower power and an extended temperature range.

The DS96F173 has TRI-STATE(TM) outputs and is optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200mV over a common mode input voltage range of -7V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96F173 features an active high and active low Enable, common to all four receivers.

Compatible RS-485 drivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96F172, DS96F174 and DS16F95.

Industry Part Number

DS96F173

NS Part Numbers

DS96F173ME/883 *
DS96F173MJ/883 **
DS96F173MW/883 ***

Prime Die

M173

Controlling Document

9076602M2A*, MEA**, MFA***

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Meets EIA Standard RS-485, RS-422A, RS-423A
- Designed for multipoint bus applications
- TRI-STATE outputs
- Common mode input voltage range: -7V to +12V
- Operates from single +5.0V supply
- Lower power version
- Input sensitivity of $\pm 200\text{mV}$ over common mode range
- Input hysteresis of 50mV typical
- High input impedance
- DS96F173 and DS96F175 are lead and function compatible with SN75173/175 or the AM26LS32/MC3486

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature Range Ceramic DIP	-65 C to +175 C
Lead Temperature (Soldering, 60 sec.)	300 C
Maximum Power Dissipation at 25 C (Note 2)	
Ceramic J Package	1500mW
Ceramic W Package	1034mW
Ceramic E Package	1500mW
Supply Voltage	7.0V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7.0V
Low Level Output Current	50mA

Note 1: "Absolute maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Derate J package 10mW/ C above 25C; Derate E package 11.11mW/ C above 25 C; Derate W package 6.90mW/ C above 25 C.

Recommended Operating Conditions

Supply Voltage (Vcc)	Min.	Typ.	Max.	Units
	4.50	5.0	5.50	V
Common Mode Input Voltage Vcm	Min.	Typ.	Max.	Units
	-7		+12	V
Differential Input Voltage(Vid)	Min.	Typ.	Max.	Units
	-7		+12	V
Output Current HIGH(Ioh)	Min.	Typ.	Max.	Units
			-400	uA
Output Current LOW(Iol)	Mix.	Typ.	Max.	Units
			16	mA
Operating Temperature (TA)	Min.	Typ.	Max.	Units
	-55	25	125	C

Electrical Characteristics

DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V_{cc} = 5.0V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc	Supply Current	$V_{cc} = 5.5V, V_{en} = 0V, V_{id} = 2V, V_{en} = 2V$	1			50	mA	1, 2, 3
Voh	Logical "1" Output Voltage	$V_{cc} = 4.5V, I_{oh} = -400\mu A, V_{id} = 0.2V$	2, 3		2.5		V	1, 2, 3
Vol	Logical "0" Output Voltage	$V_{cc} = 4.5V, I_{ol} = 8mA, V_{id} = -0.2V$	2, 3			0.45	V	1, 2, 3
Vth	Diff. Input Threshold Voltage	$V_{cc} = 4.5V, V_{cm} = 0V$	4, 5			0.2	V	1, 2, 3
		$V_{cc} = 5.5V, V_{cm} = 0V$	4, 5			0.2	V	1, 2, 3
		$V_{cc} = 4.5V, V_{cm} = -12V$	4, 5			0.2	V	1, 2, 3
		$V_{cc} = 5.5V, V_{cm} = -12V$	4, 5			0.2	V	1, 2, 3
		$V_{cc} = 4.5V, V_{cm} = 12V$	4, 5			0.2	V	1, 2, 3
		$V_{cc} = 5.5V, V_{cm} = 12V$	4, 5			0.2	V	1, 2, 3
Vtl	Diff. Input Threshold Voltage	$V_{cc} = 4.5V, V_{cm} = 0V$	4, 6		-0.2		V	1, 2, 3
		$V_{cc} = 5.5V, V_{cm} = 0V$	4, 6		-0.2		V	1, 2, 3
		$V_{cc} = 4.5V, V_{cm} = -12V$	4, 6		-0.2		V	1, 2, 3
		$V_{cc} = 5.5V, V_{cm} = -12V$	4, 6		-0.2		V	1, 2, 3
		$V_{cc} = 4.5V, V_{cm} = 12V$	4, 6		-0.2		V	1, 2, 3
		$V_{cc} = 5.5V, V_{cm} = 12V$	4, 6		-0.2		V	1, 2, 3
Ii	Input Line Current	$V_{cc} = 4.5V, V_{in} = 12V$ (Untested)	2			1.0	mA	1, 2, 3
		$V_{cc} = 5.5V, V_{in} = -7V$ (Input are 0V)	2		-0.8		mA	1, 2, 3
Iih	Logical "1" Enable Input Current	$V_{cc} = 5.5V, V_{ih} = 2.7V$				10	μA	1, 2, 3
Iil	Logical "0" Enable Input Current	$V_{cc} = 5.5V, V_{il} = 0.4V$			-100		μA	1, 2, 3

Electrical Characteristics

DC PARAMETERS: (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V_{cc} = 5.0V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ios	Output Short Circuit Current	$V_{cc} = 4.5V, V_o = 0V$	2		-85	-15	mA	1, 2, 3
		$V_{cc} = 5.5V, V_o = 0V$	2		-85	-15	mA	1, 2, 3
Vik	Enable Input Clamp Voltage	$V_{cc} = 4.5V, I_i = -18mA$			-1.5		V	1, 2, 3
Ioz	High Impedance Output Current	$V_{cc} = 5.5V, V_{en} = 0.8V$ (O/P Disabled), $V_{en} = 2V, V_{out} = 0.4V$			-20	20	uA	1, 2, 3
		$V_{cc} = 5.5V, V_{en} = 0.8V$ (O/P Disabled), $V_{en} = 2V, V_{out} = 2.4V$			-20	20	uA	1, 2, 3
Vih	Logical "1" Enable Input Voltage		7		2.0		V	1, 2, 3
Vil	Logical "0" Enable Input Voltage		8			0.8	V	1, 2, 3
Rin	Input Resistance				10		K Ohms	1, 2, 3
tPLH	Propagation Delay Time	Cl = 15pF				22	nS	1
						30	nS	2, 3
tPHL	Propagation Delay Time	Cl = 15pF				22	nS	1
						30	nS	2, 3
tPZH	Propagation Delay Time	Cl = 15pF				16	nS	1
						27	nS	2, 3
tPZL	Propagation Delay Time	Cl = 15pF				18	nS	1
						27	nS	2, 3
tPHZ	Propagation Delay Time	Cl = 5pF	9			20	nS	1
			9			27	nS	2, 3
		Cl = 20pF	9			30	nS	1
			9			37	nS	2, 3
tPLZ	Propagation Delay Time	Cl = 5pF				18	nS	1
						30	nS	2, 3
tPW	Pulse Width					3	nS	1
						8	nS	2
						5	nS	3

(Continued)

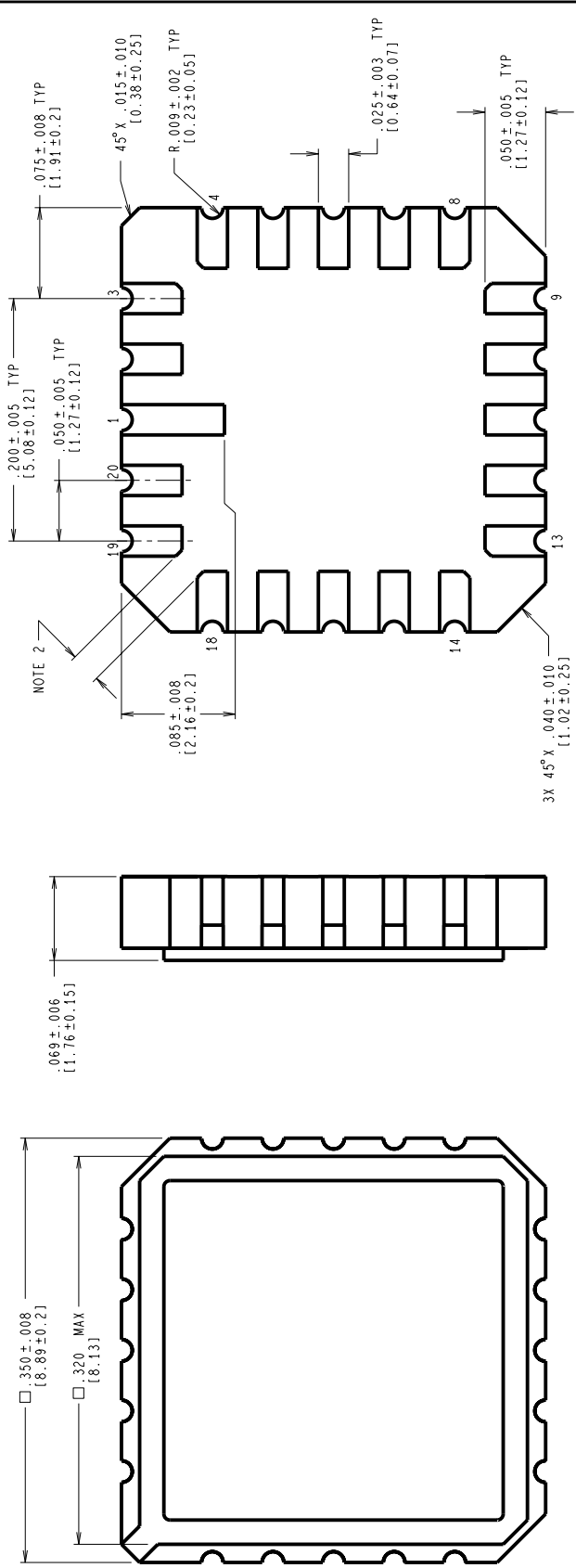
- Note 1: Icc is tested with outputs disabled (worst case); Icc enabled is guaranteed by this test.
- Note 2: Ven, Ven=2V. Voh and Vol are tested over the Common Mode Voltage Range of +/-12V via the Vth/Vtl tests.
- Note 3: Ven, Ven=0V.
- Note 4: Ven=2.5V, Ven=0.0V.
- Note 5: Vo=2.5V, Io= -400uA.
- Note 6: Vo=0.5V, Io=16mA.
- Note 7: Guaranteed by Vol and Voh tests.
- Note 8: Guaranteed by Ioz test.
- Note 9: Testing at 20pF assures conformance to spec at 5pF.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LDLESS CHIP CARRIER, TYPE C 20 TERMINAL(P/P DWG)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
W16ARL	CERPAC (W), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
E	REVISE AND REDRAW	10005	02/10/94 DEG/



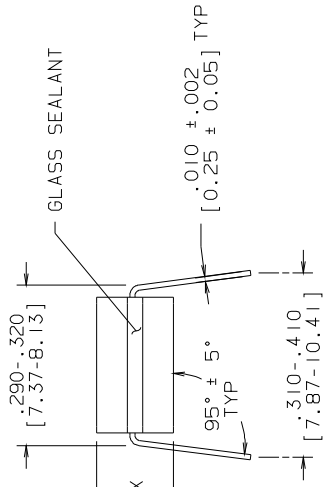
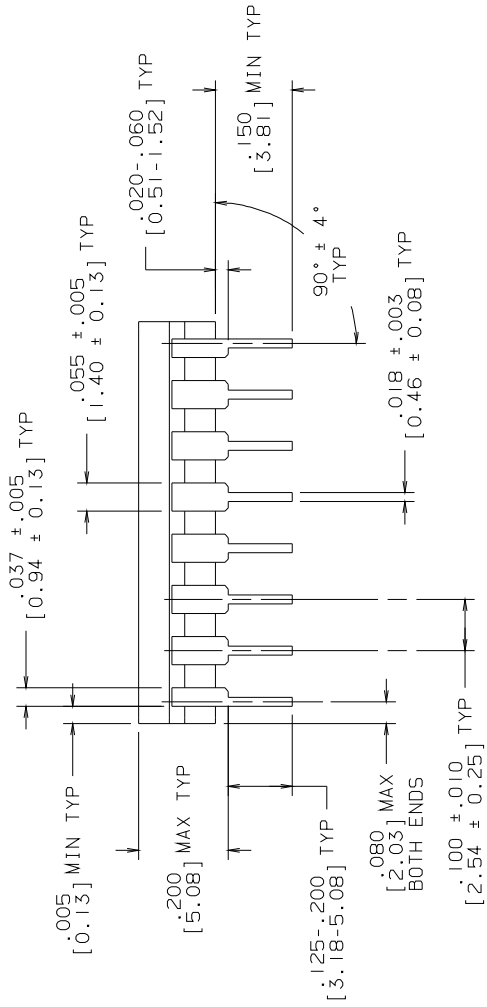
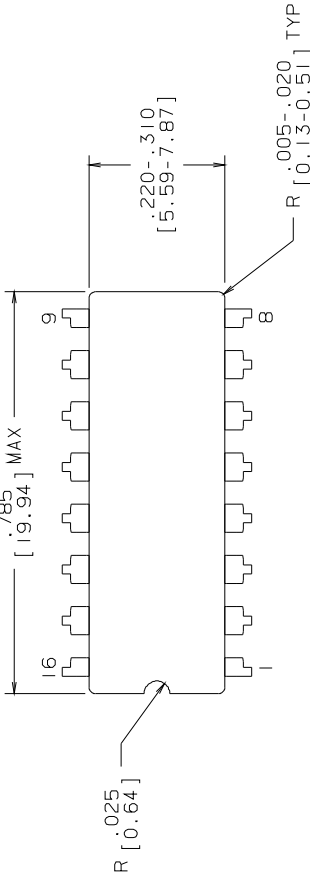
CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

- LEAD FINISH TO BE ONE OF THE FOLLOWING:
 - 50 MICRONS/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICRONS/1.27-8.89 MICROMETERS NICKEL.
 - SOLDER DIP.
 - SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.
- CORNER PADS MAY HAVE A 45° X 0.20 IN/ 0.51 mm MAXIMUM CHAMFER TO ACCOMPLISH THE 0.015 IN/ 0.38 mm DIMENSION.
- REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO CONFIGURATION CONTROL	
NATIONAL SEMICONDUCTOR CORPORATION 2300 Semiconductor Drive, Santa Clara, Ca. 95052-8000	
APPROVALS	DATE
DRN: <i>Deane Gedy</i>	02/10/94
DFTG: CHK.	
ENGR: CHK.	
APPROVAL	
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL	
SCALE	SIZE
N/A	C
DRAWING NUMBER MKT-E20A	
DO NOT SCALE DRAWING	REV E
SHEET 1 of 1	

R E V I S I O N S			
LTR	DESCRIPTION	E. C. N.	DATE
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93
			TL/



MILIAERO MIL-M-38510
 CONFIGURATION CONTROL CONFIGURATION CONTROL

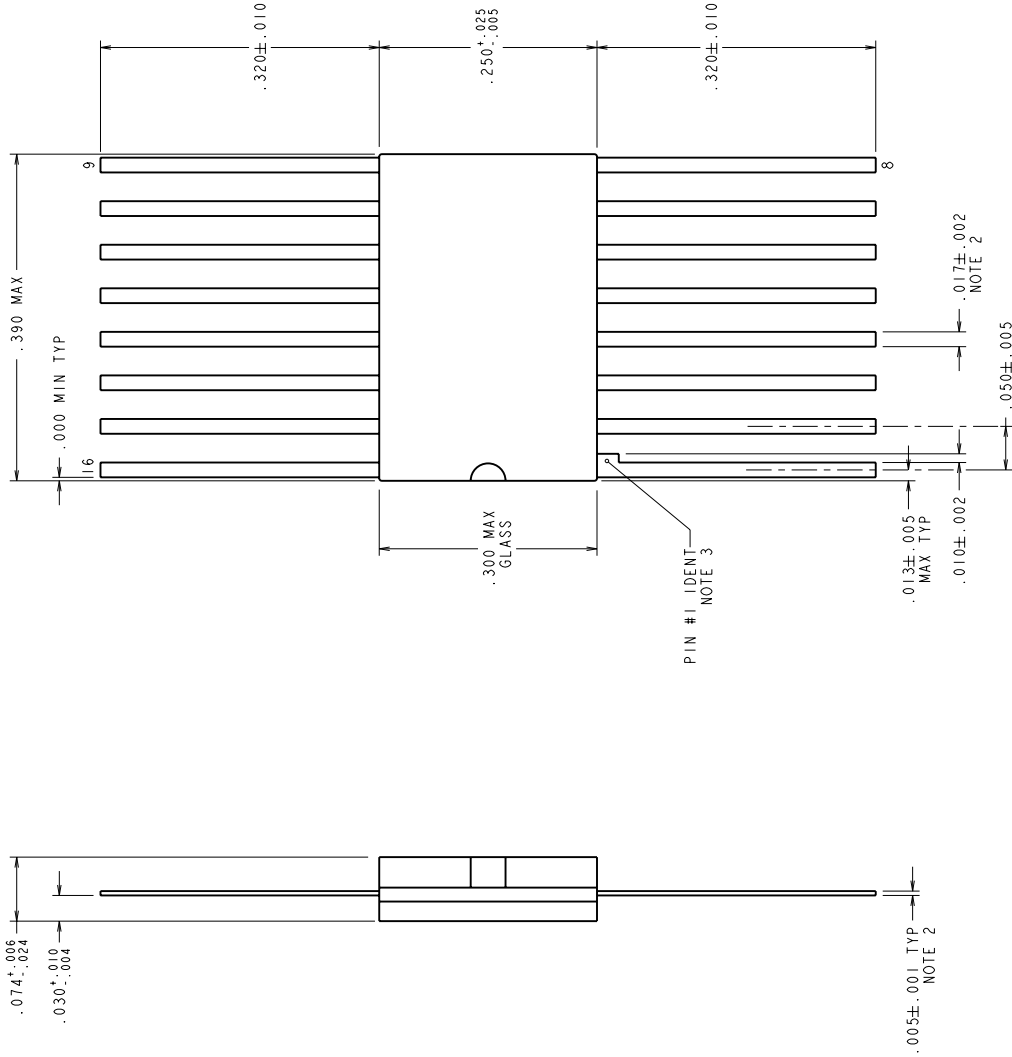
CONTROLLING DIMENSION: INCH	
APPROVALS	DATE
DRAWN <i>T. LEQUANG</i>	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	
PROJECTION  INCH [MM]	
SCALE N/A	SIZE B
DRAWING NUMBER MKT-J16A	REV L
DO NOT SCALE DRAWING	SHEET 1 OF 1

NATIONAL SEMICONDUCTOR CORPORATION
 2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J),
 16 LEAD

- NOTES: UNLESS OTHERWISE SPECIFIED
- LEAD FINISH TO BE 200 MICROMETERS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
 - JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
K	REVISE AND REDRAW PER NEW STANDARD.	10514	07/28/94
L	.017±.002 WAS .017±.020.	10656	10/21/94



NOTES: UNLESS OTHERWISE SPECIFIED.

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
- MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
- LEAD 1 IDENTIFICATION SHALL BE:
 - A NOTCH OR OTHER MARK WITHIN THIS AREA
 - A TAB ON LEAD 1, EITHER SIDE
- REFERENCE JEDEC REGISTRATION M0-092, VARIATION AC, DATED 04/89.

MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

APPROVALS		DATE	
DRWN	<i>D. F. Grady</i>		07/28/94
DTG. CHK.			
ENGR. CHK.			

PROJECTION			

National Semiconductor			
2800 Semiconductor dr., Santa Clara, CA 95052-8090			
SCALE		DRAWING NUMBER	
N/A		MKT-W16A	
DO NOT SCALE DRAWING		SHEET 1 of 1	