National Semiconductor

February 2001

CLC420
High Speed, Voltage Feedback Op Amp

General Description

The CLC420 is an operational amplifier designed for applications requiring matched inputs, integration or transimpedance amplification. Utilizing voltage feedback architecture, the CLC420 offers a 300MHz bandwidth, a 1100V/µs slew rate and a 4mA supply current (power consumption of 40mW,±5V supplies).

Applications such as differential amplifiers will benefit from 70dB common mode rejection ratio and an input offset current of 0.2µA. With its unity-gain stability, 2pA/$\sqrt{Hz}$ current noise and 3µA of input bias current, the CLC420 is designed to meet the needs of filter applications and log amplifiers. The low input offset current and current noise, combined with a settling time of 18ns to 0.01% make the CLC420 ideal for D/A converters, pin diode receivers and photo multipliers amplifiers. All applications will find 70dB power supply rejection ratio attractive.

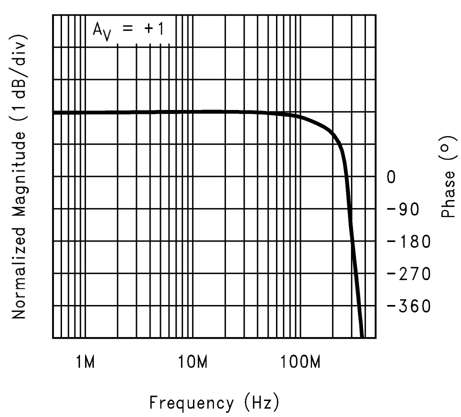
Features

- 300MHz small signal bandwidth
- 1100V/µs slew rate
- Unity-gain stability
- Low distortion, -60dBc at 20MHz
- 0.01% settling in 18ns
- 0.2µA input offset current
- 2pA$\sqrt{Hz}$ current noise

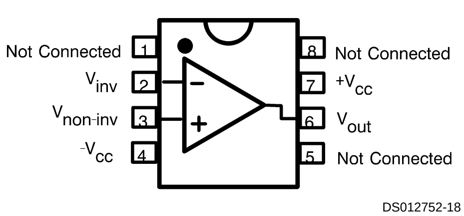
Applications

- Active filters/integrators
- Differential amplifiers
- Pin diode receivers
- Log amplifiers
- D/A converters
- Photo multiplier amplifiers

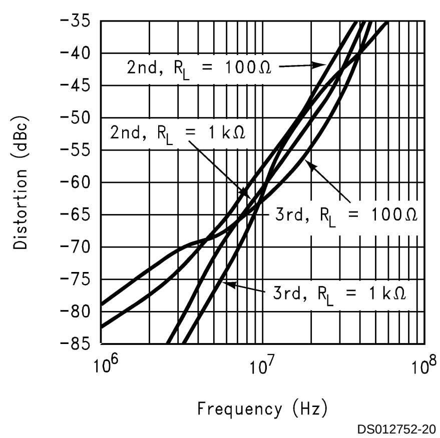
Non-Inverting Frequency Response



Connection Diagram



Pinout
DIP & SOIC



2nd and 3rd Harmonic Distortion

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	−40˚C to +85˚C	CLC420AJP	CLC420AJP	N08E
8-pin plastic SOIC	−40˚C to +85˚C	CLC420AJE	CLC420AJE	M08A
		CLC420AJE-TR13	CLC420AJE	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	±7V
I_{OUT} (is short circuit protected to ground, but maximum reliability will be maintained if I_{OUT} does not exceed 70mA, except A8D, B8D which should not exceed 35mA over the military temperature range)..	70mA
Common Mode Input Voltage	$\pm V_{CC}$
Differential Input Voltage	10V
Junction Temperature	+150˚C
Operating Temperature Range	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Solder Duration (+300˚C)	10 sec

Operating Ratings

Thermal Resistance

Package	(θ_{JC})	(θ_{JA})
MDIP	65˚C/W	120˚C/W
SOIC	60˚C/W	140˚C/W

Electrical Characteristics

$A_V = +1$, $V_{CC} = \pm5V$, $R_L = 100\Omega$, $R_f = 0\Omega$; unless specified

Symbol	Parameter	Conditions	Typ	Max/Min (Note 2)			Units
Ambient Temperature		CLC420AJ	+25˚C	−40˚C	+25˚C	+85˚C	
Frequency Domain Response							
SSBW	-3dB Bandwidth	$V_{OUT} < 0.4V_{PP}$	300	>200	>200	>130	MHz
LSBW		$V_{OUT} < 5V_{PP}$	40	>20	>25	>20	MHz
SSBWI	$A_V = -1$, $R_f = 500\Omega$	$V_{OUT} < 0.4V_{PP}$	100	>65	>65	>45	MHz
LSBWI	$A_V = -1$, $R_f = 500\Omega$	$V_{OUT} < 5V_{PP}$	60	>30	>35	>30	MHz
	Gain Flatness	$V_{OUT} < 0.4V_{PP}$					
GFPL	Peaking	0.1MHz to 100MHz	0	<1	<0.6	<0.6	dB
GFPH	Peaking	>100MHz	0	<5	<3	<3	dB
GFR	Rolloff	0.1MHz to 100MHz	0.2	<1	<1	<2	dB
GFRI	Rolloff, $A_V = -1$, $R_f = 500\Omega$	0.1MHz to 30MHz	0.2	<1.4	<1.4	<1.6	dB
LPD	Linear Phase Deviation	0.1MHz to 100MHz	0.9	<1.8	<1.8	<2.5	deg
Time Domain Response							
TRS	Rise and Fall Time	0.4V Step	1.2	<2	<2	<3	ns
TRL		5V Step	1.4	<25	<20	<20	ns
TRSI	Rise and Fall Time, $A_V = -1$, $R_f = 500\Omega$	0.4V Step	3.5	<5.5	<5.5	<7.8	ns
TRLI		5V Step	6	<10	<9.5	<10	ns
TSS	Settling Time to ±0.1%	2V Step	12	<18	<18	<18	ns
TSP	±0.01%	2V Step	18	<25	<25	<25	ns
OS	Overshoot	0.4V Step	8	<35	<25	<25	%
SR	Slew Rate, $A_V = +2$	5V Step	1100	>600	>750	>600	V/µs
SRI	Slew Rate, $A_V = -1$, $R_f = 500\Omega$	5V Step	750	>430	>500	>430	V/µs
Distortion And Noise Response							
HD2	2nd Harmonic Distortion	$2V_{PP}$, 20MHz	−50	<−40	<−40	<−40	dBc
HD3	3rd Harmonic Distortion	$2V_{PP}$, 20MHz	−53	<−45	<−45	<−40	dBc
HD2	2nd Harmonic Distortion	$A_V = -1$ $2V_{PP}$, 20MHz, $R_f = 500\Omega$	−51	<−40	<−40	<−40	dBc
HD3	3rd harmonic distortion	$A_V = -1$, $R_f = 500\Omega$ $2V_{PP}$, 20MHz, $R_f = 500\Omega$	−51	<−40	<−40	<−35	dBc
	Input Referred Noise						
VN	Voltage	1MHz to 200MHz	4.2	<5.3	<5.3	<6	$nV/\sqrt{Hz}$
ICN	Current	1MHz to 200MHz	2	<2.9	<2.6	<2.3	$pA/\sqrt{Hz}$
Static DC Performance							
VIO	Input Offset Voltage (Note 3)		1	<3.2	<2	<3.5	mV

Electrical Characteristics (Continued)

A_V = +1, V_{CC} = ±5V, R_L = 100Ω, R_f = 0Ω; unless specified

Symbol	Parameter	Conditions	Typ	**Max/Min** (Note 2)			Units
Static DC Performance							
DVIO	Average Temperature Coefficient		8	<15	-	<15	μV/˚C
IB	Input Bias Current (Note 3)		3	<20	<10	<10	μA
DIB	Average Temperature Coefficient		45	<120	-	<60	nA/˚C
IIO	Input Offset Current (Note 3)		0.2	<2.6	<1	<2	μA
DIIO	Average Temperature Coefficient		2	<20	-	<10	nA/˚C
AOL	Open Loop Gain (Note 3)		65	>52	>56	>56	μA
PSRR	Power Supply Rejection Ratio		70	>55	>60	>60	dB
CMRR	Common Mode Rejection Ratio		80	>60	>65	>65	dB
ICC	Supply Current (Note 3)	No Load, Quiescent	4	<5	<5	<5	mA
Miscellaneous Performance							
RIND	Differential Mode Input	Resistance	2	>0.5	>1	>1	MΩ
CIND		Capacitance	1	<2	<2	<2	pF
RINC	Common Mode Input	Resistance	1	>0.25	>0.5	>0.5	MΩ
CINC		Capacitance	1	<2	<2	<2	pF
RO	Output Impedence	At DC	0.02	<0.3	<0.2	<0.2	Ω
VO	Output Voltage Range	No Load	±3.6	±2.8	±3	±3	V
VOL	Output Voltage Range	RL = 100Ω	±2.9	±2.5	±2.5	±2.5	V
CMIR	Common Mode Input Range	For Rated Performance	±3.2	±2.5	±2.8	±2.8	V
IO	Output Current		±60	±30	±50	±50	mA

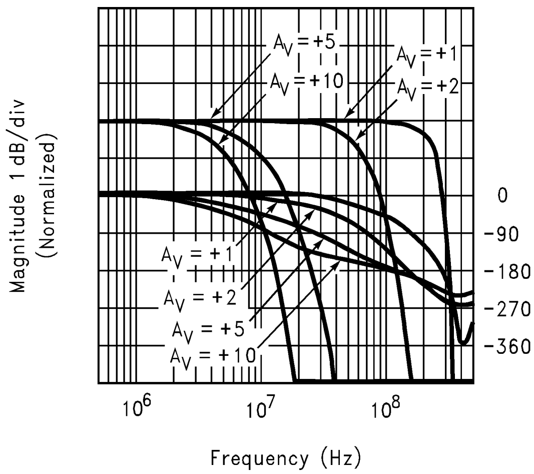
Note 1: “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.

Note 2: Max/min ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: AJ-level: spec. is 100% tested at +25˚C.

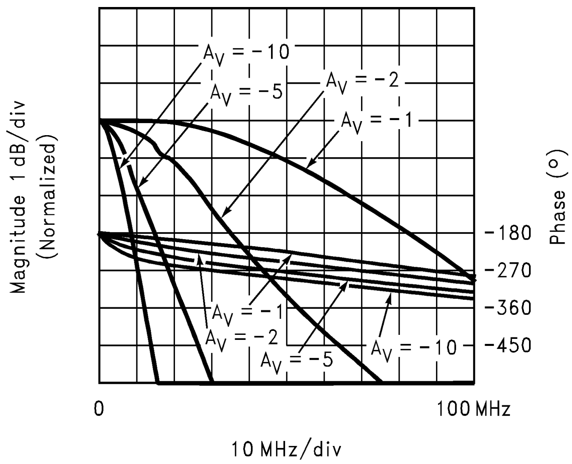
Typical Performance Characteristics

Non-Inverting Frequency Response



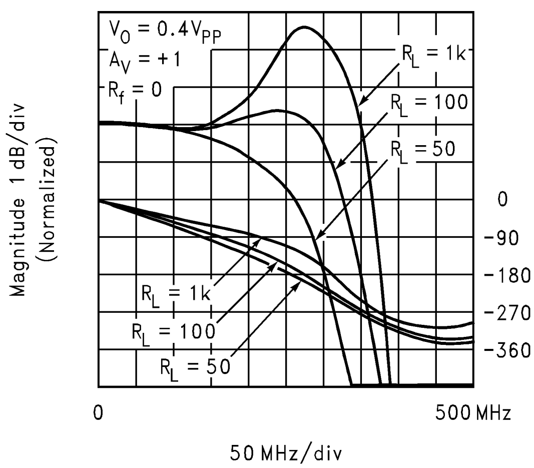
DS012752-1

Inverting Frequency Response



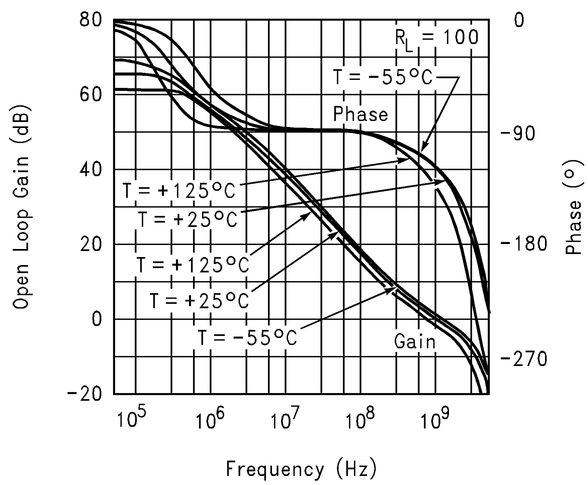
DS012752-2

Frequency Response for Various R_LS



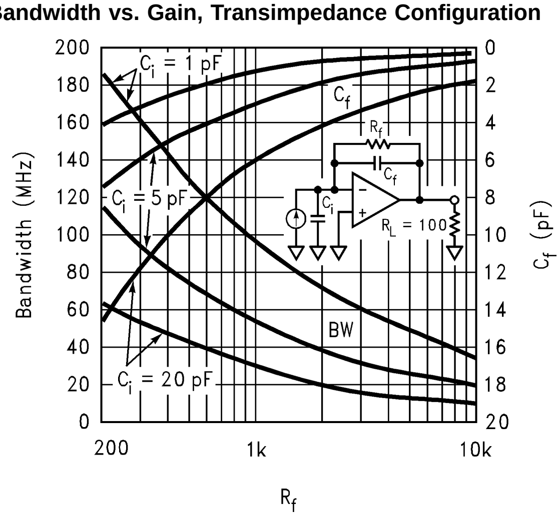
DS012752-3

Open Loop Gain and Phase



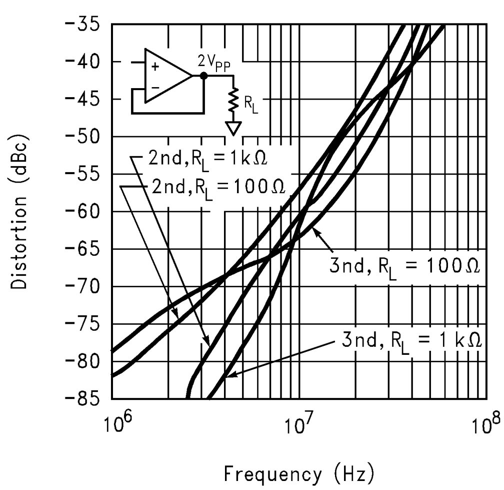
DS012752-4

Bandwidth vs. Gain, Transimpedance Configuration



DS012752-5

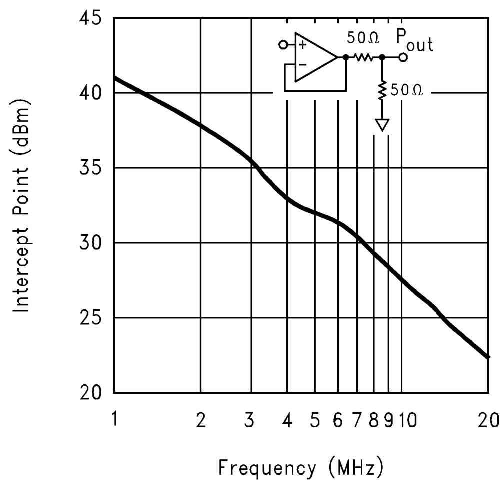
2nd and 3rd Harmonic Distortion



DS012752-6

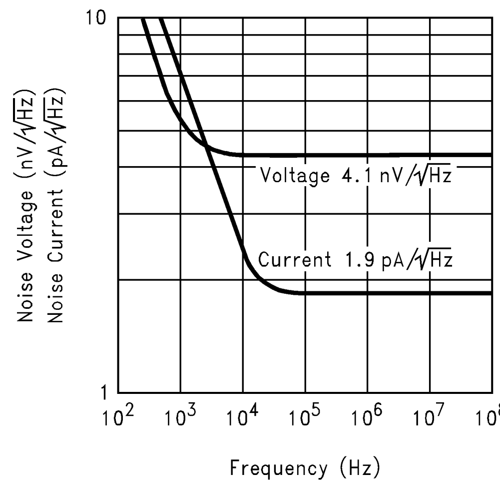
Typical Performance Characteristics (Continued)

2-Tone, 3rd Order Intermodulation Intercept



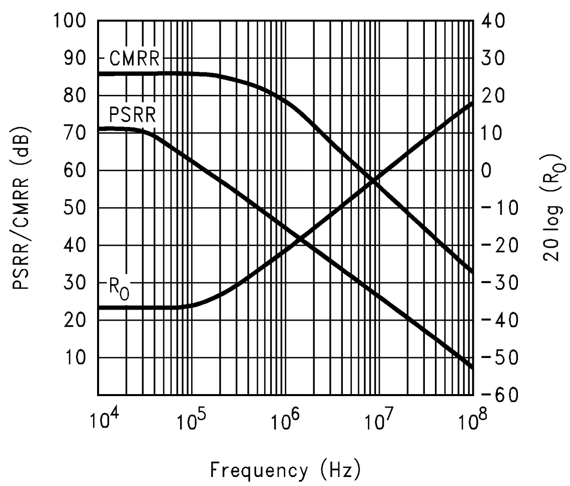
DS012752-7

Equivalent Input Noise



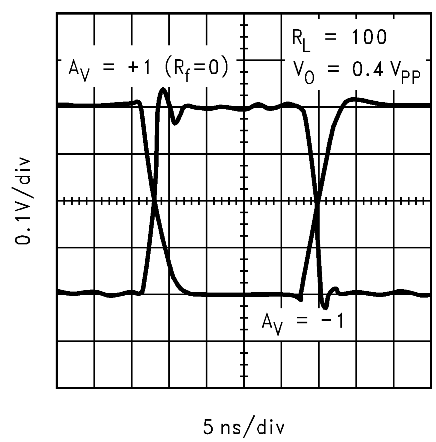
DS012752-8

PSRR, CMRR, and Closed Loop R_O



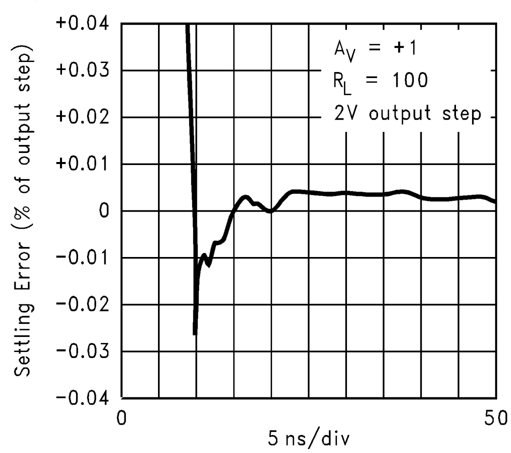
DS012752-9

Pulse Response



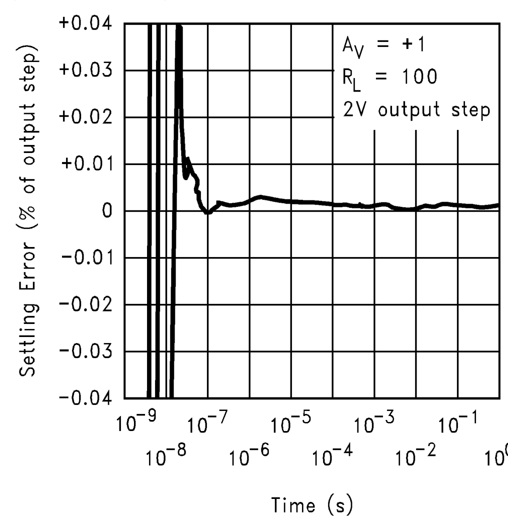
DS012752-10

Settling Time



DS012752-11

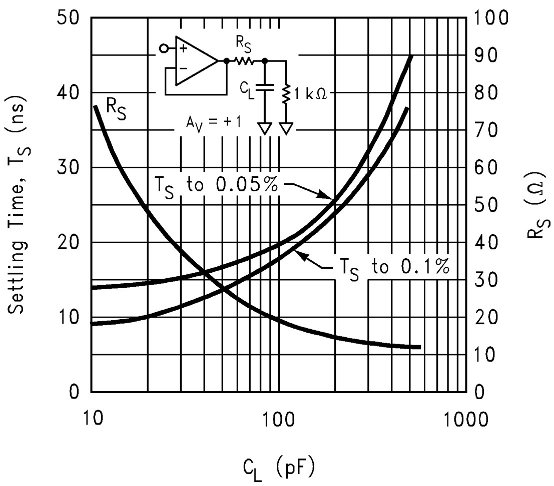
Long-Term Settling Time



DS012752-12

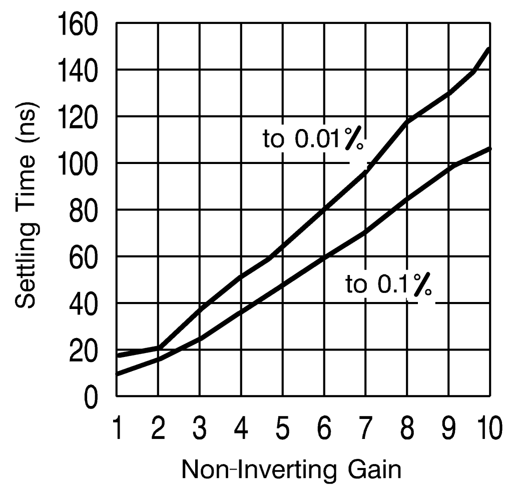
Typical Performance Characteristics (Continued)

Settling Time vs. Capacitive Load



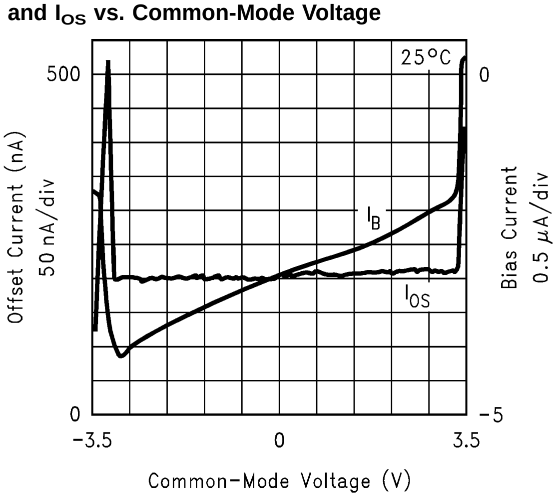
DS012752-13

Settling Time vs. Gain



DS012752-14

I_B and I_{OS} vs. Common-Mode Voltage



DS012752-15

Application Division

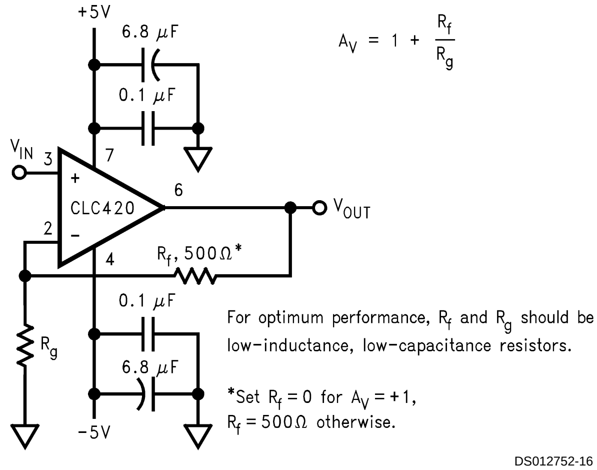


FIGURE 1. Recommended Non-Inverting Gain Circuit

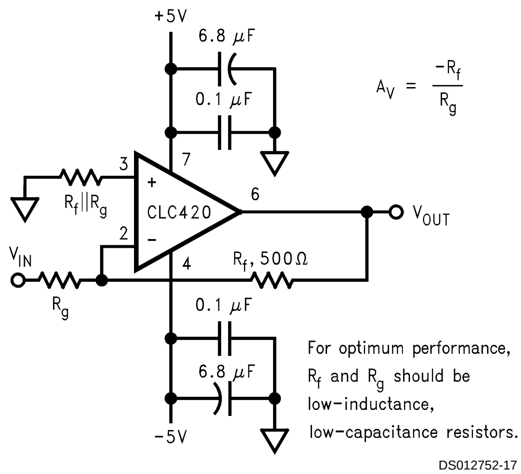


FIGURE 2. Recommended Inverting Gain Circuit

Description

The CLC420 is a high speed, slew boosted, voltage feedback amplifier with unity-gain stability. These features along with matched inputs, low input bias and noise currents, and excellent CMRR render the CLC420 very attractive for active filters, differential amplifiers, log amplifiers, and transimpedance amplifiers.

DC accuracy

Unlike current feedback amplifiers, voltage-feedback amplifiers have matched inputs. This means that the non inverting and inverting input bias current are well matched and track over temperature, etc. As a result, by matching the resistance looking out of the two inputs, these errors can be reduced to a small offset current term.

Gain bandwidth product

Since the CLC420 is a voltage feedback op amp, closed loop bandwidth is approximately equal to the gain bandwidth product (typically 100MHz) divided by the noise gain of the circuit (for noise gains greater than 5). At lower noise gains, higher order amplifier poles contribute to higher closed loop bandwidth. At low gains use the frequency response performance plots given in the data sheet.

Another point to remember is that the closed loop bandwidth is determined by the noise gain, not the signal gain of the circuit. Noise gain is the reciprocal of the attenuation in the feedback network enclosing the op amp. For example, a CLC420 setup as a non-inverting amplifier with a closed loop gain of +1 (a noise gain of 1) has a 300MHz bandwidth. When used as an inverting amplifier with a gain of −1 (a noise gain of 2), the bandwidth is less, typically only 100MHz.

Full-power bandwidth, and slew-rate

The CLC420 combines exceptional full power bandwidths (40MHz, V_o = 5Vpp, A_V = +1) and slew rates (1100V/µs, A_V = +1) with low (40mW) power consumption. These attractive results are achieved by using slew boosting circuitry to keep the slew rates high while consuming very little power.

In non slew boosted amplifiers, full power bandwidth can be easily determined from slew rate measurements, but in slew boosting amplifiers, such as the CLC420, you can't. For this reason we provide data for both.

Slew rate is also different for inverting and non-inverting configurations. This occurs because common-mode signal voltages are present in non-inverting circuits but absent in inverting circuits. Once again data is provided for both.

Application Division (Continued)

Transimpedance amplifier circuits

Low inverting, input current noise ($2pA/\sqrt{Hz}$) makes the CLC420 ideal for high sensitivity transimpedance amplifier circuits for applications such as pin diode optical receivers, and detectors in receiver IFs. However, feedback resistors 4kΩ or greater are required if feedback resistor noise current is going to be less than the input current noise contribution of the op amp.

With feedback resistors this large, shunt capacitance on the inverting input of the op amp (from the pin diode, etc.) will unacceptably degrade phase margin causing frequency response peaking or oscillations a small valued capacitor shunting the feedback resistor solves this problem (Note: This approach does not work for a current-feedback op amp configured for transimpedance applications). To determine the value of this capacitor, refer to the "Transimpedance BW vs. R_f and C_i" plot.

For example, let's assume an optical transimpedance receiver is being developed. Total capacitance from the inverting input to ground, including the photodiode and strays is 5pF. A 5kΩ feedback resistor value has been determined to provide best dynamic range based on the response of the photodiode and the range of incident optical powers, etc. From the "Transimpedance BW vs. R_f and C_i" plot, using C_i= 5pF it is determined from the two curves labeled C_i = 5pF, that C_f = 1.5pF provides optimal compensation (no more than 0.5dB frequency response peaking) and a −3dB bandwidth of approximately 27MHz.

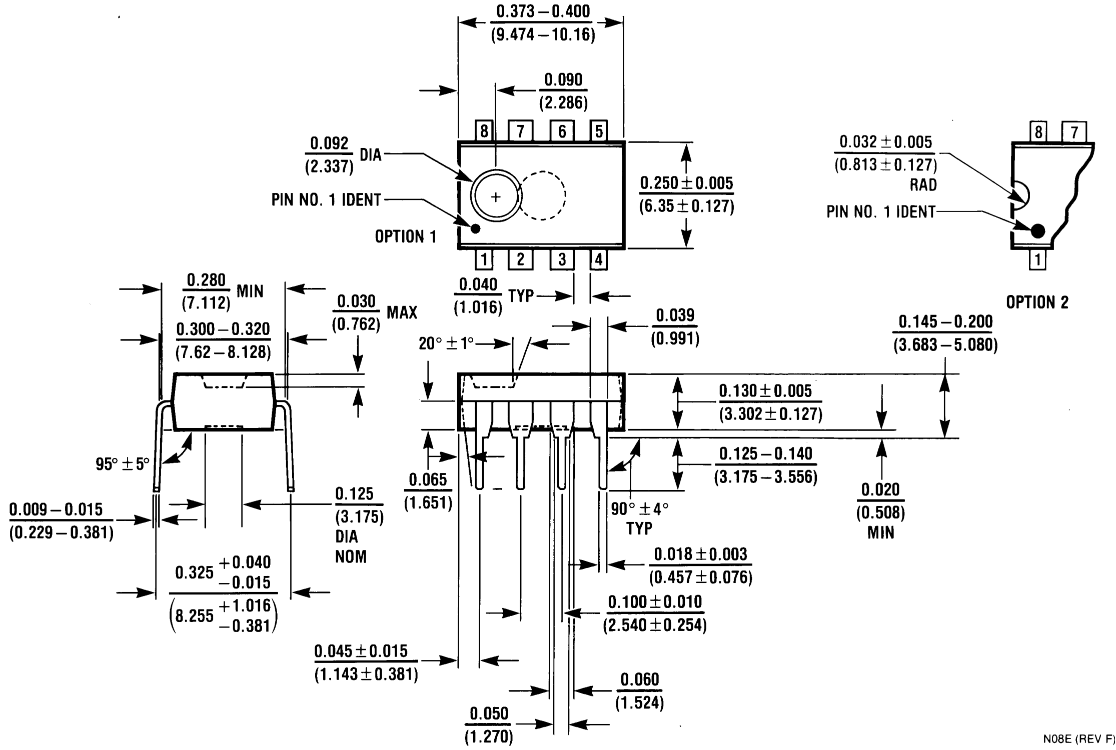
Printed circuit layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. The amplifier is sensitive to stray capacitance to ground at the output and inverting input: Node connections should be small with minimal coupling to the ground plane.

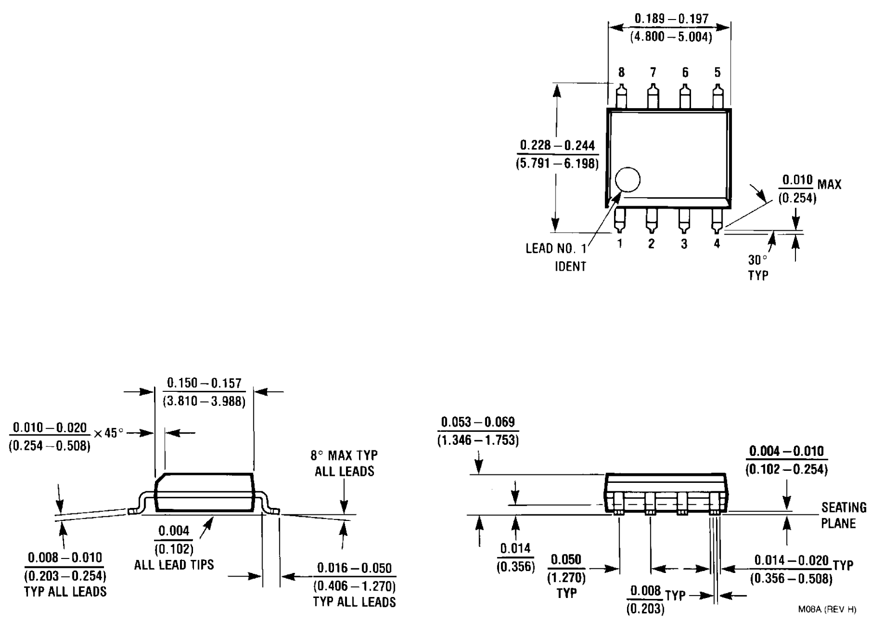
Parasitic or load capacitance directly on the output (pin 6) will introduce additional phase shift in the loop degrading the loop phase margin and leading to frequency response peaking. A small series resistor before this capacitance, if present, effectively decouples this effect. The graphs on the preceding page, " Settling Time vs. C_L", illustrates the required resistor value and resulting performance vs. capacitance.

Evaluation PC boards (part no. 730013 for through-hole and CLC730027 for SOIC) are available for the CLC420.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin MDIP
NS Package Number N08E



8-Pin SOIC
NS Package Number M08A

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507