National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC406A-X REV 0A0

Original Creation Date: 02/10/99
Last Update Date: 09/08/99
Last Major Revision Date:

WIDEBAND, LOW POWER MONOLITHIC OP AMP

General Description

The CLC406 is a wideband monolithic operational amplifier designed for low-gain applications where power and cost are of primary concern. Operating from ±5V supplies, the CLC406 consumes only 50mW of power yet maintains a 160MHz small signal bandwidth and a 1500V/us slew rate. Benefitting from Comlinear's current feedback architecture, the CLC406 offers a gain range of ± 1 to ± 10 while providing stable, oscillation free operation without external compensation, even at unity gain.

With its exceptional differential gain and phase, typically 0.02% and 0.02 degrees at 3.58MHz, the CLC406 is designed to meet the performance and cost requirements of high volume composite video applications. The CLC406's large signal bandwidth, high slew rate and high drive capability are features well suited for RGB video applications.

Providing a 12ns settling time to 0.05% (1/2 LSB in 10-bit systems) and -68/-75dBc 2nd/3rd harmonic distortion (2Vpp at 10MHz, Rl = 1kOhms), the CLC406 is an excellent choice as a buffer or driver for high speed A/D and D/A converter systems.

Commercial remote sensing applications and battery powered radio transceivers requiring a high performance, low power amplifier will find the CLC406 to be an attractive, cost-effective solution.

Industry Part Number

CLC406A

NS Part Numbers

CLC406AJ-QML

Prime Die

UB1373C

Controlling Document

5962-9200401MPA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 160MHz small signal bandwidth
- 50mW power (±5V supplies)
- 0.02%/0.02degrees differential gain/phase
- 12ns settling to 0.05%
- 1500V/us slew rate
- 2.2ns rise and fall time (2Vpp)
- 70mA output current

Applications

- Video distribution amp
- HDTV amplifier
- Flash A/D driver
- D/A transimpedance buffer
- Pulse amplifier
- Photodiode amp
- LAN amplifier

(Absolute Maximum Ratings)

Supply voltage (Vcc) (Note 1)		±7 V dc
Output current (Io)		±70 mA
Common mode input voltage (Vcm)		±Vcc
Differential input voltage		+10 V dc
Maximum Power Dissipation (Pd) (Note 2)		1.2W
Lead Temperature (soldering, 10 seconds)		+300C
Junction temperature (Tj)		+175C
Storage temperature range		-65C to +150C
Thermal Resistance		
Junction -to-ambient	(ThetaJA)	
Ceramic DIP	(Still Air)	TBD
	(500 LFPM)	TBD
Junction -to-case	(ThetaJC)	
Ceramic DIP		TBD
Package Weight (typical)		
Ceramic DIP		TBD
ESD Tolerance		
ESD Rating (Note 3)		2000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) / ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100 pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply voltage (Vcc)	±5 V dc
Gain Range	±1 to ±10
Ambient Operating Temperature Range (Ta)	-55C to +125C

Electrical Characteristics

AC/DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vcc = ±5 V dc, Av = +6, Rf (feedback resistor) = 500 Ohms, Rg (gain resistor) = 100 Ohms, -55C ≤ Ta ≤ +125C (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ibn	Input bias current, noninverting				-12	12	uA	1, 2
					-24	24	uA	3
DIBN	Input bias current, average temperature coefficient, noninverting		1		-50	50	nA/C	2
			1		-125	125	nA/C	3
Ibi	Input bias current, inverting				-15	15	uA	1
					-20	20	uA	2
					-23	23	uA	3
DIBI	Input bias currrent, average temperature coefficient, inverting		1		-50	50	nA/C	2
			1		-100	100	nA/C	3
Vio	Input offset voltage				-6	6	mV	1
					-12	12	mV	2
					-10	10	mV	3
DVIO	Input offset voltage, average temperature coefficient		1		-60	60	uV/C	2, 3
Icc	Supply current no load					6.0	mA	1, 2
						6.4	mA	3
PSRR	Power supply rejection ratio	-Vcc = -4.5 V to -5.0 V, +Vcc = +4.5 V to +5.0 V	2		46		dB	1, 3
			2		44		dB	2
+Io	Output current		1		45		mA	1, 2
			1		25		mA	3
-Io	Output current		1			-45	mA	1, 2
			1			-25	mA	3
+Vo	Output voltage range				2.7		V	1, 2
					2.0		V	3
-Vo	Output voltage range					-2.7	V	1, 2
						-2.5	V	3

Electrical Characteristics

AC/DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vcc = ±5 V dc, Av = +6, Rf (feedback resistor) = 500 Ohms, Rg (gain resistor) = 100 Ohms, -55C ≤ Ta ≤ +125C (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Rin	Noninverting input resistance		1		500		k Ohms	1, 2
			1		300		k Ohms	3
CMRR	Common mode rejection ratio	Vcm = ±1.0 V	1		45		dB	4, 6
			1		43		dB	5
SSBW	Small signal bandwidth	-3 dB bandwidth, Vout < 2 Vpp .			110		MHz	4
			2		90		MHz	5
			2		110		MHz	6
LSBW	Large signal bandwidth	-3 dB bandwidth, Vout < 5 Vpp .	1		95		MHz	4, 6
			1		80		MHz	5
GFPL	Gain flatness peaking	0.1 MHz to 25 MHz , Vout < 2 Vpp				0.2	dB	4
			2			0.2	dB	5, 6
GFPH	Gain flatness peaking	> 25MHz, Vout < 2 Vpp				0.5	dB	4
			2			0.5	dB	5, 6
GFR	Gain flatness rolloff	0.1 MHz to 50 MHz, Vout < 2 Vpp				1	dB	4
			2			1.3	dB	5
			2			1	dB	6
LPD	Linear phase deviation	0.1 MHz to 75 MHz	1			0.8	Deg	4, 6
			1			1.2	Deg	5
DG	Differential gain	Rl = 150 Ohms, 3.58 MHz, 4.43 MHz, Av = +2	1			0.04	%	4, 5, 6
DP1	Differential phase	Rl = 150 Ohms, 3.58 MHz, Av = +2	1			0.04	Deg	4, 6
			1			0.08	Deg	5
DP2	Differential phase	Rl = 150 Ohms, 4.43 MHz, Av = +2	1			0.05	Deg	4, 6
			1			0.10	Deg	5
HD2	2nd harmonic distortion	2 Vpp at 20 MHz				-42	dBc	4
			2			-38	dBc	5
			2			-42	dBc	6
HD2L	2nd harmonic distortion	2 Vpp at 10 MHz, Rl = 1 kOhms	1			-62	dBc	4, 6
			1			-60	dBc	5

Electrical Characteristics

AC/DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vcc = ±5 V dc, Av = +6, Rf (feedback resistor) = 500 Ohms, Rg (gain resistor) = 100 Ohms, -55C ≤ Ta ≤ +125C (note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
HD3	3rd harmonic distortion	2 Vpp at 20 MHz				-46	dBc	4
			2			-42	dBc	5
			2			-46	dBc	6
HD3L	3rd harmonic distortion	2 Vpp at 10 MHz, Rl = 1 kOhms	1			-70	dBc	4, 6
			1			-65	dBc	5
Trs	Rise and fall time	2 V step, Cl < 10 pf, measured between 10% and 90% points	1			3.0	ns	9, 11
			1			3.9	ns	10
Trl	Rise and fall time	4 V step, Cl < 10 pF, measured between 10% and 90% points	1			3.6	ns	9, 11
			1			5.0	ns	10
Ts	Settling time	Cl < 10 pF, 2 V step at 0.05% of the final value	1			18	ns	9, 11
			1			20	ns	10
OS	Overshoot	2 V step, Cl < 10 pF	1			15	%	9, 10, 11
SR	Slew Rate	Vout = 4 V step, measured at ±1 V, C1 < 10 pF	1		1200		V/us	4, 6
			1		1000		V/us	5
VN	Equivalent input noise, noninverting voltage	> 1 MHz	1			3.4	nV/Sq RtHz	4, 6
			1			3.8	nV/Sq RtHz	5
ICN	Equivalent input noise, inverting current	> 1 MHz	1			13.9	pA/Sq RtHz	4, 6
			1			15.5	pA/Sq RtHz	5
NCN	Equivalent input noise, noninverting current	> 1 MHz	1			2.6	pA/Sq RtHz	4, 6
			1			3.0	pA/Sq RtHz	5
SNF	Equivalent input noise, total noise floor	> 1 MHz	1			-156	dBm (1Hz)	4, 6
			1			-155	dBm (1Hz)	5
INV	Equivalent input noise, total integrated noise	1 MHz to 100 MHz	1			38	uV	4, 6
			1			42	uV	5

Note 1: Guaranteed, if not tested.
Note 2: This parameter is group A sample tested only and is excluded from final electrical testing, but is guaranteed to the limits specified.

(Continued)

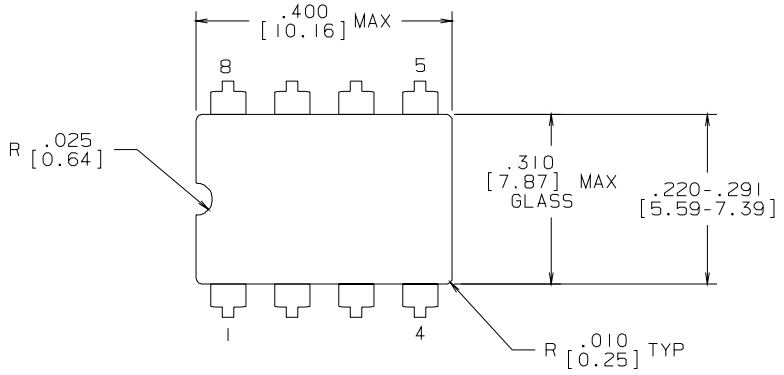
Note 3: The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

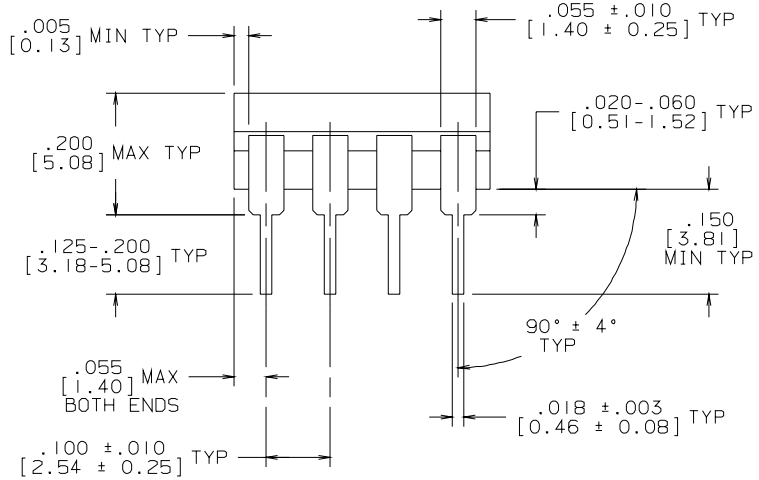
Graphics and Diagrams

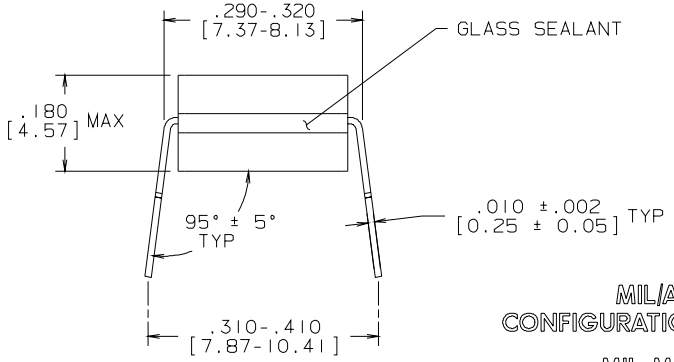
GRAPHICS#	DESCRIPTION
07081HRA3	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000418A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
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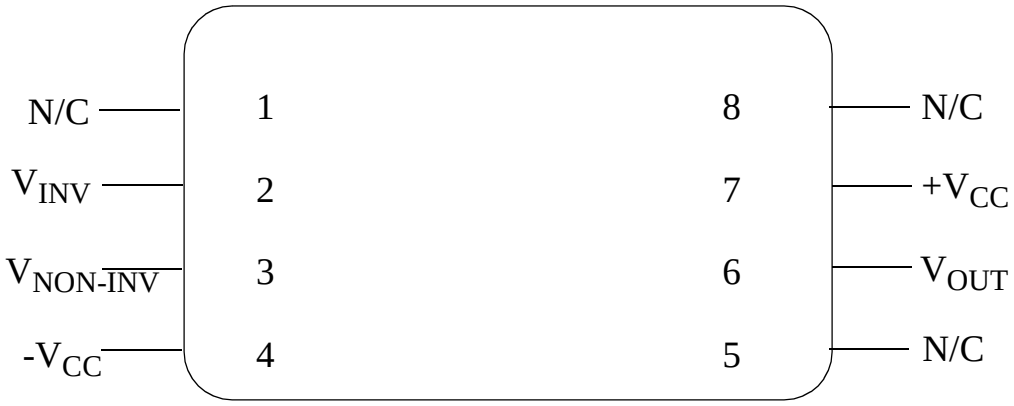
CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC406J

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000418A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003524	09/08/99	Rose Malone	Initial MDS Release