National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC409A-X REV 0A0

Original Creation Date: 08/05/98
Last Update Date: 02/24/99
Last Major Revision Date: 11/12/98

VERY WIDEBAND, LOW DISTORTION MONOLITHIC OP AMP

General Description

The CLC409 is a very wideband, DC coupled monolithic operational amplifier designed specifically for wide dynamic range systems requiring exceptional signal fidelity. Benefiting from Comlinear's current feedback architecture, the CLC409 offers a gain range of ±1 to ±10 while providing stable, oscillation free operation without external compensation, even at unity gain.

With its 350MHz small signal bandwidth (Vout = 2Vpp), 10-bit distortion levels through 20MHz (Rl = 100Ohms), 8-bit distortion levels through 60Mhz, 2.2nV/SqRtHz input referred noise and 13.5mA supply current, the CLC409 is the ideal driver or buffer for high speed flash A/D and D/A converters.

Wide dynamic range systems such as radar and communication receivers requiring a wideband amplifier offering exceptional signal purity will find the CLC409's low input referred noise and low harmonic and intermodulation distortion make it an attractive high speed solution.

Industry Part Number

CLC409A

NS Part Numbers

CLC409AE-QML**
CLC409AJ-QML*

Prime Die

UB1927B

Controlling Document

5962-9203401MPA*, M2A**

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 350MHz small signal bandwidth
- -65/-72dBc 2nd/3rd harmonics (20MHz)
- Low Noise
- 8ns settling to 0.1%
- 1200V/us slew rate
- 13.5mA supply current (±5V)
- 70mA output current

Applications

- Flash A/D driver
- D/A transimpedance buffer
- Wide dynamic range IF amp
- Radar/communication receivers
- DDS post-amps
- Wideband inverting summer
- Line driver

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (Vcc)	±7V dc
Common Mode Input Voltage (Vcm)	±Vcc
Differential Input Voltage	+10V dc
Output Current (Io)	±70mA
Power Dissipation (Pd) (Note 2)	1.2W
Junction Temperature (Tj)	+175 C
Lead Temperature (soldering, 10 seconds)	+300 C
Storage Temperature Range	-65 C to +125 C
Thermal Resistance	
ThetaJA (Junction to Ambient)	
CERAMIC DIP (Still Air)	132 C/W
(500 LFPM)	77 C/W
LCC (Still Air)	97 C/W
(500 LFPM)	67 C/W
ThetaJC (Junction to Case)	
CERAMIC DIP	26 C/W
LCC	27 C/W
Package Weight (Typical)	
CERAMIC DIP	1070 mg
LCC	465 mg
ESD Tolerance (Note 3)	
ESD Rating	500 V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance, and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 1.5K Ohms in series with 100pF.

Recommended Operating Conditions

Supply Voltage (Vcc)	±5V dc
Gain Range	±1 to ±10
Ambient Operating Temperature Range (Ta)	-55 C to +125 C

Electrical Characteristics

AC/DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vcc = ±5V dc, Av = +2, feedback resistor (Rf) = 250 Ohms, gain resistor (Rg) = 250
AC: Ohms -55 C ≤ Ta ≤ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ibn	Input Bias Current, Noninverting				-22	+22	uA	1, 2
					-44	+44	uA	3
DIbn	Input Bias Current, Average Temperature Coefficient, Noninverting		1		-125	+125	nA/C	2
			1		-275	+275	nA/C	3
Ibi	Input Bias Current, Inverting				-20	+20	uA	1
					-30	+30	uA	2
					-36	+36	uA	3
DIbi	Input Bias Current, Average Temperature Coefficient, Inverting		1		-100	+100	nA/C	2
			1		-200	+200	nA/C	3
Vio	Input Offset Voltage				-4.5	+4.5	mV	1
					-9.5	+9.5	mV	2
					-8.5	+8.5	mV	3
DVio	Input Offset Voltage, Average Temperature Coefficient		1		-50	+50	uV/C	2
			1		-50	+50	uV/C	3
Icc	Supply Current, no load					14.2	mA	1, 2, 3
PSRR	Power Supply Rejection Ratio	-Vcc = -4.5V to -5.0V, +Vcc = +4.5V to +5.0V			45		dB	1, 2, 3
+Io	Output Current		1		+50		mA	1, 2
			1		+36		mA	3
-Io	Output Current		1			-50	mA	1, 2
			1			-36	mA	3
+Vo	Output Voltage Range		1		+3.2		V	1, 2
			1		+3.0		V	3
-Vo	Output Voltage Range		1			-3.2	V	1, 2
			1			-3.0	V	3

Electrical Characteristics

AC/DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vcc = ±5V dc, Av = +2, feedback resistor (Rf) = 250 Ohms, gain resistor (Rg) = 250
AC: Ohms -55 C ≤ Ta ≤ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Rin	Noninverting Input Resistance		1		500		KOhms	1
			1		1000		KOhms	2
			1		250		KOhms	3
Cin	Noninverting Input Capacitance		1			2	pF	4, 5, 6
Ro	Output Impedance		1			0.2	Ohms	1, 2
			1			0.3	Ohms	3
CMRR	Common Mode Rejection Ratio	Vcm = ±1.0V	1		45		dB	4, 5, 6
SSBW	Small Signal Bandwidth	-3dB bandwidth, Vout < 2Vpp	1		250		MHz	4, 6
			1		200		MHz	5
LSBW	Large Signal Bandwidth	-3dB bandwidth, Vout < 5Vpp	1		90		MHz	4, 6
			1		80		MHz	5
GFPL	Gain Flatness Peaking	0.1MHz to 75MHz, Vout < 0.5Vpp				0.4	dB	4
			2			0.4	dB	5, 6
GFPH	Gain Flatness Peaking	> 75MHz, Vout < 0.5Vpp				0.8	dB	4
			2			0.8	dB	5, 6
GFR1	Gain Flatness Rolloff	0.1MHz to 125MHz				1.0	dB	4
			2			1.0	dB	5, 6
GFR2	Gain Flatness Rolloff	At 200MHz				2.2	dB	4
			2			3.0	dB	5
			2			2.0	dB	6
LPD	Linear Phase Deviation	.01MHz to 100MHz	1			0.8	Degree	4, 6
			1			1.0	Degree	5
DG	Differential Gain	Rl = 150 Ohms, 3.58MHz, 4.43MHz	1			.06	%	4, 5
			1			.07	%	6
DP	Differential Phase	Rl = 150 Ohms, 3.58MHz, 4.43MHz	1			.02	Degree	4, 5, 6
HD2	2nd Harmonic Distortion	2Vpp at 20MHz				-52	dBc	4
			2			-52	dBc	5, 6

Electrical Characteristics

AC/DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vcc = ±5V dc, Av = +2, feedback resistor (Rf) = 250 Ohms, gain resistor (Rg) = 250
AC: Ohms -55 C ≤ Ta ≤ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
HD2L	2nd Harmonic Distortion	2Vpp at 5MHz	1			-81	dBc	4, 5
			1			-78	dBc	6
HD2H	2nd Harmonic Distortion	2Vpp at 60MHz	1			-44	dBc	4, 5
			1			-41	dBc	6
HD3	3rd Harmonic Distortion	2Vpp at 20MHz				-65	dBc	4
			2			-65	dBc	5, 6
HD3L	3rd Harmonic Distortion	2Vpp at 5MHz	1			-76	dBc	4, 5, 6
HD3H	3rd Harmonic Distortion	2Vpp at 60MHz	1			-52	dBc	4, 5, 6
Trs	Rise and Fall Time	2V step, Cl < 10pF, measured between 10% and 90% points	1			1.6	ns	9, 10, 11
Trl	Rise and Fall Time	5V step, Cl < 10pF, measured between 10% and 90% points	1			4.2	ns	9, 11
			1			4.6	ns	10
Ts	Settling Time	Cl < 10pF, 2V step at 0.1% of the final value	1			12	ns	9, 10, 11
OS	Overshoot	2V step, Cl < 10pF	1			18	%	9, 10
			1			15	%	11
SR	Slew Rate	Vout = 4V step, Cl < 10pF, measured at ±1V	1		1000		V/us	4, 5, 6
VN	Equivalent Input Noise, Noninverting Voltage	> 1MHz	1			2.8	nV/Sq Rt	4, 6
			1			3.1	nV/Sq Rt	5
ICN	Equivalent Input Noise, Inverting Current	> 1MHz	1			18	pA/Sq Rt	4, 6
			1			20	pA/Sq Rt	5
NCN	Equivalent Input Noise, Noninverting Current	> 1MHz	1			4.0	pA/Sq Rt	4, 6
			1			4.5	pA/Sq Rt	5
SNF	Equivalent Input Noise, Total Noise Floor	> 1MHz	1			-155	dBm 1Hz	4, 6
			1			-154	dBm 1Hz	5

Electrical Characteristics

AC/DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vcc = ±5V dc, Av = +2, feedback resistor (Rf) = 250 Ohms, gain resistor (Rg) = 250
AC: Ohms -55 C ≤ Ta ≤ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
INV	Equivalent Input Noise, Total Integrated Noise	1MHz to 150MHz	1			47	uV	4, 6
			1			52	uV	5

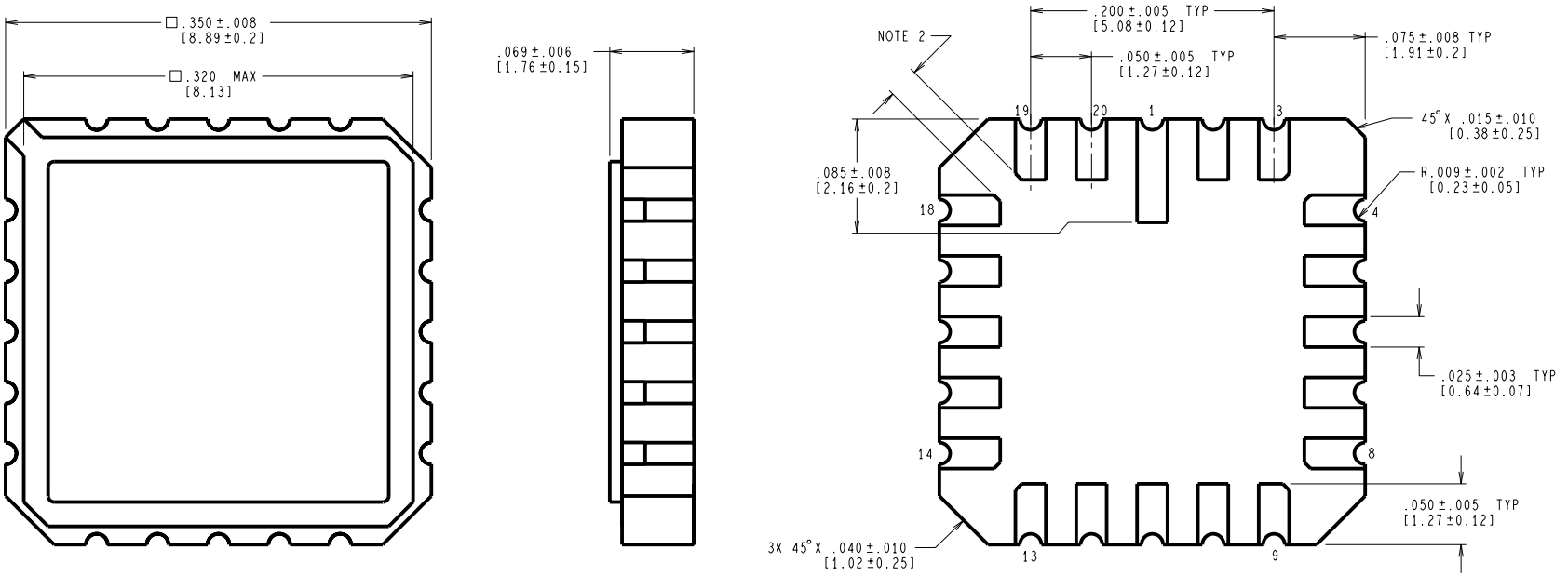
Note 1: Guaranteed, if not tested.
Note 2: This parameter is group A sample tested only and is excluded from final electrical testing, but is guaranteed to the limits specified.
Note 3: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as convential current flow out of a device terminal.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
07077HRA2	CERDIP (J), 8 LEAD (B/I CKT)
07086HRA2	LCC (E), TYPE C, 20 TERMINAL (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000406A	CERDIP (J), 8 LEAD (PINOUT)
P000446A	LCC (E), TYPE C, 20 TERMINAL (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

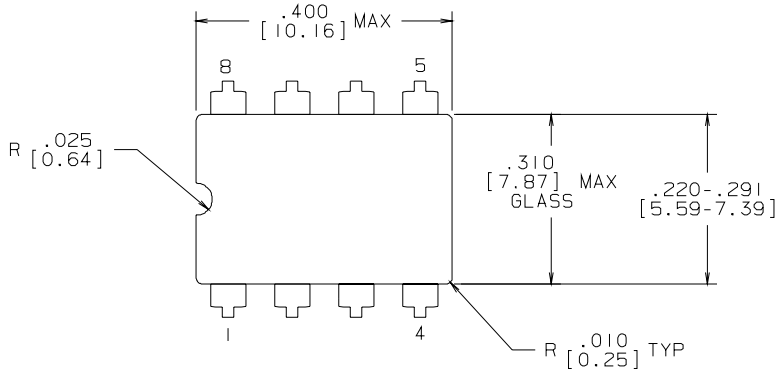
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

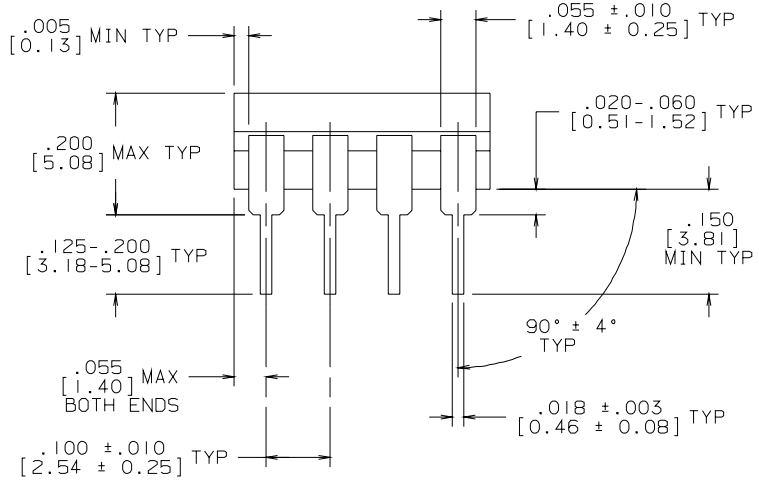
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

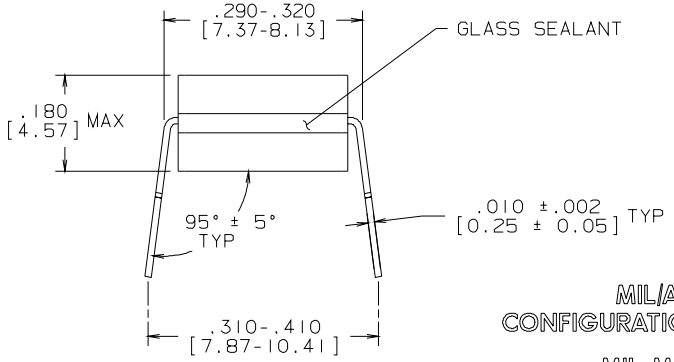
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

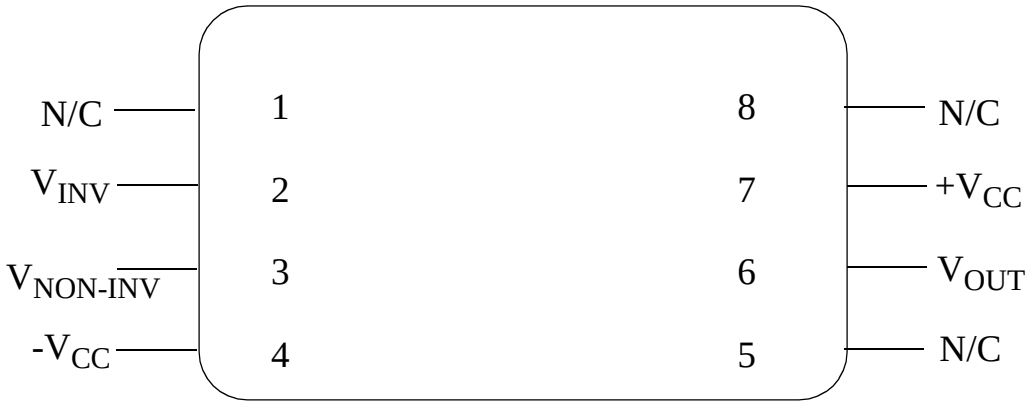
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC409J

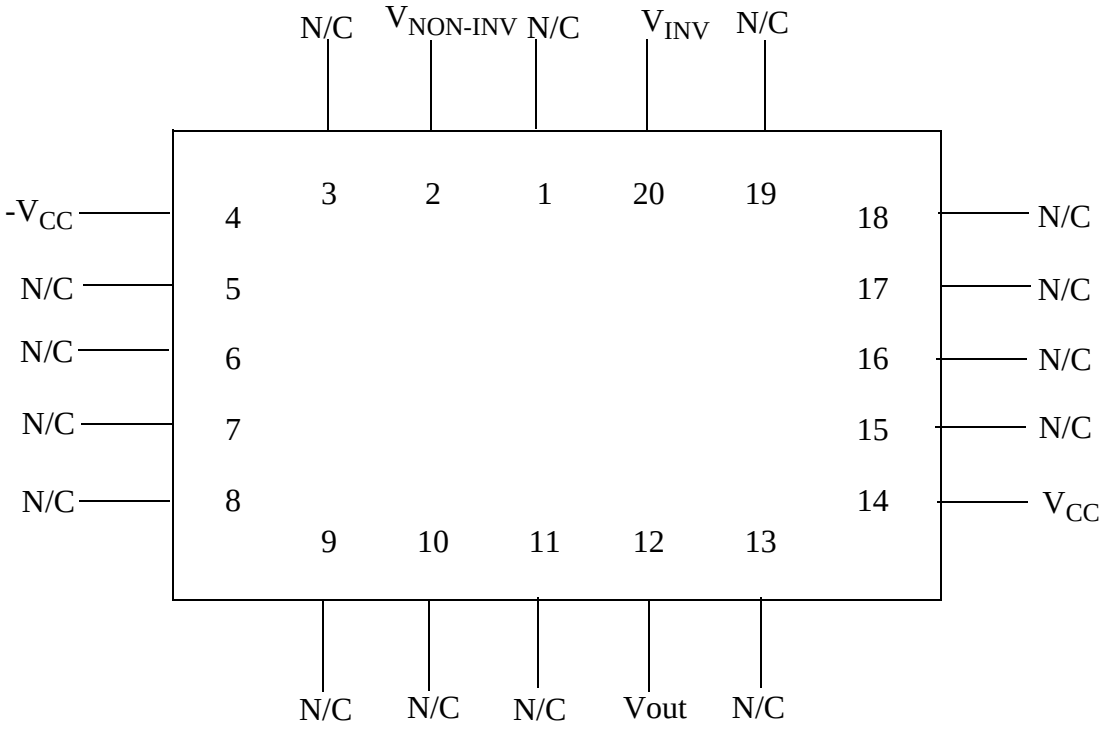
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000406A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



CLC409E
20 - LEAD LCC
CONNECTION DIAGRAM
TOP VIEW
P000446A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003257	02/24/99	Shaw Mead	Initial MDS Release