National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC412A-X REV 2A0

Original Creation Date: 02/02/99
Last Update Date: 06/09/03
Last Major Revision Date: 05/07/03

Dual Wideband Video Op Amp

General Description

The Comlinear CLC412 combines a high-speed complementary bipolar process with Comlinear's current-feedback topology to produce a very high-speed dual op amp. The CLC412 provides a 250MHz small-signal bandwidth at a gain of +2V/V and a 1300V/us slew rate while consuming only 50mW per amplifier from ±5V supplies.

The CLC412 offers exceptional video performance with its 0.02% and 0.02 degrees differential gain and phase errors for NTSC and PAL video signals while driving one back terminated 75ohms load. The CLC412 also offers a flat gain response of 0.1dB to 30MHz and very low channel-to-channel crosstalk of -76dB at 10MHz. Additionally, each amplifier can deliver a 70mA continuous output current. This level of performance makes the CLC412 an ideal dual op amp for high-density broadcast-quality video systems.

The CLC412's two very well-matched amplifiers support a number of applications such as differential line drivers and receivers. In addition, the CLC412 is well suited for Sallen Key active filters in applications such as anti-aliasing filters for high-speed A/D converters. Its low power requirement, low noise and low distortion also allow the CLC412 to serve portable RF applications such as IQ-channels.

Industry Part Number

CLC412A

NS Part Numbers

CLC412AE-QML
CLC412AJ-MLS
CLC412AJ-QML

Prime Die

UB1709A

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Wide bandwidth: 330MHz (Av=+1V/V)
  250MHz (Av=+2V/V)
- 0.1dB gain flatness to 30MHz
- Low power: 5mA/channel
- Very low diff. gain, phase: 0.02%, 0.02degrees
- -76dB channel-to-channel crosstalk (10MHz)
- Fast slew rate: 1300V/ms
- Unity-gain stable

CONTROLLING DOCUMENTS:

CLC412AE-QML	5962-9471901M2A
CLC412AJ-QML	5962-9471901MPA

Applications

- HDTV, NTSC & PAL video systems
- Video switching and distribution
- IQ amplifiers
- Wideband active filters
- Cable drivers
- DC coupled single-to-differential conversions

(Absolute Maximum Ratings)
(Note 1)

Supply voltage(Vcc)		±7 V dc
Output current (Iout)		96mA
Common mode input voltage (Vcm)		±Vcc
Power dissipation (Pd) (Note 2)		201mW
Lead temperature (soldering, 10 seconds)		+300C
Junction temperature (Tj)		+175C
Storage temperature range		-65C ≤ Ta ≤ +150C
Thermal Resistance		
Junction-to-ambient (ThetaJA)		
Ceramic DIP	(Still Air)	TBD
	(500 LFPM)	TBD
LCC	(Still Air)	TBD
	(500 LFPM)	TBD
Junction-to-case (ThetaJC)		
Ceramic DIP		TBD
LCC		TBD
Package Weight (typical)		
Ceramic DIP		TBD
LCC		TBD
ESD Tolerance (Note 3)		1000V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) /ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5k Ohms.

Recommended Operating Conditions

Supply Voltage (Vcc)	±5 V dc
Gain Range (Av)	±1 V/V to ±10 V/V
Ambient operating temperature range (Ta)	-55C ≤ Ta ≤ +125C

Electrical Characteristics

DC Paramaters: Static and DC tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100Ohms, Vcc = ±5 V dc, Av= +2, Rf=634Ohms, Rg=634Ohms,-55C ≤ Ta ≤ + 125C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ibn	Input bias current, noninverting				-12	12	uA	1, 2
					-28	28	uA	3
Ibn	Input bias current, inverting				-15	15	uA	1
					-20	20	uA	2
					-34	34	uA	3
Vio	Input offset voltage				-6	6	mV	1
					-12	12	mV	2
					-10	10	mV	3
Tc(+Ibn)	Average input bias current drift	Ta = +125C, -55C	1		-90	90	nA/C	2
			1		-187	187	nA/C	3
Tc(-Ibn)	Average input bias current drift	Ta = +125C, -55C	1		-80	80	nA/C	2
			1		-125	125	nA/C	3
Tc(Vio)	Average input offset voltage drift	Ta = +125C, -55C	1		-60	60	uV/C	2, 3
Icc	Supply current	Rl = infinity				12.8	mA	1, 2
						13.6	mA	3
PSRR	Power supply rejection ration	+Vs = +4.5 V to +5.0 V, -Vs = -4.5 V to -5.0 V			46		dB	1
					44		dB	2, 3
CMRR	Common mode rejection ration	Vcm = ±1 V	1		45		dB	4
			1		43		dB	5, 6

Electrical Characteristics

AC Parameters: Frequeuncy domain tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100Ohms, Vcc = ±5 V dc, Av= +2, Rf=634Ohms, Rg=634Ohms,-55C ≤ Ta ≤ + 125C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SSBW	Small signal bandwith	-3dB bandwidth, Vout < 0.5 Vpp			175		MHz	4
			2		135		MHz	5
			2		150		MHz	6
LSBW	Large signal bandwith	-3dB bandwidth, Vout < 4.0 Vpp	1		80		MHz	4, 6
			1		65		MHz	5
GFP	Gain flatness peaking high	0.1MHz to 30 MHz, Vout ≤ 0.5Vpp				0.1	dB	4
			2			0.2	dB	5
			2			0.1	dB	6
GFR	Gain flatness rolloff	0.1MHz to 30 MHz, Vout ≤ 0.5Vpp				0.3	dB	4
			2			0.3	dB	5
			2			0.4	dB	6
LPD	Linear phase deviation	DC to 75 MHz, Vout ≤ 0.5Vpp	1			1.0	Deg	4, 5
			1			1.3	Deg	6
DG	Differential gain	4.43 MHz, Rl = 150 Ohms	1		0.04		%	4, 6
			1		0.08		%	5
DP	Differential phase	4.43 MHz, Rl = 150 Ohms	1		0.04		Deg	4, 6
			1		0.08		Deg	5

AC Paramaters: Distortion and noise tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100Ohms, Vcc = ±5 V dc, Av= +2, Rf=634Ohms, Rg=634Ohms,-55C ≤ Ta ≤ + 125C (Note 3)

HD2	Second harmonic distortion	2 Vpp at 20 MHz				-42	dBc	4
			2			-38	dBc	5
			2			-42	dBc	6
HD3	Third harmonic distortion	2 Vpp at 20 MHz				-46	dBc	4
			2			-42	dBc	5
			2			-46	dBc	6
VEN	Equivalent noise input positive voltage	> 1 MHz	1			3.4	nV/Sq RtHz	4, 6
			1			3.8	nV/Sq RtHz	5

Electrical Characteristics

AC Paramaters: Distortion and noise tests - Continued

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100Ohms, Vcc = ±5 V dc, Av= +2, Rf=634Ohms, Rg=634Ohms,-55C ≤ Ta ≤ + 125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
ICN	Equivalent input inverting current noise	> 1 MHz	1			13.9	pA/Sq RtHz	4, 6
			1			15.5	pA/Sq RtHz	5
NICN	Equivalent input non-inverting current noise	> 1 MHz	1			2.6	pA/Sq RtHz	4, 6
			1			3.0	pA/Sq RtHz	5
SNF	Noise floor	> 1 MHz	1		-156		dBm (1 Hz)	4, 6
			1		-155		dBm (1 Hz)	5
XTLK	Crosstalk (input refered)	At 10 MHz	1		-64		dB	4, 5, 6

AC Paramaters: Timing tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100Ohms, Vcc = ±5 V dc, Av= +2, Rf=634Ohms, Rg=634Ohms,-55C ≤ Ta ≤ + 125C (Note 3)

tRS	Rise and fall time	0.5 V step	1		2.0		ns	9
			1		2.6		ns	10
			1		2.3		ns	11
tRL	Rise and fall time	4 V step	1		4.4		ns	9, 11
			1		4.8		ns	10
SR	Slew Rate	Measured ±1 V with ±2 V step, Av = 2	1			1000	V/us	4, 6
			1			800	V/us	5
tS	Settling time	2 V step at 0.05% of the fixed value	1			18	ns	9, 11
			1			20	ns	10
OS	Overshoot	0.5 V step	1			15	%	9, 10, 11

Electrical Characteristics

DC Paramaters: Performance tests

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100Ohms, Vcc = ±5 V dc, Av= +2, Rf=634Ohms, Rg=634Ohms,-55C ≤ Ta ≤ + 125C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Rin	Input resistance (positive)		1		500		kOhms	4, 5
			1		300		kOhms	6
Cin	Input capacitance (positive)		1		2.0		pF	4, 5, 6
Vout	Output voltage range	Rl = infinity	1		-3.0	3.7	V	1, 2
			1		-2.9	3.6	V	3
		Rl = 100 Ohms	1		-2.7	2.7	V	1, 2
			1		-2.5	2.0	V	3
Rout	Output resistance	Closed loop	1		0.3		Ohms	4
			1		0.2		Ohms	5
			1		0.6		Ohms	6
CMIR	Common mode input voltage range		1		-2.0	2.0	V	1, 2
			1		-1.4	1.4	V	3
Iout	Output current		1		45		mA	1, 2
			1		25		mA	3

DC Paramaters: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: "Deltas not required on B-Level product. Deltas required for S-Level product at Group B5 ONLY, or as specified on the Internal Processing Instructions (IPI), (Note 3).

Ibn	Input bias current, noninverting		1		-1.2	+1.2	uA	1
Ibi	Input bias current, inverting		1		-1.5	+1.5	uA	1
Vio	Input offset voltage		1		-0.3	+0.3	mV	1
Icc	Supply Current	Rl = Infinity	1		-0.64	+0.64	mA	1

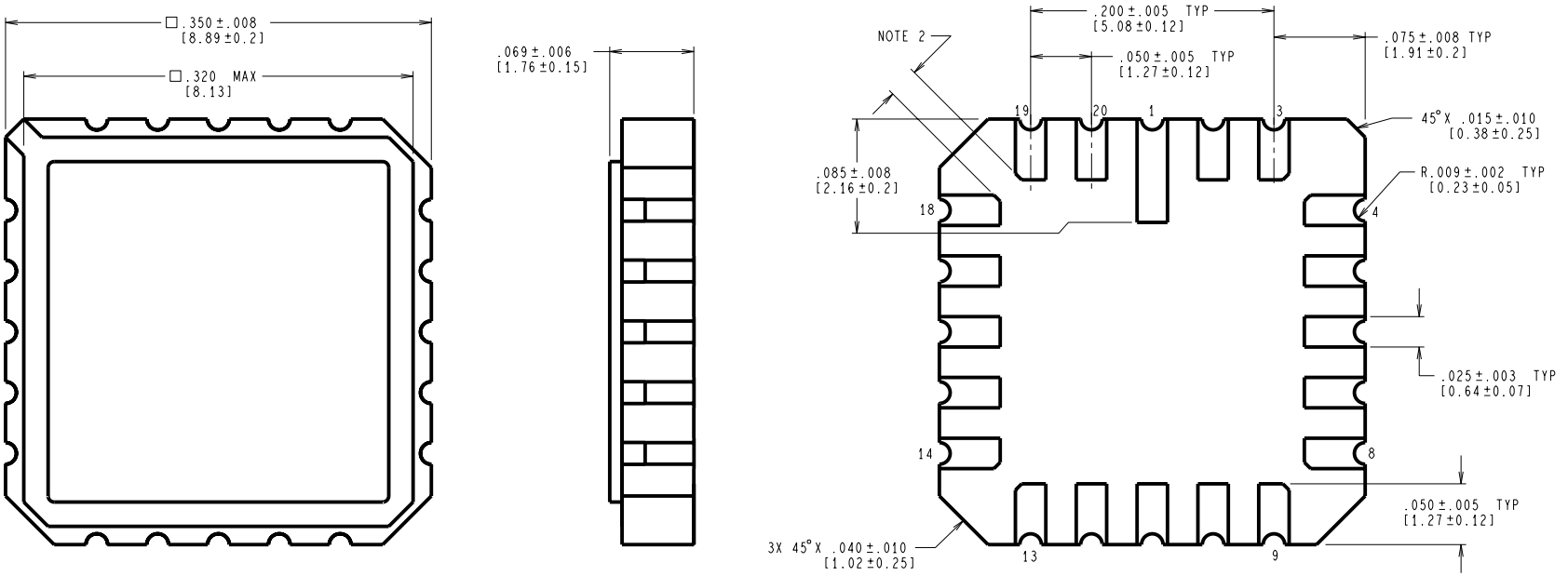
Note 1: If not tested, shall be guaranteed to the limits specified in table 1 herein.
Note 2: Group A testing only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
07082HRA2	CERDIP (J), 8 LEAD (B/I CKT)
07088HRA2	LCC (E), TYPE C, 20 TERMINAL (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000415A	CERDIP (J), 8 LEAD (PINOUT)
P000450A	LCC (E), TYPE C, 20 TERMINAL (PIN OUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

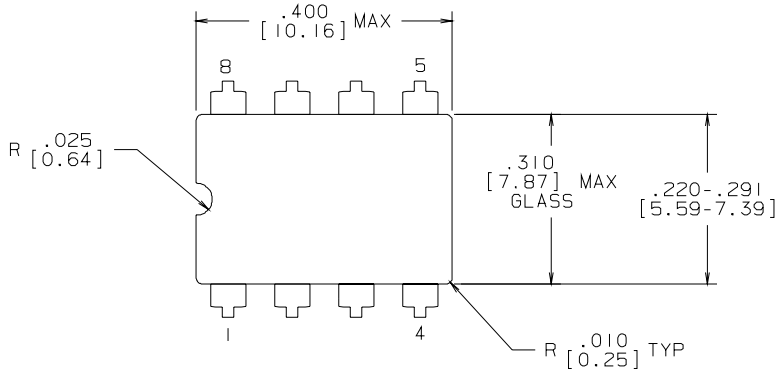
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

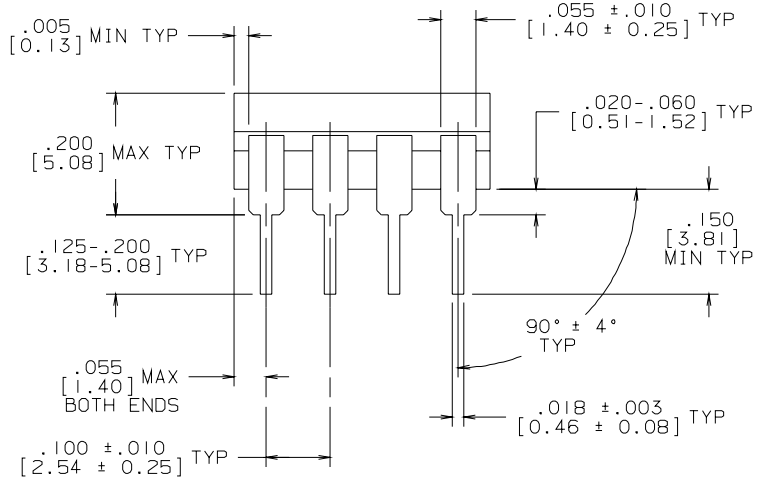
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

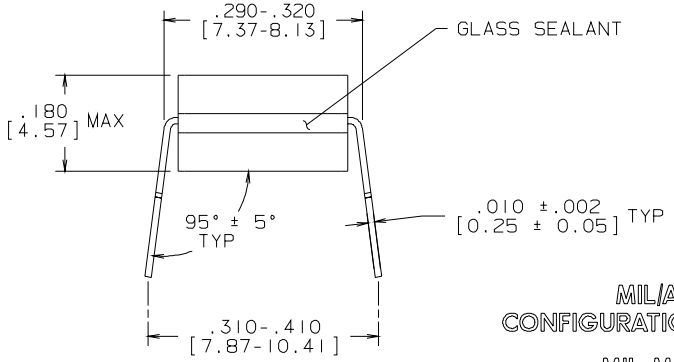
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

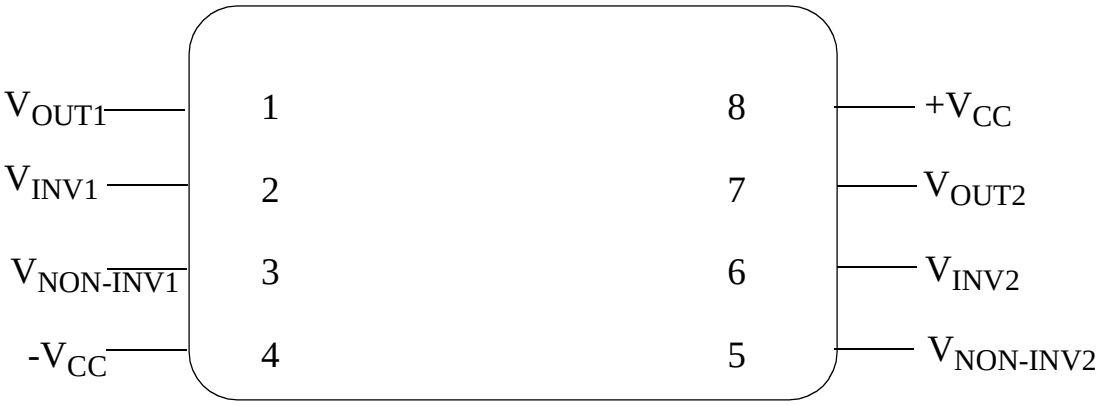
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC412J

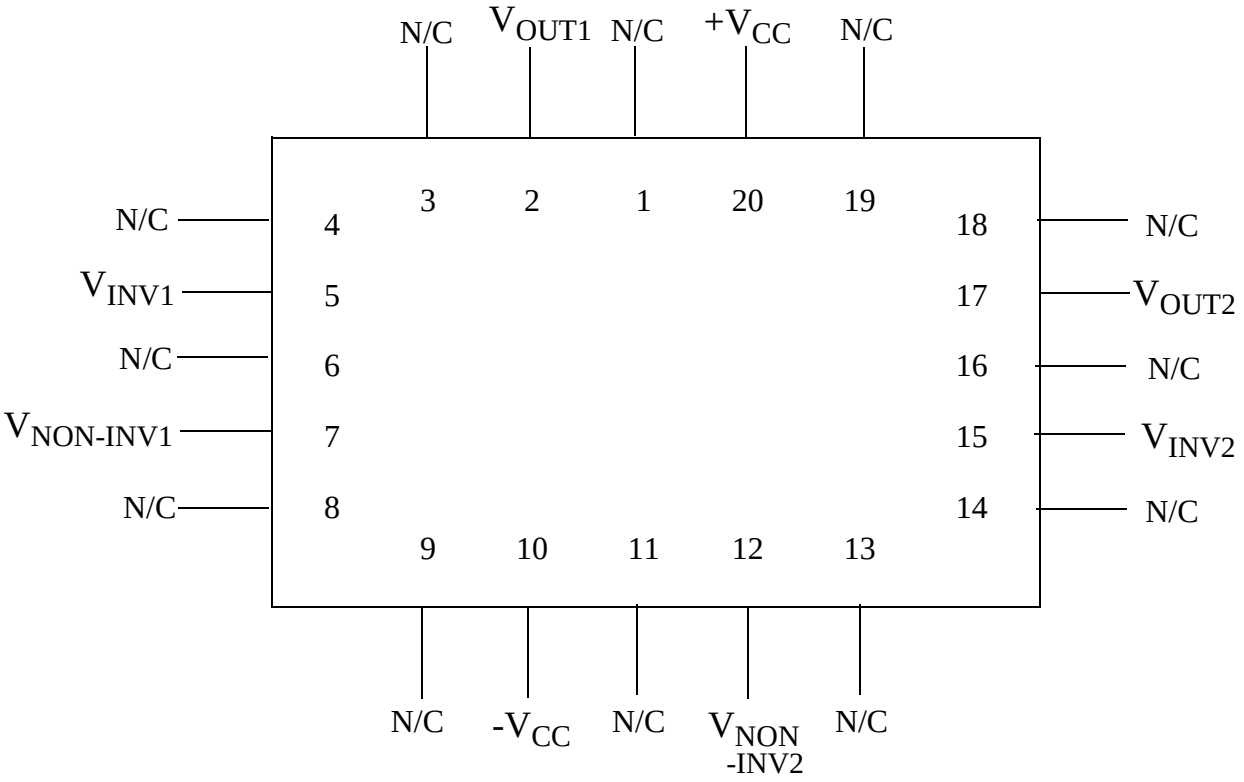
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000415A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



CLC412AE-QML
20 - LEAD LCC
CONNECTION DIAGRAM
TOP VIEW
P000450A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003253	02/11/03	Shaw Mead	Initial MDS Release
1A0	M0004108	06/09/03	Rose Malone	Update MDS: MNCLC412A-X, Rev. 0A0 to MNCLC412A-X, Rev. 1A0. Moved reference to SMD numbers to Features Section. Added Drift Table to Electrical Section.
2A0	M0004157	06/09/03	Rose Malone	Update MDS: MNCLC412A-X, Rev. 1A0 to MNCLC412A-X, Rev. 2A0. Electricals in Drift Values Section have been changed to reflect the customer drawing. Added Note 2 to parameters SSBW, GFP, GFR, HD2 and HD3, Subgroups 5 and 6.