

MNCLC432A-X REV 0A0

Original Creation Date: 01/06/99
Last Update Date: 04/05/99
Last Major Revision Date: 04/01/99

DUAL WIDEBAND MONOLITHIC OP AMP
General Description

The CLC432 is a current-feedback amplifier that provides a wide bandwidth and high slew rate for applications where board density and power are key considerations. This amplifier provides a dc-coupled small signal bandwidth exceeding 92MHz while consuming only 7mA per channel. Operating from $\pm 15V$ supplies, the CLC432's enhanced slew rate circuitry delivers large-signal bandwidths with output voltage swings up to 28Vpp. A wide range of bandwidth-insensitive gains are made possible by virtue of the CLC432's current-feedback topology.

The large common-mode input range and fast settling time (70ns to 0.05%) makes this amplifier well suited for CCD & data telecommunication applications. Many high performance video applications requiring signal gain and/or switching will be satisfied with the CLC432 due to its very low differential gain and phase errors (less than 0.1% and 0.1 degrees; $A_v = +2V/V$ at 4.43MHz into 1500hms load).

Quick 8ns rise and fall times on 10V pulses allow the CLC432 to drive either twisted pair or coaxial transmission lines over long distances.

The CLC432's combination of low input voltage noise, wide common-mode input voltage range and large output voltage swings makes it especially well suited for wide dynamic range signal processing applications.

Industry Part Number

CLC432A

NS Part Numbers

CLC432AJ-QML

Prime Die

LB1792A

Controlling Document

5962-9472502MPA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Wide bandwidth: 92Mhz ($A_v = +1$)
62MHz ($A_v = +2$)
- Fast slew rate: 2000V/us
- Fast disable: 1us to high-Z output
- High channel isolation: 70dB at 10MHz
- Single or dual supplies: $\pm 5V$ to $\pm 16.5V$

Applications

- Video signal multiplexing
- Twisted-pair differential driver
- CCD buffer & level shifting
- Discrete gain-select amplifier
- Transimpedance amplifier

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vs)	±16.5 V dc
Output Current (Iout)	100mA
Common Mode Input Voltage (Vcm)	±Vs
Differential Input Voltage(Vid)	±10 V
Maximum Power Dissipation (Pd) (Note 2)	1.02W
Lead Temperature (Soldering, 10 seconds)	+300 C
Junction Temperature (Tj)	+175 C
Storage Temperature Range	-65 C to +150 C
Thermal Resistance	
Junction -to-ambient (ThetaJA) Ceramic DIP (Still Air)	128 C/W
Junction -to-ambient (ThetaJA) Ceramic DIP (500 LFPM)	67 C/W
Junction -to-case (ThetaJC) Ceramic DIP	23 C/W
Package Weight (Typical) Ceramic DIP	TBD
ESD Tolerance (Note 3)	
ESD Ratings	2000 V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum package power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable package power dissipation at any temperature is $P_{dmax} = (T_{jmax} - T_A) / \Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100 pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vs)	$\pm 15\text{V}$ dc
Gain Range (Av)	± 1 V/V to ± 10 V/V
Ambient Operating Temperature Range (TA)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS: Static and DC Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_s = \pm 15V$ dc, $A_v = +2$, and load resistance (R_L) = 1000hms. Gain Resistance (R_g) and Feedback resistance (R_f) equals 7500hms. $-55\text{ C} \leq T_a \leq +125\text{ C}$ (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Ibn	Input Bias Current, noninverting				-8	+8	uA	1, 2
					-18	+18	uA	3
Ibi	Input Bias Current, inverting				-6	6	uA	1, 2
					-9	9	uA	3
Vio	Input Offset Voltage				-6	6	mV	1, 3
					-9	9	mV	2
Dibn	Average Input Bias Current Drift, noninverting	$T_a = +125\text{ C}, -55\text{ C}$	1		-150	150	nA/C	2, 3
Dibi	Average Input Bias Current Drift, inverting	$T_a = +125\text{ C}, -55\text{ C}$	1		-40	40	nA/C	2, 3
Dvio	Average Input Offset Voltage Drift	$T_a = +125\text{ C}, -55\text{ C}$	1		-50	50	uV/C	2, 3
Icc	Supply Current	No Load				15.8	mA	1, 2
						19.6	mA	3
PSRR	Power Supply Rejection Ratio	$+V_s = +4.0V$ to $+5.0V$, $-V_s = -4.0V$ to $-5.0V$			59		dB	4, 6
					57		dB	5
CMRR	Common Mode Rejection Ratio	$V_{cm} = \pm 1V$	1		58		dB	4
			1		56		dB	5, 6

Electrical Characteristics

AC PARAMETERS: Frequency Domain Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $V_s = \pm 15V$ dc, $A_v = +2$, and load resistance (R_l) = 1000hms. Gain Resistance (R_g) and Feedback resistance (R_f) equals 7500hms. $-55^\circ C \leq T_a \leq +125^\circ C$ (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SSBW	Small Signal Bandwidth	-3 dB bandwidth, $V_{out} < 4.0 V_{pp}$			42		MHz	4
			2		34		MHz	5
			2		42		MHz	6
LSBW	Large Signal Bandwidth	-3 dB bandwidth, $V_{out} < 10 V_{pp}$	1		21		MHz	4, 6
			1		17		MHz	5
GFPH	Gain Flatness Peaking High	0.1 MHz to 100 MHz, $V_{out} \leq 4.0 V_{pp}$				0.5	dB	4
			2			0.9	dB	5, 6
GFR	Gain Flatness Rolloff	0.1 MHz to 20 MHz, $V_{out} \leq 4.0 V_{pp}$				0.8	dB	4
			2			0.8	dB	5, 6
DG	Differential Gain	4.43 MHz	1		0.18		%	4, 6
			1		0.22		%	5
DP	Differential Phase	4.43 MHz	1		0.18		Deg.	4, 6
			1		0.32		Deg.	5
LPD	Linear Phase Deviation	DC to 20MHz, $V_{out} \leq 4.0 V_{pp}$	1		1.8		Deg.	4, 6
			1		2.3		Deg.	5

Electrical Characteristics

AC PARAMETERS: Distortion and Noise Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $V_s = \pm 15V$ dc, $A_v = +2$, and load resistance (R_L) = 1000hms. Gain Resistance (R_g) and Feedback resistance (R_f) equals 7500hms. $-55\text{ C} \leq T_a \leq +125\text{ C}$ (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
HD2	2nd Harmonic Distortion	2 Vpp at 10 MHz				38	dBc	4
			2			33	dBc	5
			2			38	dBc	6
HD3	3rd Harmonic Distortion	2 Vpp at 10 MHz				48	dBc	4
			2			48	dBc	5, 6
VN	Input Noise Voltage	> 1 MHz	1			4.2	nV/Sq RtHz	4, 6
			1			4.7	nV/Sq RtHz	5
-ICN	Inverting Input Noise Current	> 1 MHz	1			16	pA/Sq RtHz	4, 5
			1			18	pA/Sq RtHz	6
+ICN	Noninverting Input Noise Current	> 1 MHz	1			2.5	pA/Sq RtHz	4
			1			2.8	pA/Sq RtHz	5, 6

AC PARAMETERS: Timing Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $V_s = \pm 15V$ dc, $A_v = +2$, and load resistance (R_L) = 1000hms. Gain Resistance (R_g) and Feedback resistance (R_f) equals 7500hms. $-55\text{ C} \leq T_a \leq +125\text{ C}$ (Note 3).

SR	Slew Rate	$V_{out} = \pm 10\text{ V Step}$	1		1500		V/ μ S	9
			1		1400		V/ μ S	10, 11
T_r, T_f	Rise and Fall Time	10 V Step	1			12	nS	9, 11
			1			14	nS	10
T_s	Settling Time	2V step at 0.05% of the fixed value	1			100	nS	9, 11
			1			120	nS	10
OS	Overshoot	2 V Step, 1 ns rise/fall	1			10	%	9, 11
			1			14	%	10

Electrical Characteristics

DC PARAMETERS: Performance Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $V_s = \pm 15V$ dc, $A_v = +2$, and load resistance (R_L) = 1000hms. Gain Resistance (R_g) and Feedback resistance (R_f) equals 7500hms. $-55^\circ C \leq T_a \leq +125^\circ C$ (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
R _{in}	Positive Input Resistance		1		16		MOhms	4, 5
			1		5		MOhms	6
C _{in}	Positive Input Capacitance		1		1		pF	4, 5, 6
V _{out}	Output Voltage Range	No Load	1		-13.6	+13.6	V	1, 2
			1		-13.2	+13.2	V	3
V _{outl}	Output Voltage Range	$R_L = 1000hms$	1		-3.7	+3.7	V	1, 2
			1		-2.7	+2.7	V	3
CMIR	Common Mode Input Voltage Range		1		12		V	1, 2
			1		11.5		V	3
I _{out}	Output Current		1		38		mA	1, 2
			1		28		mA	3

AC PARAMETERS: Switching Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $V_s = \pm 15V$ dc, $A_v = +2$, and load resistance (R_L) = 1000hms. Gain Resistance (R_g) and Feedback resistance (R_f) equals 7500hms. $-55^\circ C \leq T_a \leq +125^\circ C$ (Note 3).

T _{on}	Switching turn on time	$V_{in} = 4 V_{pp}$ at 10 MHz	1			150	uS	9, 10
			1			170	uS	11
T _{off}	Switching turn off time	$V_{in} = 4 V_{pp}$ at 10 MHz	1			1000	uS	9, 11
			1			1400	uS	10
V _{ih}	Disable Logic High Input Voltage	Single ended mode	1			2	V	1, 2, 3
V _{il}	Disable Logic Low Input Voltage	Single ended mode	1		0.8		V	1, 2, 3
I _{din}	Disable Logic Maximum Input Current	DIS = V _{il} to V _{ih}	1			180	uA	1, 2
			1			210	uA	3
V _{min}	Minimum Differential Voltage	DIS = V _{il} to V _{ih}	1			0.4	V	1, 2
			1			0.5	V	3

Electrical Characteristics

AC PARAMETERS: Isolation Tests

(The following conditions apply to all the following parameters, unless otherwise specified.)

AC: $V_s = \pm 15V$ dc, $A_v = +2$, and load resistance (R_l) = 1000hms. Gain Resistance (R_g) and Feedback resistance (R_f) equals 7500hms. $-55\text{ C} \leq T_a \leq +125\text{ C}$ (Note 3).

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
XTLK	Crosstalk, input referred isolation	10 MHz	1		64		dB	4, 5, 6
ISO	Off Isolation	10 MHz	1		53		dB	4, 5, 6

Note 1: If not tested, shall be guaranteed to the limits specified in table I

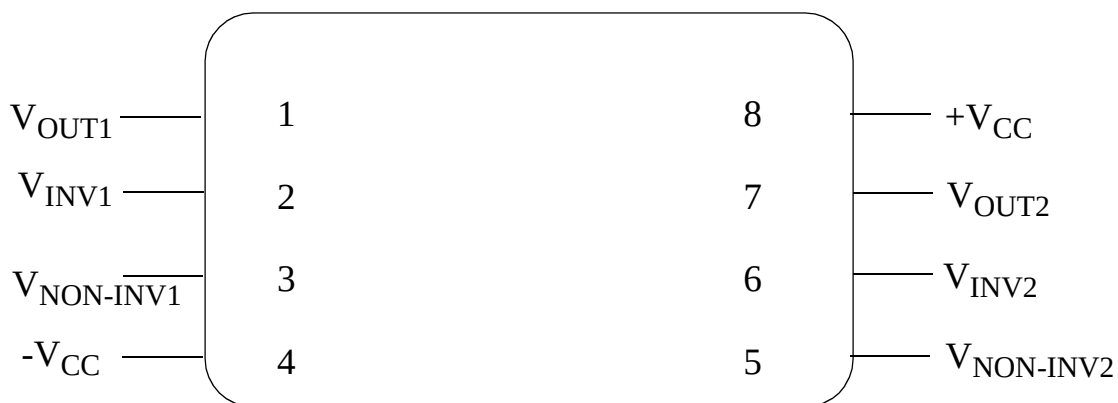
Note 2: Group A testing only.

Note 3: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
07082HRA2	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000405A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.



CLC432J

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000405A

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003352	04/05/99	Shaw Mead	Initial MDS Release