National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM6172AM-X-RH REV 0A0

Original Creation Date: 07/19/01
Last Update Date: 08/13/01
Last Major Revision Date:

DUAL HIGH SPEED, LOW POWER, VOLTAGE FEEDBACK AMPLIFIERS: ALSO AVAILABLE GUARANTEED TO 300k RAD (Si) TESTED TO MIL-STD-883, METHOD 1019.5

General Description

The LM6172 is a dual high speed voltage feedback amplifier. It is unity-gain stable and provides excellent DC and AC performance. With 100 MHz unity-gain bandwidth, 3000V/uS slew rate and 50mA of output current per channel, the LM6172 offers high performance in dual amplifiers; yet it consumes only 2.3 mA of supply current per amplifier.

The LM6172 operates on ±15V power supply for systems requiring large voltage swings, such as ADSL, scanners and ultrasound equipment. It is also specified at ±5V power supply for low voltage applications such as portable video systems.

The LM6172 is built with National's advanced VIP[TM]III (Vertically Integrated PNP) complementary bipolar process.

Industry Part Number

LM6172

Prime Die

LM6172

Controlling Document

SEE FEATURES SECTION

NS Part Numbers

LM6172AMJ-QML
LM6172AMJ-QMLV
LM6172AMJFQML
LM6172AMJFQMLV
LM6172AMWG-QML
LM6172AMWG-QMLV
LM6172AMWGFQML
LM6172AMWGFQMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

(Typical)

- Easy to use Voltage Feedback Topology
- High Slew Rate 3000 V/uS
- Wide Unity-Gain Bandwidth 100 MHz
- Low Supply Current 2.3 mA/Amplifier
- High Output Current 50 mA/Amplifier
- Specified for ±15V and ±5V operation
- CONTROLLING DOCUMENT:

LM6172AMJ-QML	5962-9560401QPA
LM6172AMJ-QMLV	5962-9560401VPA
LM6172AMJFQML	5962F9560401QPA
LM6172AMJFQMLV	5962F9560401VPA
LM6172AMWG-QML	5962-9560401QXA
LM6172AMWG-QMLV	5962-9560401VXA
LM6172AMWGFQML	5962F9560401QXA
LM6172AMWGFQMLV	5962F9560401VXA

Applications

- Scanner I-to-V Converters
- ADSL/HDSL Drivers
- Multimedia Broadcast Systems
- Video Amplifiers
- NTSC, PAL and SECAM Systems
- ADC/DAC Buffers
- Pulse Amplifiers and Peak Detectors

APPLICATION NOTES:

PERFORMANCE DISCUSSION: The LM6172 is a dual high-speed, low power, voltage feedback amplifier. It is unity-gain stable and offers outstanding performance with only 2.3 mA of supply current per channel. The combination of 100 MHz unity-gain bandwidth, 3000V/us slew rate, 50 mA per channel output current and other attractive features make it easy to implement the LM6172 in various applications. Quiescent power of the LM6172 is 138 mW operating at ±15V supply and 46 mW at ±5V supply.

CIRCUIT OPERATION: The class AB input stage in the LM6172 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the LM6172 Simplified Schematic (AN00006), Q1 through Q4 form the equivalent of the current feedback input buffer, RE the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

SLEW RATE CHARACTERISTIC: The slew rate of LM6172 is determined by the current available to charge and discharge an internal high impedance node capacitor. This current is the differential input voltage divided by the total degeneration resistor RE. Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations.

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external series resistor such as 1k Ohm to the input of LM6172, the slew rate is reduced to help lower the overshoot, which reduces settling time.

Applications (Continued)

REDUCING SETTLING TIME: The LM6172 has a very fast slew rate that causes overshoot and undershoot. To reduce settling time on the LM6172, a 1 k Ohm resistor can be placed in series with the input signal to decrease slew rate. A feedback capacitor can also be used to reduce overshoot and undershoot. This feedback capacitor serves as a zero to increase the stability of the amplifier circuit. A 2 pF feedback capacitor is recommended for initial evaluation. When the LM6172 is configured as a buffer, a feedback resistor of 1 k Ohm must be added in parallel to the feedback capacitor.

Another possible source of overshoot and undershoot comes from a capacitive load at the output. Please see the section "Driving Capacitive Loads" for more detail.

LAYOUT CONSIDERATION: Printed Circuit Boards and High Speed Op Amps: There are many things to consider when designing PC boards for high speed op amps. Without proper caution, it is very easy to cause excessive ringing, oscillation and to degrade the AC performance in high speed circuits. As a rule, the signal traces should be short and wide to provide low inductance and low impedance paths. Any unused board space must be grounded to reduce stray signal pickup. Critical components should also be grounded at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect frequency performance. It is better to solder the amplifier directly into the PC board without using any socket.

USING PROBES: Active (FET) probes are ideal for taking high frequency measurements because they have wide bandwidth, high input impedance, and low input capacitance. However, the probe ground leads provide a long ground loop that will produce errors in measurement. Instead, the probes can be grounded directly to the oscilloscope by removing the ground leads and probe jackets and using scope probe jacks.

COMPONENT SELECTION & FEEDBACK RESISTOR: It is important in high speed applications to keep all component leads short because wires are inductive at high frequency. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high speed amplifiers. For the LM6172, a feedback resistor of 1k Ohm gives optimal performance.

COMPENSATION FOR INPUT CAPACITANCE: The combination of an amplfier's input capacitance, with the gain setting resistors, adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value Cf>(Rg X Cin)/Rf can be used to cancel that pole. For the LM6172, a feedback capacitor of 2pF is recommended. AN00003 illistrates the compensation circuit.

POWER SUPPLY BYPASSING: Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Both positive and negative device power supply pins should be bypassed individually by placing 0.01uF ceramic capacitors directly to the device supply pins, and 2.2uF tantalum capacitors within 0.25 inch of the power supply pins. See AN00004.

TERMINATION: In high frequency applications, reflections occur if signals are not properly terminated. Figure 6, in the Commercial Data Book, shows a properly terminated signal while, Figure 7, in the Commercial Data Book, shows an improperly terminated signal.

To minimize reflection, coaxial cable, with characteristic impedance matched to the signal source, should be used. The other end of the cable should be terminated with the same value terminator or resistor. For the commonly used cables, RG59 has 75 Ohm characteristic impedance, and RG58 has 50 Ohm characteristic impedance.

DRIVING CAPACITIVE LOADS: Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown in AN00007. The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends upon the value of the isolation resistor; the bigger the isolation resistor, the more damped (slow) the pulse response becomes. For LM6172, a 50 Ohm isolation resistor is recommended for initial evaluation.

POWER DISSIPATION: The maximum power allowed to dissipate in a device is defined as: Pd=(Tj(max) - TA)/ThetaJA, where Pd is the power dissipation in a device, Tj(max) is the maximum junction temperature, TA is the ambient temperature, ThetaJA is the thermal resistance of a particular package.

For example, for the LM6172 in a J-8 package, the maximum power dissipation at 25 C ambient temperature is 1030mW.

Thermal resistance, ThetaJA, depends upon parameters such as die size, package size and package material. The smaller the die size and package, the higher ThetaJA becomes.

Applications (Continued)

The total power dissipation in a device can be calculated as: Pd = Pq + Pl where Pq is the quiescent power dissipated in a device with no load connected at the output, and Pl is the power dissipated in the device with a load connected at the output. Pl is not the power dissipated by the load.

Furthermore, Pq = supply current x total supply voltage with no load or Is[V+ plus V-]. Pl = output current x (voltage difference between supply voltage and output voltage of the same supply) or Il[V+ - Vo].

For example, the total power dissipated by the LM6172 with Vs = ±15V with both amplifiers swinging output voltage of 10V into 1k Ohm is:

Pd = Pq + Pl

= 2[(2.3 mA)(30V)]+2[(10mA)(15V - 10V)]

= 138mW + 100mW

= 238mW

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (V+ - V-)	36V
Differential Input Voltage (Note 6)	±10V
Maximum Junction Temperature	150 C
Power Dissipation (Note 2, 3)	1.03W
Output Short Circuit to Ground (Note 4)	Continuous
Operating Temperature Range	-55 C ≤ Ta ≤ +125 C
Storage Temperature Range	-65 C ≤ Ta ≤ +150 C
Thermal Resistance (Note 7)	
ThetaJA	
8-Pin CERAMIC DIP (Still Air)	100 C/W
(500LF/Min Air flow)	46 C/W
CERAMIC SOIC (Still Air)	124 C/W
(500LF/Min Air flow)	74 C/W
ThetaJC (Note 3)	
8-Pin CERAMIC DIP	2 C/W
CERAMIC SOIC	6 C/W
Package Weight (Typical)	
CERAMIC DIP	980mg
CERAMIC SOIC	365mg
ESD Tolerance (Note 5)	
Human Body Model	4kV

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using junction-to-ambient, rather than junction-to-case, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out of the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated junction-to-case thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.

(Continued)

Note 4: Continuous short circuit operation can result in exceeding the maximum allowed junction temperature of 150 C.
Note 5: Human body model, 1.5k Ohms in series with 100pF.
Note 6: Differential Input Voltage is measured at Vs = ±15V.
Note 7: All numbers apply for packages soldered directly into a PC board.

Recommended Operating Conditions

(Note 1)

Supply Voltage

$5.5V \leq Vs \leq 36V$

Operating Temperature Range

$-55\ C \leq Ta \leq +125\ C$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for whiÙ'OIhe device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics

DC PARAMETERS: ±15V (See NOTE 6)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Tj = 25 C, V+ = +15V, V- = -15V, Vcm = 0V, and Rl > 1M Ohm

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage					1.5	mV	1
						3.5	mV	2, 3
Iib	Input Bias Current					3	uA	1
						4	uA	2, 3
Iio	Input Offset Current					2	uA	1
						3	uA	2, 3
CMRR	Common Mode Rejection Ratio	Vcm = ±10V			70		dB	1
					65		dB	2, 3
PSRR	Power Supply Rejection Ratio	Vs = ±15V to ±5V			75		dB	1
					70		dB	2, 3
Av	Large Signal Voltage Gain	Rl = 1K Ohm	1		75		dB	1
			1		70		dB	2, 3
		Rl = 100 Ohms	1		65		dB	1
			1		60		dB	2, 3
Vo	Output Swing	Rl = 1K Ohm			12.5	-12.5	V	1
					12	-12	V	2, 3
		Rl = 100 Ohms			6	-6	V	1
					5	-5	V	2, 3
Il	Output Current (Open Loop)	Sourcing, Rl = 100 Ohms	2		60		mA	1
			2		50		mA	2, 3
		Sinking, Rl = 100 Ohms	2			-60	mA	1
			2			-50	mA	2, 3
Is	Supply Current	Both Amplifiers				8	mA	1
						9	mA	2, 3

AC PARAMETERS: ±15V (SEE NOTE 6)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Tj = 25 C, V+ = +15V, V- = -15V, Vcm = 0V

Sr	Slew Rate	Av = 2, Vin = ±2.5V, 3nS rise & fall time	3, 4		1700		V/uS	4
Gbw	Unity-Gain Bandwidth		5		80		MHz	4

Electrical Characteristics

DC PARAMETERS: ±5V (See NOTE 6)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Tj = 25 C, V+ = +5V, V- = -5V, Vcm = 0V, and Rl > 1M Ohm

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage					1	mV	1
						3	mV	2, 3
Iib	Input Bias Current					2.5	uA	1
						3.5	uA	2, 3
Iio	Input Offset Current					1.5	uA	1
						2.2	uA	2, 3
CMRR	Common Mode Rejection Ratio	Vcm = ±2.5V			70		dB	1
					65		dB	2, 3
PSRR	Power Supply Rejection Ratio	Vs = ±15V to ±5V			75		dB	1
					70		dB	2, 3
Av	Large Signal Voltage Gain	Rl = 1K Ohm	1		70		dB	1
			1		65		dB	2, 3
		Rl = 100 Ohms	1		65		dB	1
			1		60		dB	2, 3
Vo	Output Swing	Rl = 1K Ohm			3.1	-3.1	V	1
					3	-3	V	2, 3
		Rl = 100 Ohms			2.5	-2.4	V	1
					2.4	-2.3	V	2, 3
Il	Output Current (Open Loop)	Sourcing, Rl = 100 Ohms	2		25		mA	1
			2		24		mA	2, 3
		Sinking, Rl = 100 Ohms	2			-24	mA	1
			2			-23	mA	2, 3
Is	Supply Current	Both Amplifiers				6	mA	1
						7	mA	2, 3

Electrical Characteristics

DC PARAMETERS: DRIFT VALUES (±5V)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Tj = 25 C, V+ = +5V, V- = -5V, Vcm = 0V, and Rl > 1M Ohm. "Delta Calculations performed on JAN S QMLV devices at Group B, Subgroup 5 ONLY."

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage				-0.25	0.25	mV	1
Iib	Input Bias Current				-0.50	0.50	uA	1
Iio	Input Offset Current				-0.25	0.25	uA	1

DC PARAMETERS: DRIFT VALUES (±15V)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Tj = 25 C, V+ = +15V, V- = -15V, Vcm = 0V. "Delta Calculations performed on JAN S QMLV devices at Group B, Subgroup 5 ONLY."

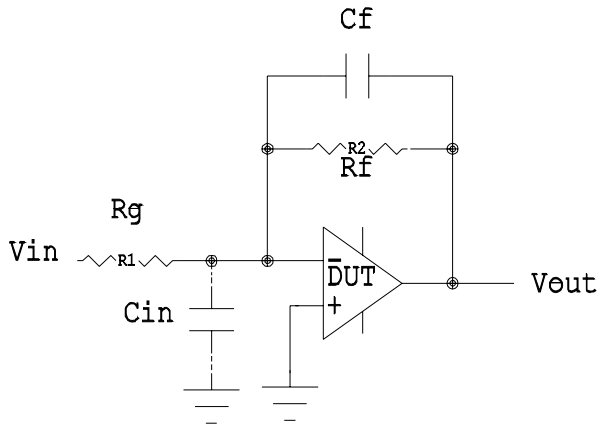
Vio	Input Offset Voltage				-0.25	0.25	mV	1
Iib	Input Bias Current				-0.50	0.50	uA	1
Iio	Input Offset Current				-0.25	0.25	uA	1

Note 1: Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For Vs = ±15V, Vout = ±5V, for Vs = ±5V, Vout = ±1V.
Note 2: The open loop output current is guaranteed, by the measurement of the open loop output voltage swing, using 100 Ohms output load.
Note 3: See AN00008 for Sr test circuit.
Note 4: Slew Rate measured between ±4V.
Note 5: See AN00009 for Gbw test circuit.
Note 6: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019.5

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06086HRC4	CERDIP (J), 8 LEAD (B/I CKT)
06339HRA1	CERAMIC SOIC (WG), 16 LEAD (B/I CKT)
AN00003A	COMPENSATING FOR INPUT CAPACITANCE
AN00004A	POWER SUPPLY BYPASSING
AN00006A	SIMPLIFIED SCHEMATIC DIAGRAM
AN00007A	ISOLATION RESISTOR TO DRIVE CAPACITIVE LOAD
AN00008A	SLEW RATE TEST CIRCUIT
AN00009A	GBW TEST CIRCUIT
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000106A	CERDIP (J), 8 LEAD (PIN OUT)
P000163A	CERAMIC SOIC (WG), 16 LEAD (PINOUT)
WG16ARC	CERAMIC SOIC (WG), 16 LEAD (P/P DWG)

See attached graphics following this page.



Compensation for Input Capacitance

AN00003A

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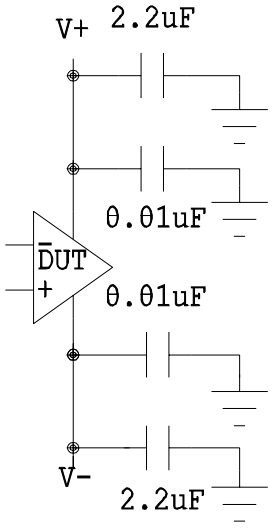
Santa Clara, CA 95051



Power Supply Bypassing

AN00004A

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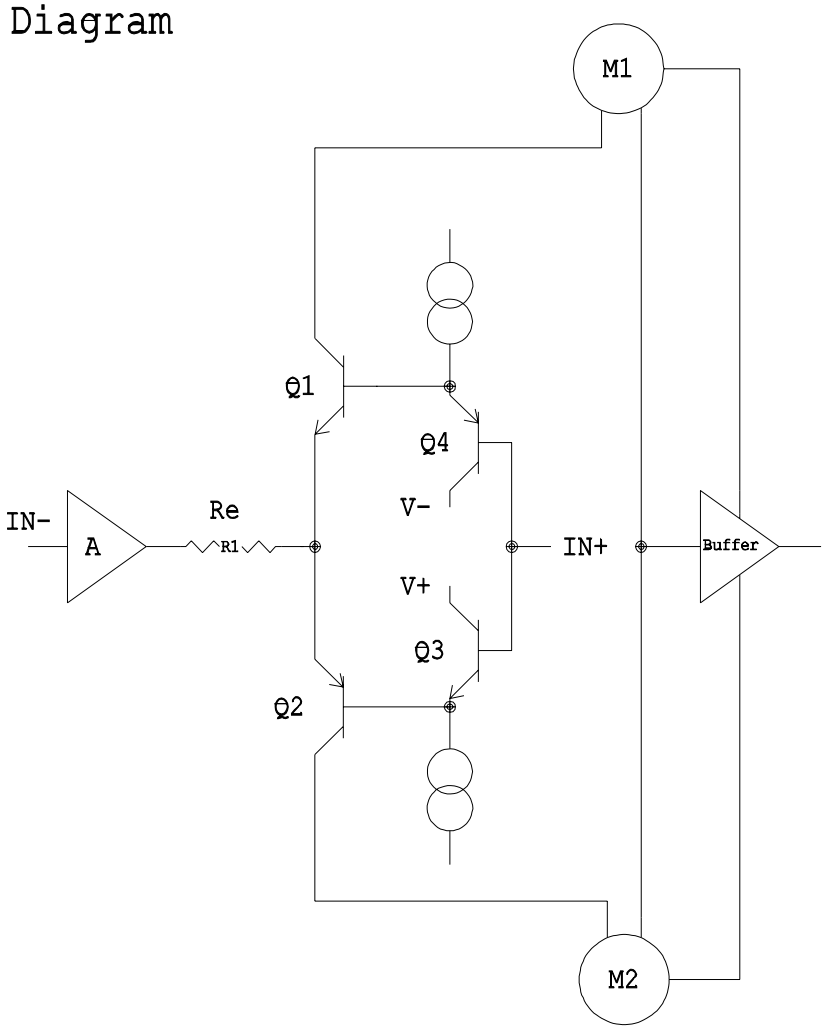
Santa Clara, CA 95051

Simplified Schematic Diagram



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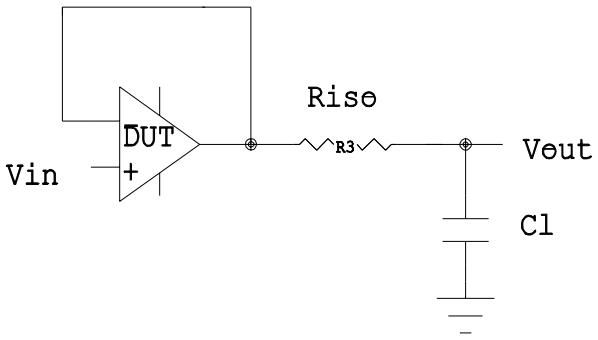
AN00006A



Isolation Resistor Used to Drive Capacitive Load

AN00007A

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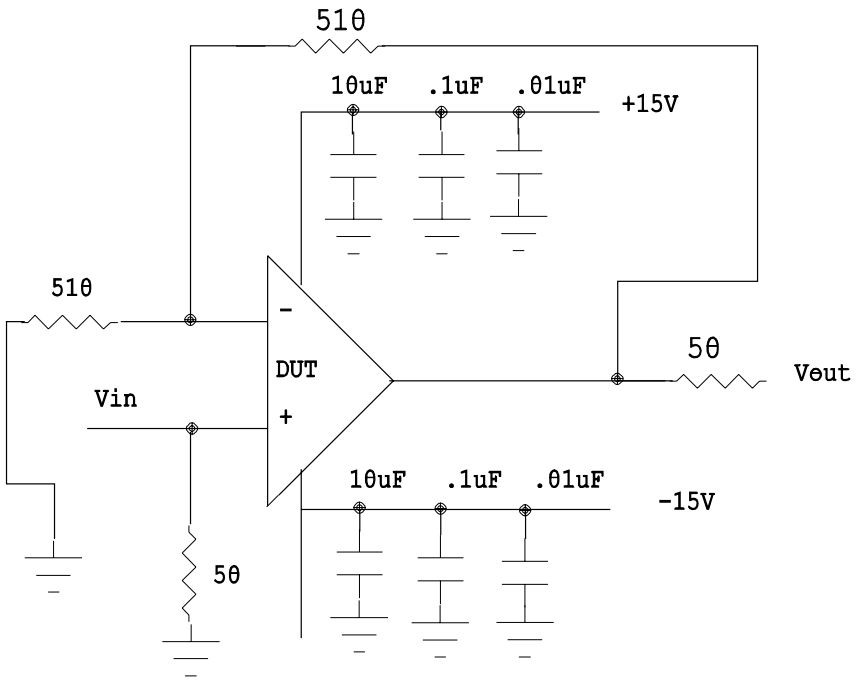
Santa Clara, CA 5051

LM6172 Slew Rate Test Circuit



Vin = +-2.5V 3nS Rise Time.

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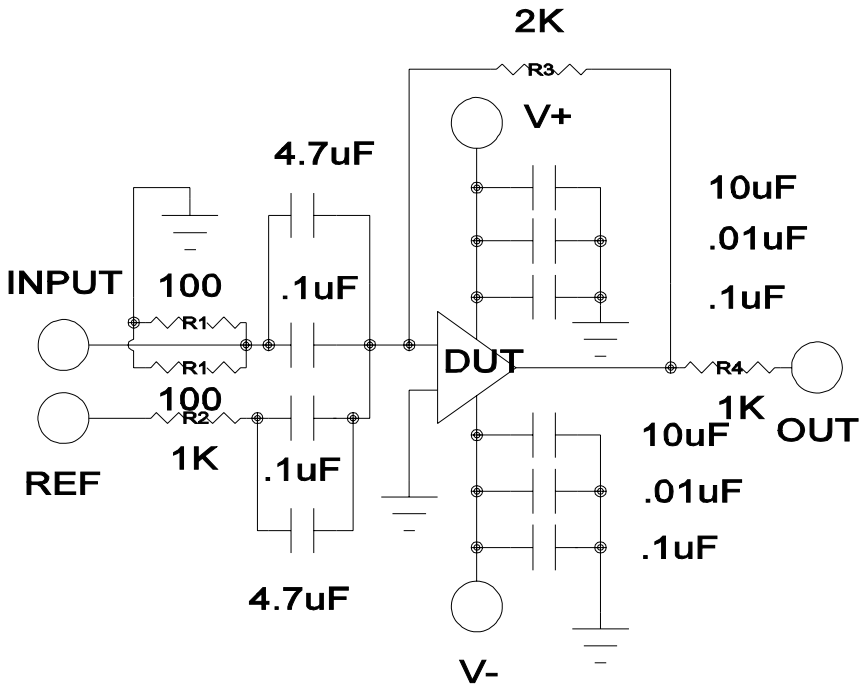
AN000088A

LM6172 GBW Test Circuit



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AN00009A

REVISIONS				
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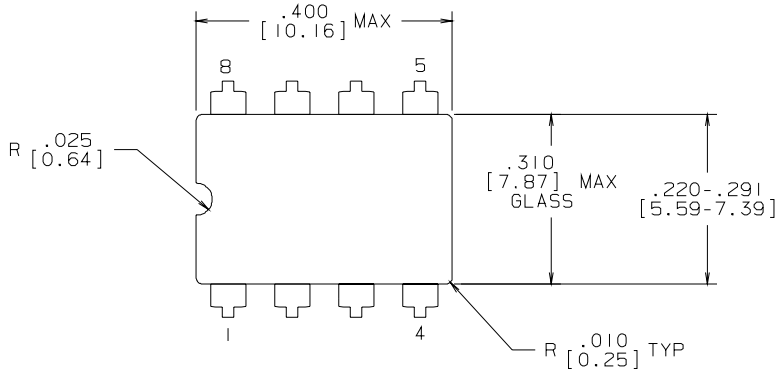
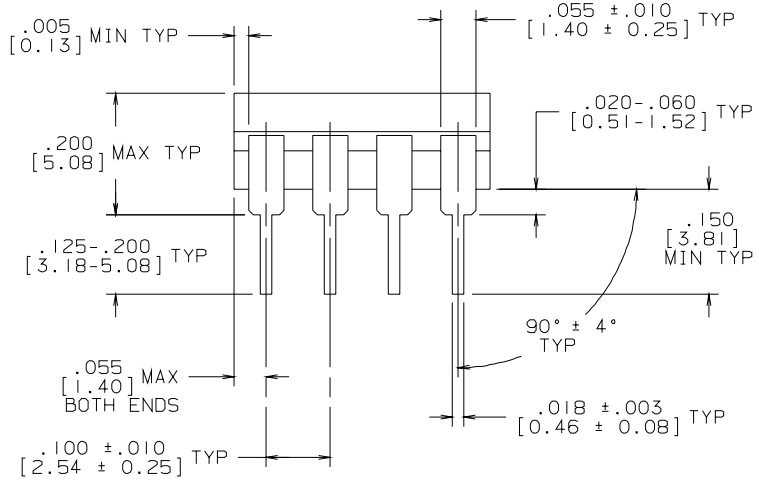
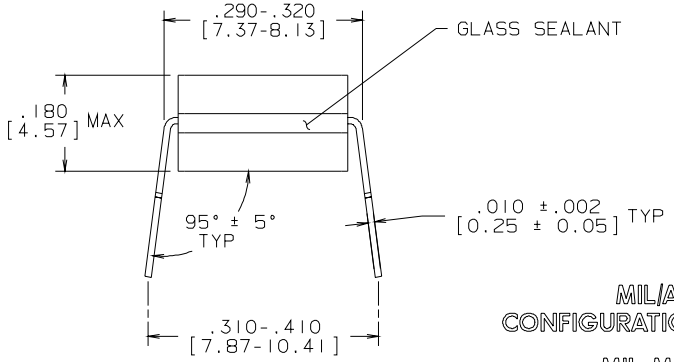






MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

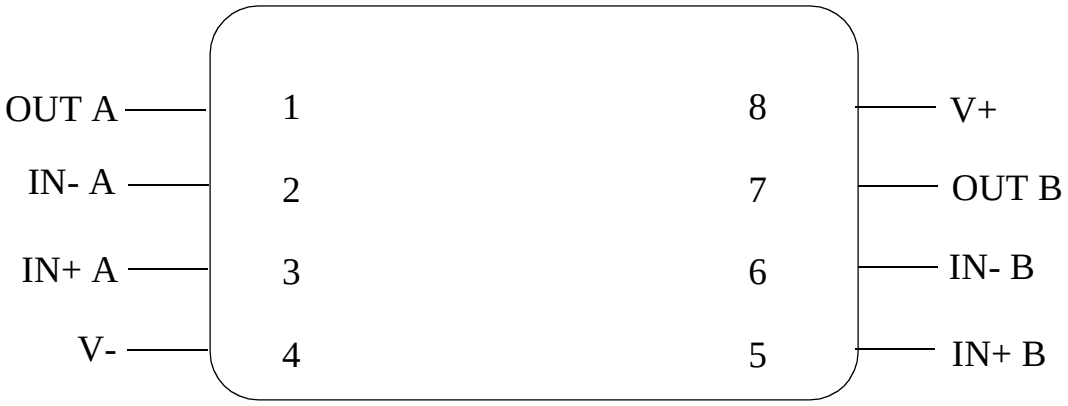
PROJECTION
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM6172J

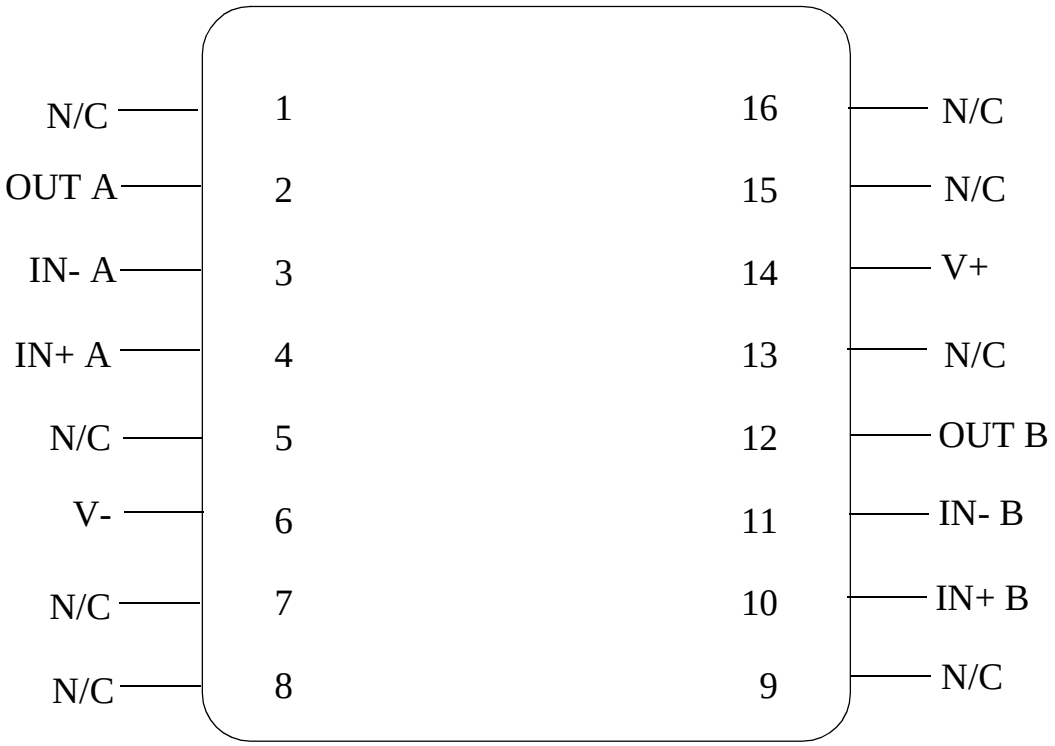
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000106A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM6172WG
16 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000163A

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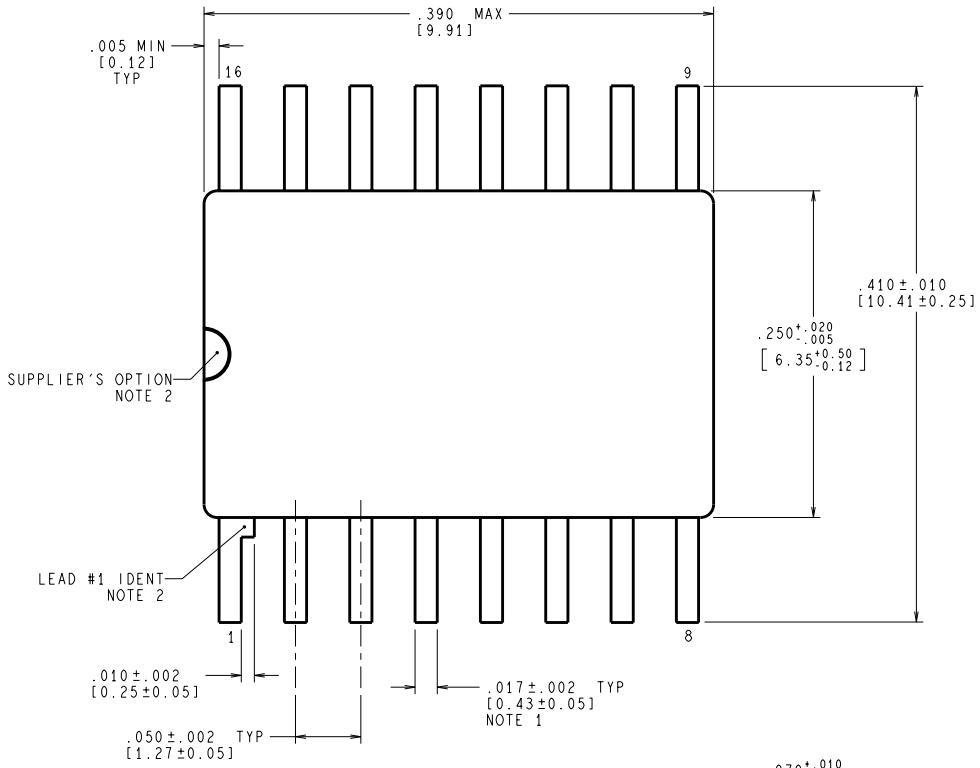
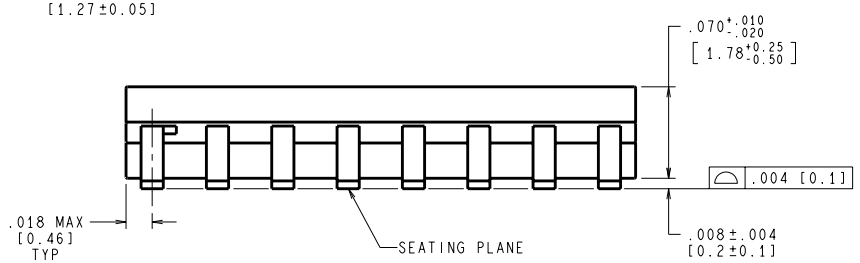
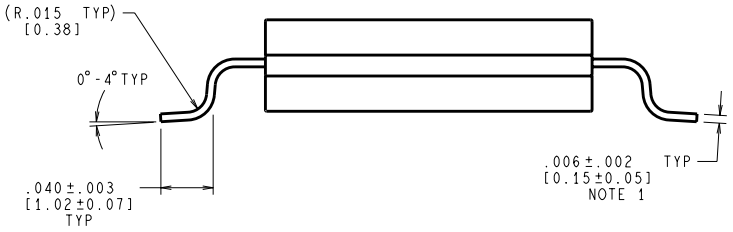
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11376	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11443	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11840	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 16 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG16A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003832	08/13/01	Rose Malone	Initial MDS Release: MNLM6172AM-X-RH, Rev. 0A0. Replacing MNLM6172AM-X, Rev. 2A1.