

MJLM118-X REV 0A0

 Original Creation Date: 07/25/95
 Last Update Date: 03/23/00
 Last Major Revision Date: 02/29/00

SINGLE OPERATIONAL AMPLIFIER, HIGH SPEED
General Description

The LM118 is a precision high speed operational amplifier designed for applications requiring wide bandwidth and high slew rate. It features a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/us and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 us.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. This device is easy to apply and offers an order of magnitude better AC performance than industry standards such as the LM709.

Industry Part Number

LM118

Prime Die

LM118

NS Part Numbers

 JL118BCA
 JL118BGA
 JL118BHA
 JL118BPA
 JL118SCA
 JL118SGA
 JL118SHA
 JL118SPA

Controlling Document

38510/10107, AMEND.2 REV G

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp Description Temp (°C)

1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

Features

- 15 MHz small signal bandwidth
- Guaranteed 50V/uS slew rate
- Maximum bias current of 250nA
- Operates from supplies of $\pm 5V$ to $\pm 20V$
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage		±20V
Power Dissipation (Note 2)		
Metal Can Pkg		750mW
J-8 Pkg		1000mW
J-14 Pkg		1250mW
Cerpak		600mW
Differential Input Current (Note 3)		±10mA
Input Voltage (Note 4)		±15V
Output Short-Circuit Duration		Continuous
Operating Temperature Range		-55 C to +125 C
Thermal Resistance		
ThetaJA		
Metal Can Pkg	(Still Air @ 0.5W)	160 C/W
	(500LF/Min Air flow @ 0.5W)	86 C/W
J-8 Pkg	(Still Air @ 0.5W)	120 C/W
	(500LF/Min Air flow @ 0.5W)	66 C/W
J-14 Pkg	(Still Air @ 0.5W)	87 C/W
	(500LF/Min Air flow @ 0.5W)	51 C/W
CERPACK	(Still Air @ 0.5W)	198 C/W
	(500LF/Min Air flow @ 0.5W)	124 C/W
ThetaJC		
Metal Can Pkg		48 C/W
J-8 Pkg		17 C/W
J-14 Pkg		17 C/W
CERPACK		22 C/W
Storage Temperature Range		-65 C to +150 C
Lead Temperature (Soldering, 10 seconds)		300 C
ESD Tolerance (Note 5)		2000V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 4: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 5: Human body model, 1.5K ohms in series with 100 pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC: $\pm V_{CC} = \pm 20V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS		
Vio	Input Offset Voltage	+Vcc = 35V, -Vcc = -5V, Vcm = -15V			-4	4	mV	1		
					-6	6	mV	2, 3		
		+Vcc = 5V, -Vcc = -35V, Vcm = 15V			-4	4	mV	1		
					-6	6	mV	2, 3		
		Vcm = 0V			-4	4	mV	1		
					-6	6	mV	2, 3		
		+Vcc = 5V, -Vcc = -5V, Vcm = 0V			-4	4	mV	1		
					-6	6	mV	2, 3		
		Iio	Input Offset Current	+Vcc = 35V, -Vcc = -5V, Vcm = -15V, Rs = 100K Ohms	5		-40	40	nA	1
					5		-80	80	nA	2, 3
+Vcc = 5V, -Vcc = -35V, Vcm = 15V, Rs = 100K Ohms	5				-40	40	nA	1		
	5				-80	80	nA	2, 3		
Vcm = 0V, Rs = 100K Ohms	5				-40	40	nA	1		
	5				-80	80	nA	2, 3		
+Vcc = 5V, -Vcc = -5V, Vcm = 0V, Rs = 100K Ohms	5				-40	40	nA	1		
	5				-80	80	nA	2, 3		
Iib+	Input Bias Current			+Vcc = 35V, -Vcc = -5V, Vcm = -15V, Rs = 100K Ohms	5		1	250	nA	1, 2
					5		1	400	nA	3
		+Vcc = 5V, -Vcc = -35V, Vcm = 15V, Rs = 100K Ohms	5		1	250	nA	1, 2		
			5		1	400	nA	3		
		Vcm = 0V, Rs = 100K Ohms	5		1	250	nA	1, 2		
			5		1	400	nA	3		
		+Vcc = 5V, -Vcc = -5V, Vcm = 0V, Rs = 100K Ohms	5		1	250	nA	1, 2		
			5		1	400	nA	3		

Electrical Characteristics

DC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $\pm V_{CC} = \pm 20V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iib-	Input Bias Current	+Vcc = 35V, -Vcc = -5V, Vcm = -15V, Rs = 100K Ohms	5		1	250	nA	1, 2
			5		1	400	nA	3
		+Vcc = 5V, -Vcc = -35V, Vcm = 15V, Rs = 100K Ohms	5		1	250	nA	1, 2
			5		1	400	nA	3
		Vcm = 0V, Rs = 100K Ohms	5		1	250	nA	1, 2
			5		1	400	nA	3
+Vcc = 5V, -Vcc = -5V, Vcm = 0V, Rs = 100K Ohms	5		1	250	nA	1, 2		
	5		1	400	nA	3		
PSRR+	Power Supply Rejection Ratio	+Vcc = 10V, -Vcc = -20V			-100	100	uV/V	1
					-150	150	uV/V	2, 3
PSRR-	Power Supply Rejection Ratio	+Vcc = 20V, -Vcc = -10V			-100	100	uV/V	1
					-150	150	uV/V	2, 3
CMRR	Common Mode Rejection Ratio	Vcm = $\pm 15V$, Vcc = $\pm 35V$ to $\pm 5V$			80		dB	1, 2, 3
Vio(adj)+	Offset Null				7		mV	1, 2, 3
Vio(adj)-	Offset Null					-7	mV	1, 2, 3
Delta Vio/Delta T	Temperature Coefficient of Input Offset Voltage	25 C \leq TA \leq 125 C	2		-50	50	uV/ C	2
		-55 C \leq TA \leq 25 C	2		-50	50	uV/ C	3
Delta Iio/Delta T	Temperature Coefficient of Input Offset Current	25 C \leq TA \leq 125 C	2		-1000	1000	pA/ C	2
		-55 C \leq TA \leq 25 C	2		-1000	1000	pA/ C	3
Ios+	Short Circuit Current	+Vcc = 15V, -Vcc = -15V, t \leq 25mS, Vcm = -15V			-65		mA	1, 2, 3
Ios-	Short Circuit Current	+Vcc = 15V, -Vcc = -15V, t \leq 25mS, Vcm = 15V				65	mA	1, 2
						80	mA	3
Icc	Power Supply Current	+Vcc = 15V, -Vcc = -15V				8	mA	1
						7	mA	2
						9	mA	3

Electrical Characteristics

DC PARAMETERS (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $\pm V_{cc} = \pm 20V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vopp+	Output Voltage Swing	Rl = 10K Ohms, Vcm = -20V			17		V	4, 5, 6
		Rl = 2K Ohms, Vcm = -20V			16		V	4, 5, 6
Vopp-	Output Voltage Swing	Rl = 10K Ohms, Vcm = 20V				-17	V	4, 5, 6
		Rl = 2K Ohms, Vcm = 20V				-16	V	4, 5, 6
Avs+	Open Loop Voltage Gain	Vout = 15V, Rl = 2K Ohms	1		50		V/mV	4
			1		32		V/mV	5, 6
		Vout = 15V, Rl = 10K Ohms	1		50		V/mV	4
			1		32		V/mV	5, 6
Avs-	Open Loop Voltage Gain	Vout = -15V, Rl = 2K Ohms	1		50		V/mV	4
			1		32		V/mV	5, 6
		Vout = -15V, Rl = 10K Ohms	1		50		V/mV	4
			1		32		V/mV	5, 6
Avs	Open Loop Voltage Gain	$\pm V_{cc} = \pm 5V$, Vout = $\pm 2V$, Rl = 2K Ohms	1		10		V/mV	4, 5, 6
		$\pm V_{cc} = \pm 5V$, Vout = $\pm 2V$, Rl = 10K Ohms	1		10		V/mV	4, 5, 6

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: $\pm V_{CC} = \pm 20V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
NI(BB)	Noise Input Broadband	BW = 10Hz to 5KHz, $R_s = 0$ Ohms				25	μV_{rms}	7
NI(PC)	Noise Input Popcorn	BW = 10Hz to 5KHz, $R_s = 20K$ Ohms				80	μV_{pk}	7
TR(tr)	Transient Response: Rise Time	$V_{in} = 50mV$, PRR = 1KHz				40	nS	7, 8A, 8B
TR(os)	Transient Response: Overshoot	$V_{in} = 50mV$, PRR = 1KHz				50	%	7, 8A, 8B
Sr+	Slew Rate	$A_v = 1$, $V_{in} = -5V$ to $+5V$			50		$V/\mu S$	7, 8B
					40		$V/\mu S$	8A
Sr-	Slew Rate	$A_v = 1$, $V_{in} = +5V$ to $-5V$			50		$V/\mu S$	7, 8B
					40		$V/\mu S$	8A
ts+	Settling Time	$V_{in} = -5V$ to $+5V$	3, 4			800	nS	12
			3, 4			1200	nS	13, 14
ts-	Settling Time	$V_{in} = +5V$ to $-5V$	3, 4			800	nS	12
			3, 4			1200	nS	13, 14

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $\pm V_{CC} = \pm 20V$. "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only".

Vio	Input Offset Voltage	$V_{cm} = 0V$			-1	1	mV	1
Iib+	Input Bias Current	$V_{cm} = 0V$, $R_s = 100K$ Ohms			-25	25	nA	1
Iib-	Input Bias Current	$V_{cm} = 0V$, $R_s = 100K$ Ohms			-25	25	nA	1

Note 1: Datalog in K = V/mV .

Note 2: Calculated parameter.

Note 3: Errorband = $\pm 2\%$.

Note 4: Test on Bench, refer to SP-16655.

Note 5: S/S $R_s = 20K$ Ohms, tested with $R_s = 100K$ Ohms for better resolution.

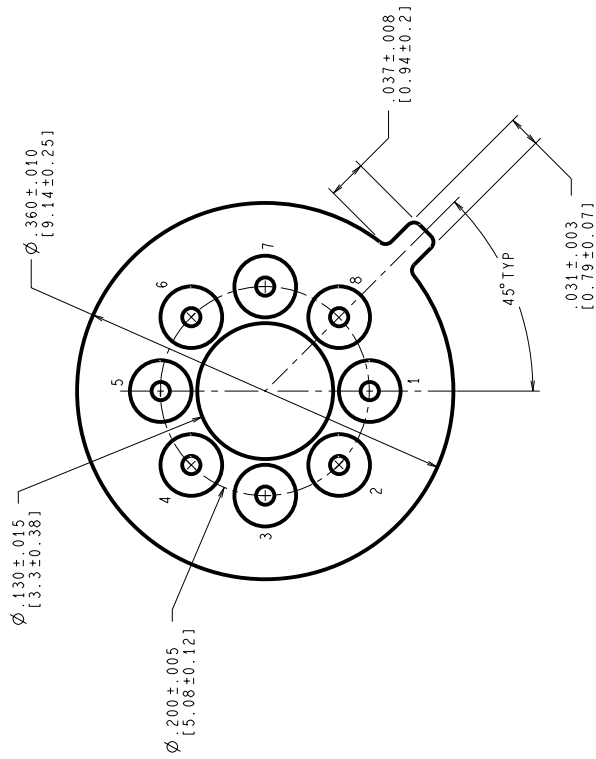
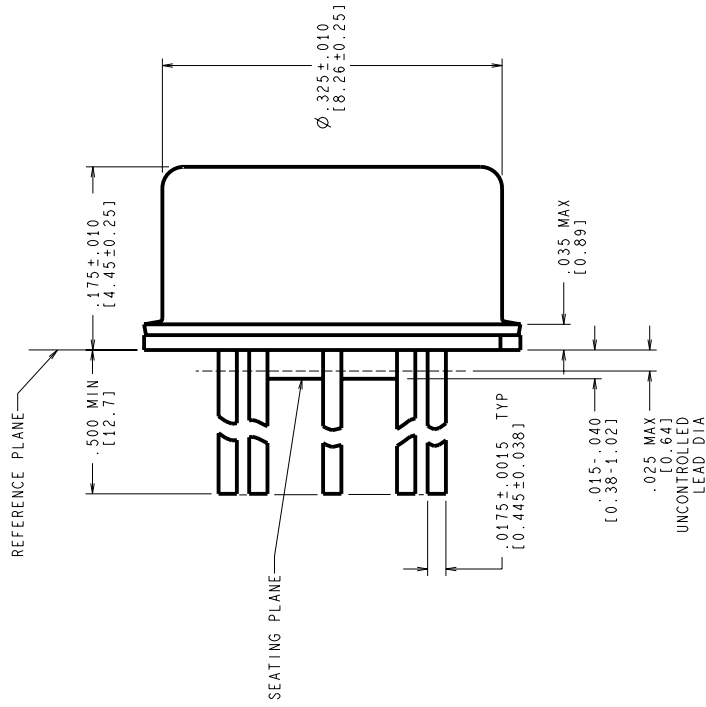
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05482HRA1	10LD CERPACK, 10LD CERAMIC SOIC (B/I CKT)
09556HR02	CERDIP (J14), CERDIP (J8) (B/I CKT)
09557HRA4	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000268A	METAL CAN (H), 8 LEAD (PINOUT)
P000315A	CERDIP (J), 8 LEAD (PINOUT)
P000316A	CERDIP (J), 14 LEAD (PINOUT)
P000473A	CERPACK (W), 10 LEAD (PIN OUT)
W10ARG	CERPACK (W), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS

LTR	DESCRIPTION	E.C. N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

- LEADS TO BE LOCATED WITHIN $.007$ IN / 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
- STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
- APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
- REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No. 95.

APPROVALS	DATE
DRN: MARTA SUCHY	06/22/95
DWG. CHK.	
ENGR. CHK.	
PROJECTION	
SCALE	SIZE
N/A	C
DRAWING NUMBER	
MKT-H08C	
REV	F

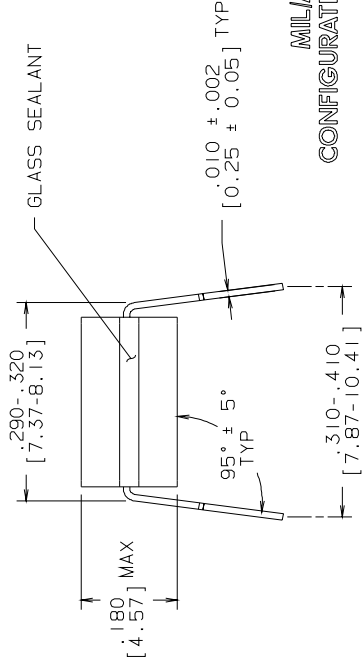
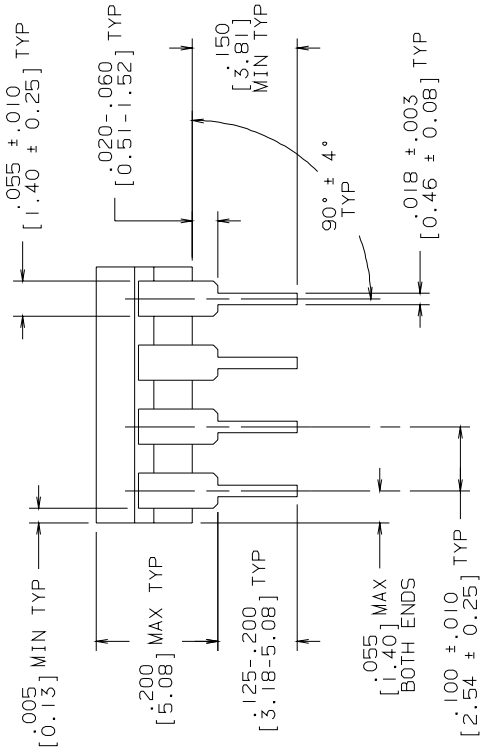
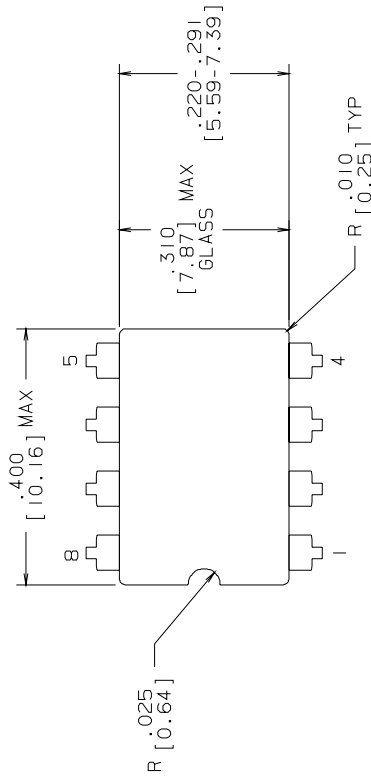
National Semiconductor
2800 Semiconductor Dr., Santa Clara, CA 95052-8090

METAL CAN,
TO-99, 8 LEAD,
.200 DIA P.C.

DO NOT SCALE DRAWING SHEET 1 of 1

REV I S I O N S

LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/



MILAERO
 CONFIGURATION CONTROL
 MIL-M-38510
 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

APPROVALS	DATE	APPROVALS	DATE
DRAWN <i>T. LEQUANG</i>	09/21/93	NATIONAL SEMICONDUCTOR CORPORATION	
DFTG. CHK.		2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
ENGR. CHK.			
APPROVAL			

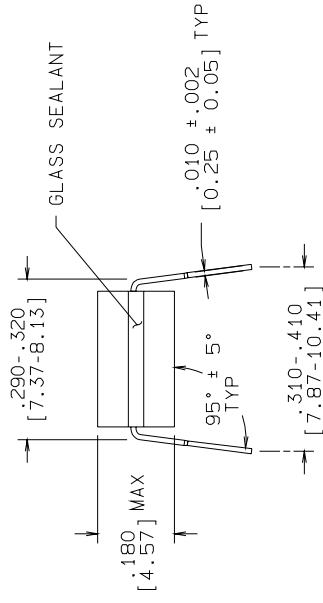
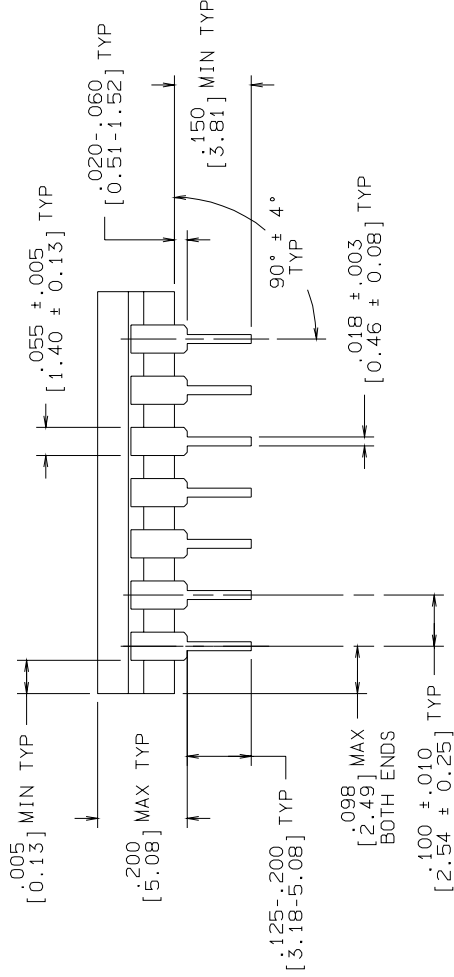
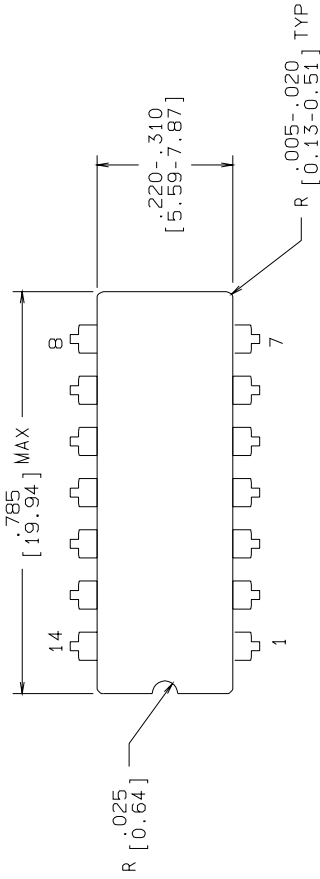
CERDIP (J),
 8 LEAD

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
	N/A	B	MKT-J08A	L
	DO NOT SCALE DRAWING	SHEET	OF	

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH TO BE 200 MICROMETERS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
- JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

R E V I S I O N S			
LTR	DESCRIPTION	E.C.N.	DATE
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93
			TL/



CONTROLLING DIMENSION: INCH

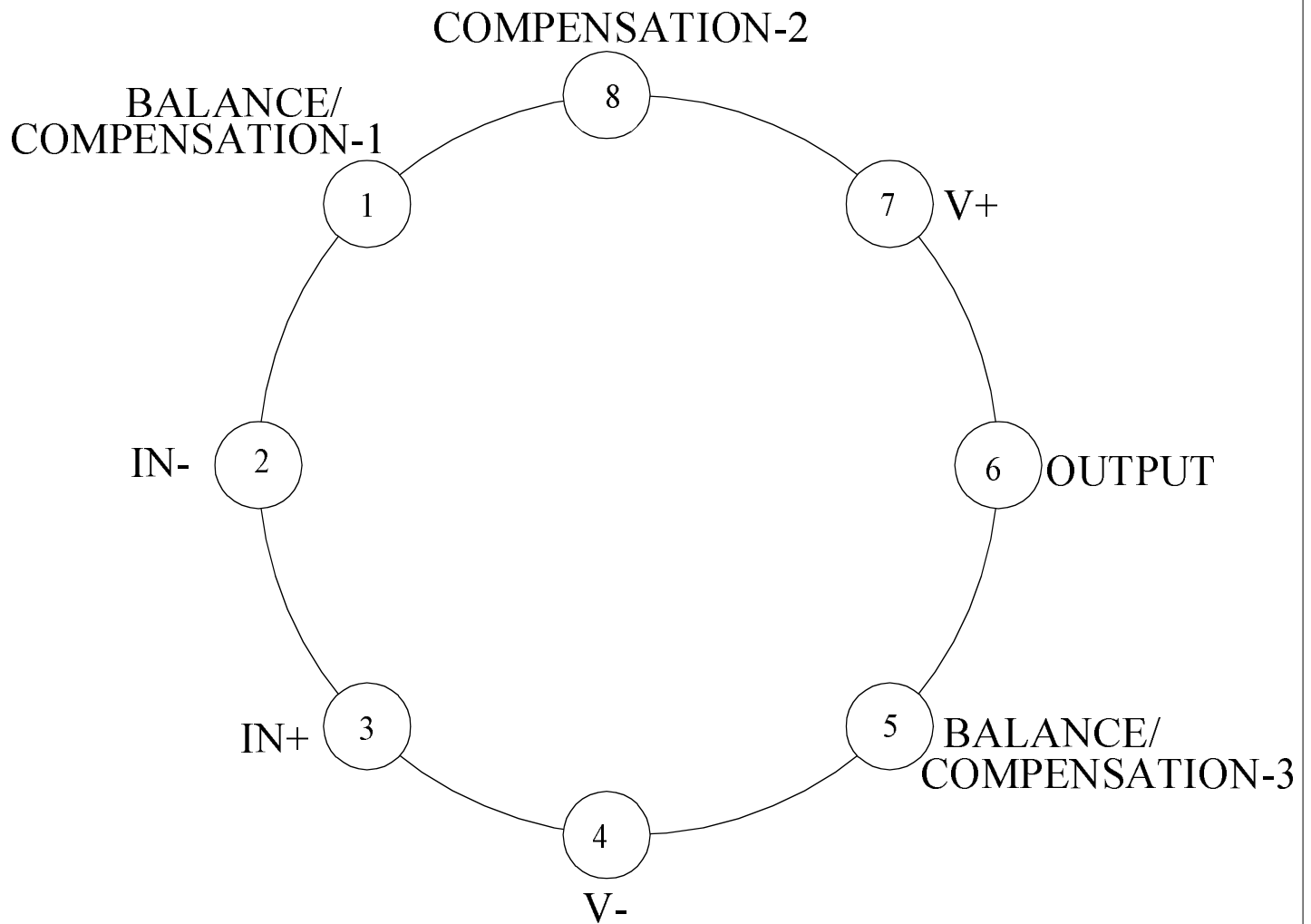
NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICRONS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE	MIL/AERO CONFIGURATION CONTROL	
DRAWN: LEQUANG	09/15/93	MIL-M-38510	
DFTG. CHK.		CONFIGURATION CONTROL	
ENGR. CHK.		NATIONAL SEMICONDUCTOR CORPORATION	
APPROVAL		2900 Semiconductor Drive, Santa Clara, CA 95052-8090	

CERDIP (J),
14 LEAD,

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
	N/A	B	MKT-J14A	H
	DO NOT SCALE	DRAWING	SHEET 1 OF 1	



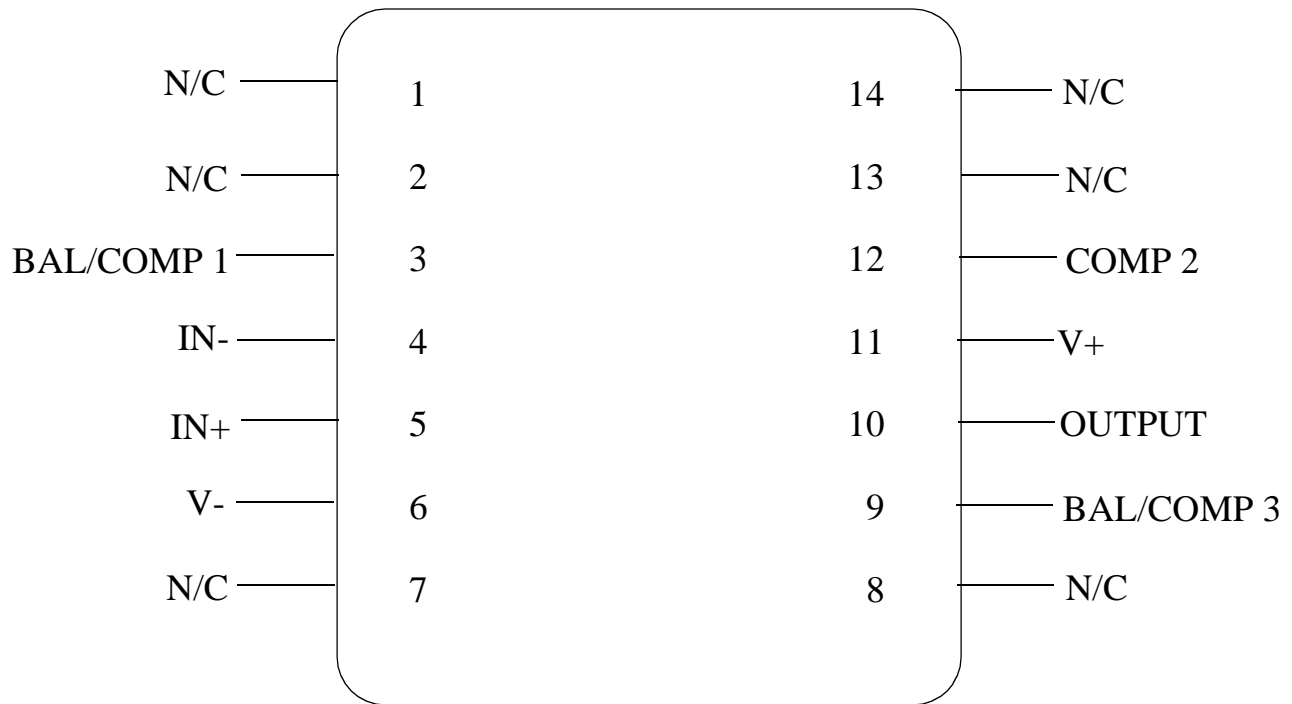
LM118H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000268A



LM118J-8
8 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000315A



National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

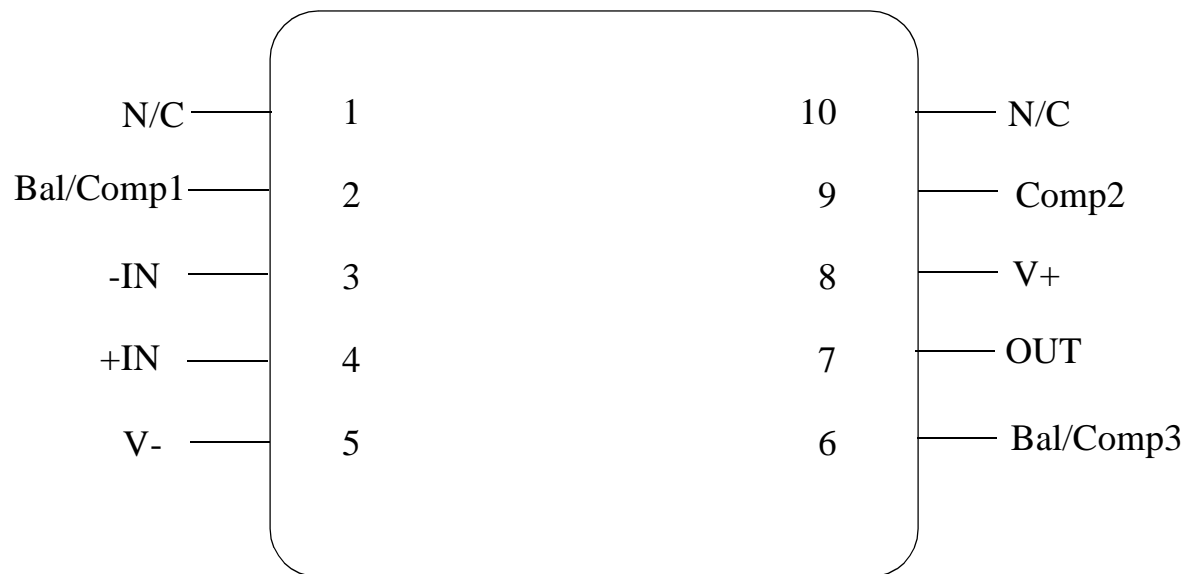


LM118J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000316A



National Semiconductor™

MIL/AEROSPACE OPERATIONS
 2900 SEMICONDUCTOR DRIVE
 SANTA CLARA, CA 95050

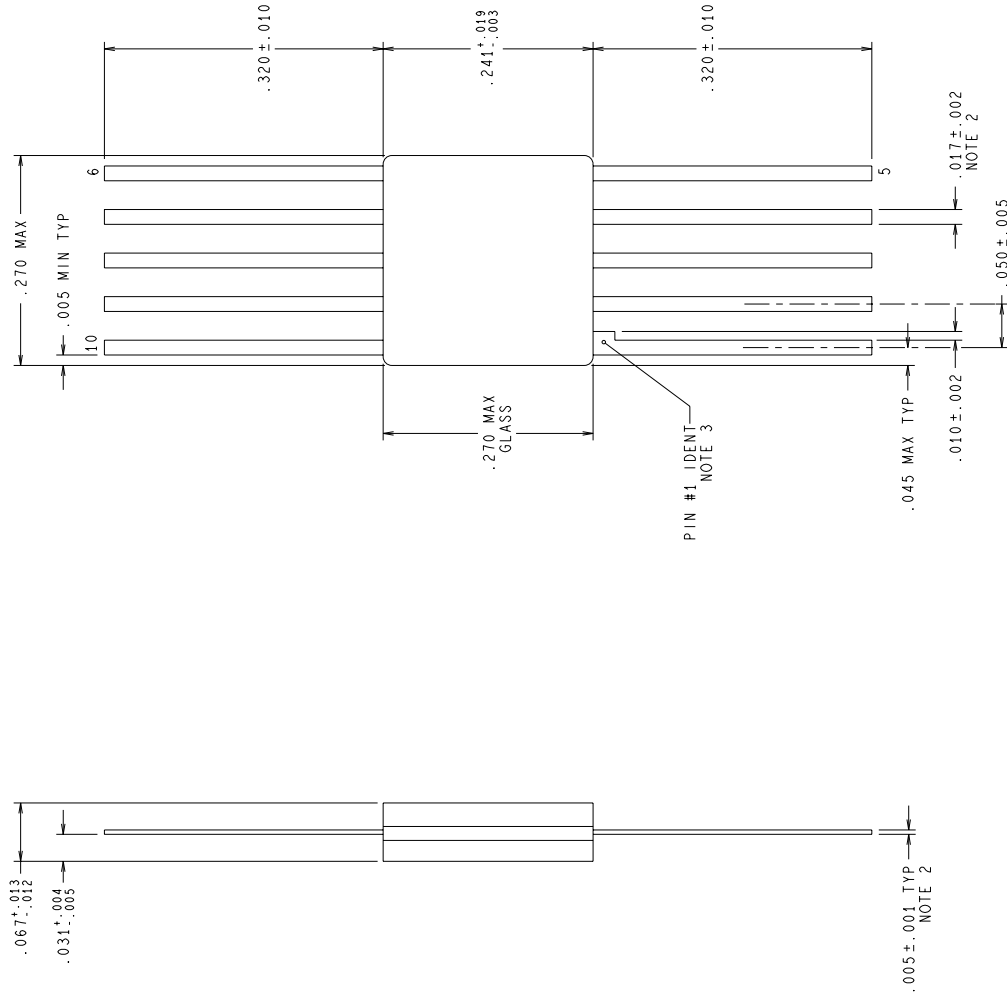


JL118SHA / JL118BHA
10 - LEAD CERPACK
CONNECTION DIAGRAM
TOP VIEW
P000473A



National Semiconductor
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
F	REVISE AND REDRAW PER NEW STANDARD.	10510	07/28/94 DEG/AEP
G	.017±.002 WAS .017±.020.	10654	10/21/94 DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
 - a) A NOTCH OR OTHER MARK WITHIN THIS AREA
 - b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION M0-003, VARIATION AG, DATED 06/01/76.

MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

APPROVALS		DATE	
DRWN	<i>D. F. Grady</i>		07/28/94
DTG. CHK.			
ENGR. CHK.			

PROJECTION			
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W10A	G

National Semiconductor	
2800 Semiconductor dr., Santa Clara, CA 95052-8090	
CERPACK, 10 LEAD	
DO NOT SCALE DRAWING	SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003642	03/23/00	Rose Malone	Update MDS - MJLM118-X, Rev. 0CL to MJLM118-X, Rev. 0A0 Fully Released MDS.