

74F113 Dual JK Negative Edge-Triggered Flip-Flop

General Description

The 'F113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the flip-flop will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

Asynchronous input:

LOW input to $\bar{S}_D$ sets Q to HIGH level
Set is independent of clock

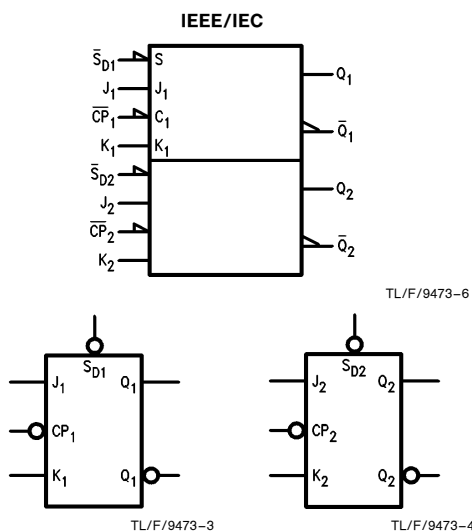
Features

- Guaranteed 4000V minimum ESD protection

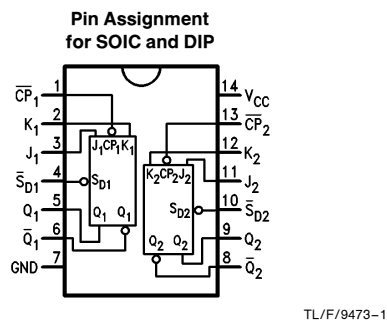
Commercial	Package Number	Package Description
74F113PC	N14A	14-Lead (0.300" Wide) Molded Dual-In-Line
74F113SC (Note 1)	M14A	14-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F113SJ (Note 1)	M14D	14-Lead (0.300" Wide) Molded Small Outline, EIAJ

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Logic Symbols



Connection Diagram



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Unit Loading/Fan Out

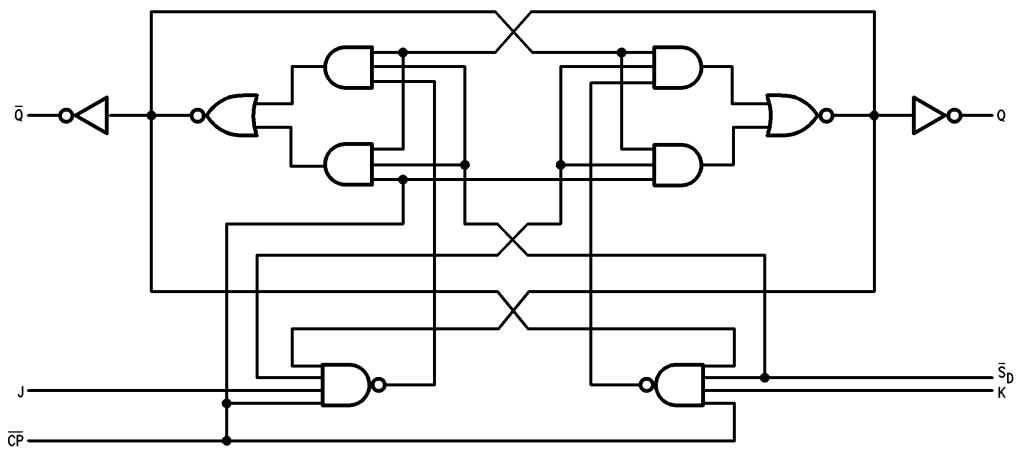
Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
J ₁ , J ₂ , K ₁ , K ₂	Data Inputs	1.0/1.0	20 μA/ −0.6 mA
CP ₁ , CP ₂	Clock Pulse Inputs (Active Falling Edge)	1.0/4.0	20 μA/ −2.4 mA
S _{D1} , S _{D2}	Direct Set Inputs (Active LOW)	1.0/5.0	20 μA/ −3.0 mA
Q ₁ , Q ₂ , Q ₁ , Q ₂	Outputs	50/33.3	−1 mA/20 mA

Truth Table

Inputs				Outputs	
S _D	CP	J	K	Q	Q̄
L	X	X	X	H	L
H	↘	h	h	Q ₀	Q ₀
H	↘	l	h	L	H
H	↘	h	l	H	L
H	↘	l	l	Q ₀	Q ₀

H(h) = HIGH Voltage Level
L(l) = LOW Voltage level
↘ = HIGH-to-LOW Clock Transition
X = Immaterial
Q₀ (Q̄₀) = Before HIGH-to-LOW Transition of Clock
Lower case letters indicate the state of the referenced input or output prior to the HIGH-to-LOW clock transition.

Logic Diagram (One Half Shown)



TL/F/9473-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Commercial	

DC Electrical Characteristics

Symbol	Parameter	74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	74F 10% V _{CC} 74F 5% V _{CC}	2.5 2.7		V	Min	I _{OH} = −1 mA I _{OH} = −1 mA
V _{OL}	Output LOW Voltage	74F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current	74F		5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	74F		7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	74F		50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6 −2.4 −3.0	mA	Max	V _{IN} = 0.5V (J _n , K _n) V _{IN} = 0.5V (C _{Pn}) V _{IN} = 0.5V (S _{Dn})
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			−50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		−60	−150	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current		12	19	mA	Max	

AC Electrical Characteristics

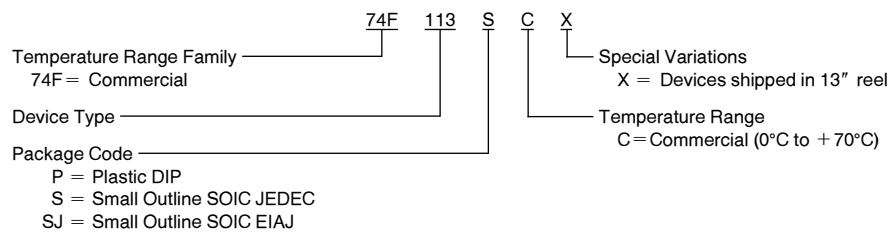
Symbol	Parameter	74F			74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	
f _{max}	Maximum Clock Frequency	85	105		80		MHz
t _{PLH} t _{PHL}	Propagation Delay $\overline{CP}_n$ to Q _n or $\overline{Q}_n$	2.0	4.0	6.0	2.0	7.0	ns
t _{PLH} t _{PHL}	Propagation Delay $\overline{SD}_n$ to Q _n or $\overline{Q}_n$	2.0	4.5	6.5	2.0	7.5	ns

AC Operating Requirements

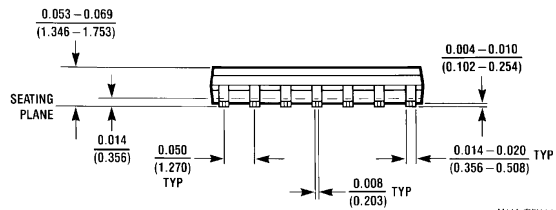
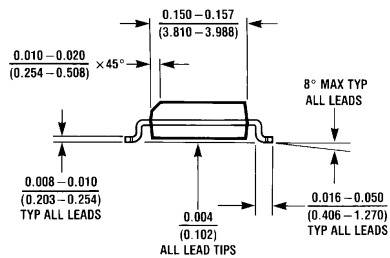
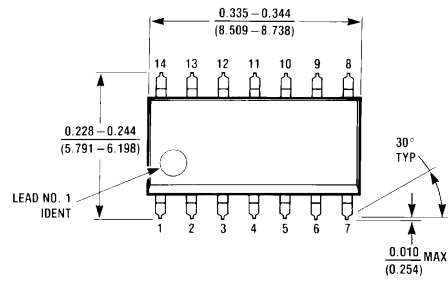
Symbol	Parameter	74F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	4.0		5.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW J_n or K_n to $\overline{CP}_n$	0		0		
$t_w(\text{H})$ $t_w(\text{L})$	$\overline{CP}_n$ Pulse Width HIGH or LOW	4.5		5.0		
$t_w(\text{L})$	$\overline{SD}_n$ Pulse Width, LOW	4.5		5.0		ns
t_{rec}	$\overline{SD}_n$ to $\overline{CP}_n$ Recovery Time	4.0		5.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

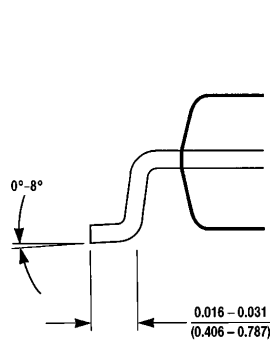


Physical Dimensions inches (millimeters)

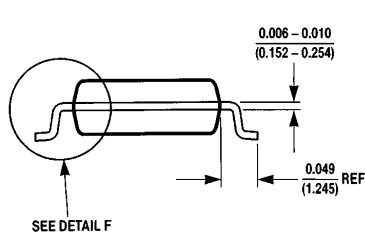
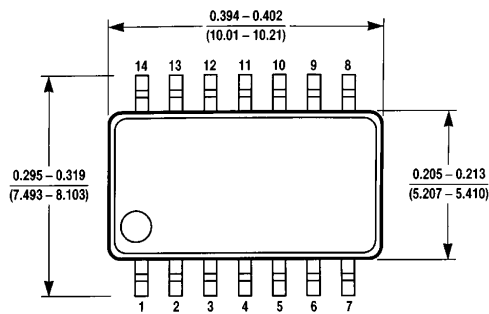


M14A (REV H)

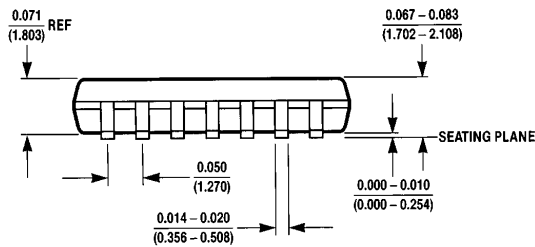
14-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M14A



DETAIL F



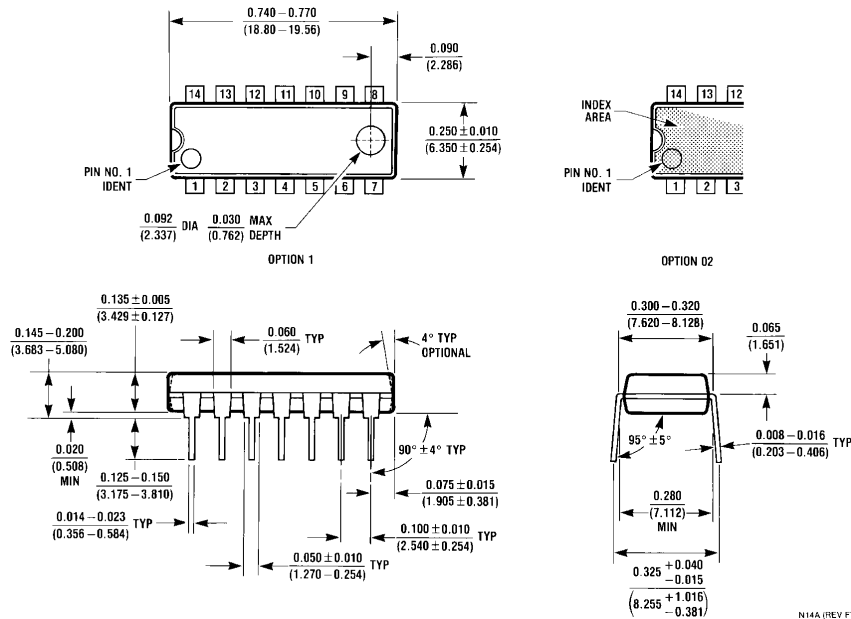
SEE DETAIL F



M14D (REV A)

14-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M14D

Physical Dimensions inches (millimeters) (Continued)



**14-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N14A**

N14A (REV F)

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