

54F/74F189 64-Bit Random Access Memory with TRI-STATE® Outputs

General Description

The 'F189 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are TRI-STATE and are in the high impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

Features

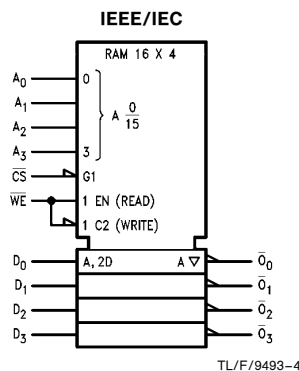
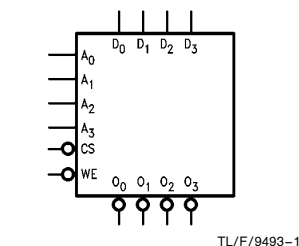
- TRI-STATE outputs for data bus applications
- Buffered inputs minimize loading
- Address decoding on-chip
- Diode clamped inputs minimize ringing
- Available in SOIC, (300 mil only)

Commercial	Military	Package Number	Package Description
74F189PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F189DL (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F189SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F189SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F189FL (Note 2)	W16A	16-Lead Cerpack
	54F189LL (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

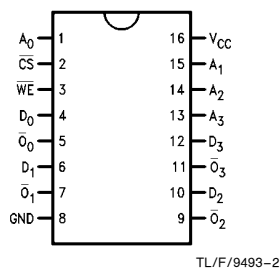
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DLQB, FLQB and LLQB.

Logic Symbols

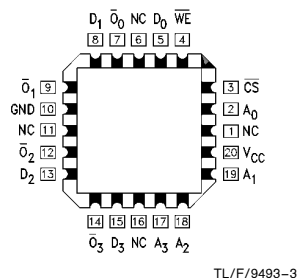


Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



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Unit Loading/Fan Out

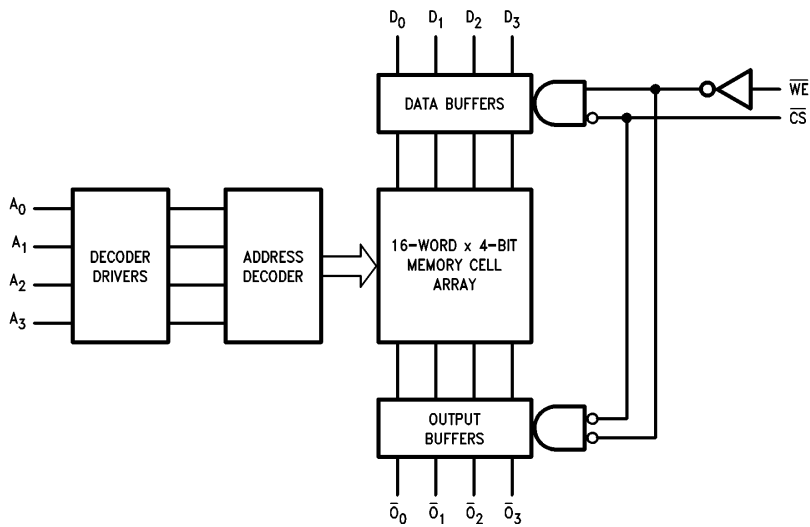
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
A ₀ –A ₃	Address Inputs	1.0/1.0	20 μA/ –0.6 mA
$\overline{\text{CS}}$	Chip Select Input (Active LOW)	1.0/1.0	20 μA/ –1.2 mA
$\overline{\text{WE}}$	Write Enable Input (Active LOW)	1.0/1.0	20 μA/ –0.6 mA
D ₀ –D ₃	Data Inputs	1.0/1.0	20 μA/ –0.6 mA
$\overline{\text{O}}_0$ – $\overline{\text{O}}_3$	Inverted Data Outputs	150/40 (33.3)	–3.0 mA/24 mA (20 mA)

Function Table

Inputs		Operation	Condition of Outputs
$\overline{\text{CS}}$	$\overline{\text{WE}}$		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



TL/F/9493-5

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.5 2.4 2.7 2.7			V	Min	I _{OH} = −1 mA I _{OH} = −3 mA I _{OH} = −1 mA I _{OH} = −3 mA I _{OH} = −1 mA I _{OH} = −3 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}			0.5 0.5	V	Min	I _{OL} = 20 mA I _{OL} = 24 mA
I _{IH}	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current				−0.6 −1.2	mA	Max	V _{IN} = 0.5V (except $\overline{CS}$) V _{IN} = 0.5V ($\overline{CS}$)
I _{OZH}	Output Leakage Current				50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current				−50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test				500	μA	0.0V	V _{OUT} = 5.25V
I _{CCZ}	Power Supply Current			37	55	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			*T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL}	Access Time, HIGH or LOW A _n to $\overline{O}_n$	10.0 8.0	18.5 13.5	26.0 19.0	9.0 8.0	32.0 23.0	10.0 8.0	27.0 20.0	ns
t _{PZH} t _{PZL}	Access Time, HIGH or LOW $\overline{CS}$ to $\overline{O}_n$	3.5 5.0	6.0 9.0	8.5 13.0	3.5 5.0	10.5 15.0	3.5 5.0	9.5 14.0	ns
t _{PHZ} t _{PLZ}	Disable Time, HIGH or LOW $\overline{CS}$ to $\overline{O}_n$	2.0 3.0	4.0 5.5	6.0 8.0	2.0 2.5	8.0 10.0	2.0 3.0	7.0 9.0	ns
t _{PZH} t _{PZL}	Write Recovery Time, HIGH or LOW $\overline{WE}$ to $\overline{O}_n$	6.5 6.5	15.0 11.0	28.0 15.5	6.5 6.5	37.5 17.5	6.5 6.5	29.0 16.5	ns
t _{PHZ} t _{PLZ}	Disable Time, HIGH or LOW $\overline{WE}$ to $\overline{O}_n$	4.0 5.0	7.0 9.0	10.0 13.0	3.5 5.0	12.0 15.0	4.0 5.0	11.0 14.0	ns

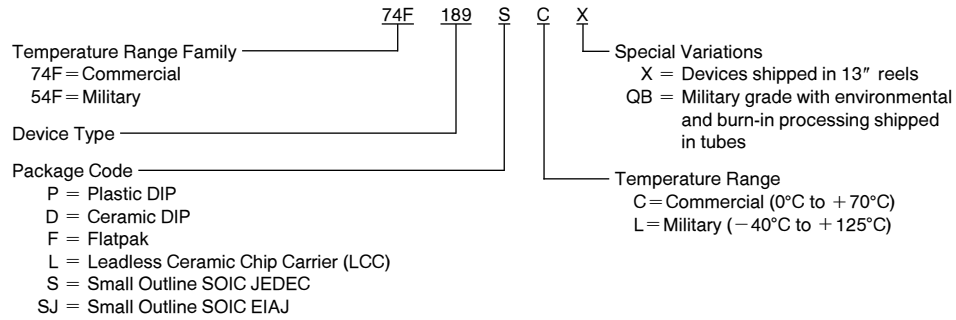
AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$*T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW A_n to $\overline{WE}$	0 0		0 0		0 0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW A_n to $\overline{WE}$	2.0 2.0		2.0 2.0		2.0 2.0		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW D_n to $\overline{WE}$	10.0 10.0		11.0 11.0		10.0 10.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW D_n to $\overline{WE}$	0 0		2.0 2.0		0 0		
$t_s(\text{L})$	Setup Time, LOW $\overline{CS}$ to $\overline{WE}$	0		0		0		ns
$t_h(\text{L})$	Hold Time, LOW $\overline{CS}$ to $\overline{WE}$	6.0		7.5		6.0		
$t_w(\text{L})$	$\overline{WE}$ Pulse Width, LOW	6.0		15.0		6.0		ns

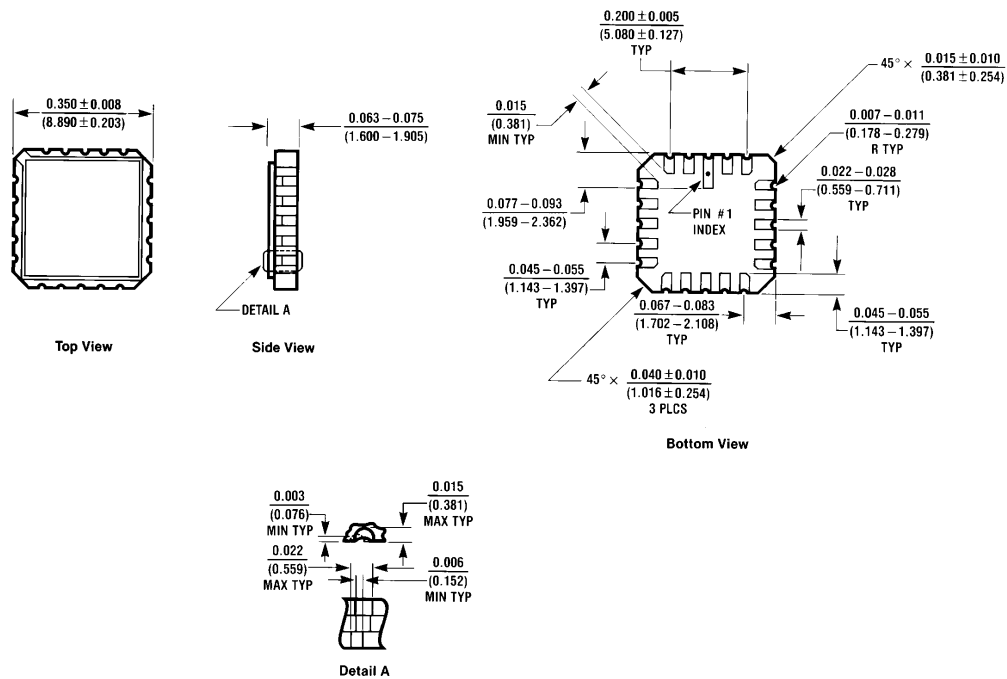
$*T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



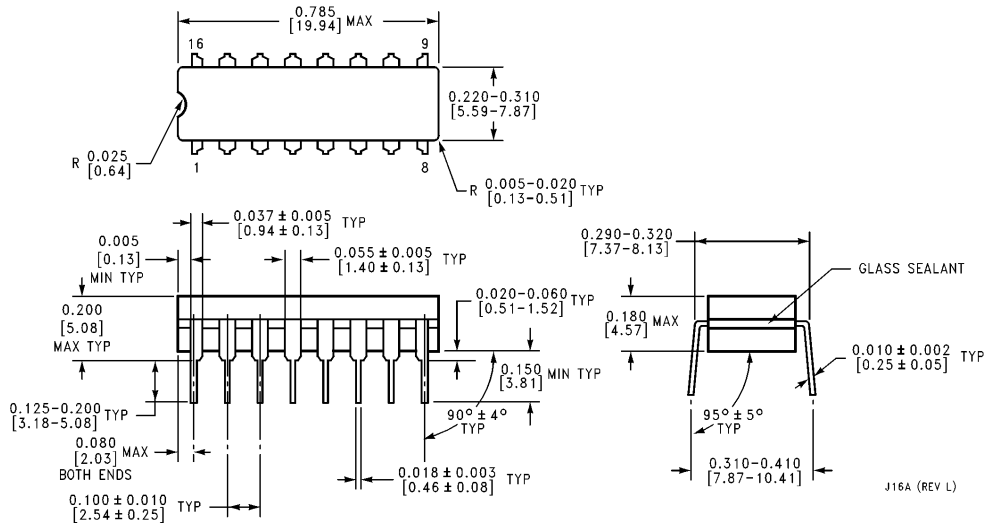
Physical Dimensions inches (millimeters)



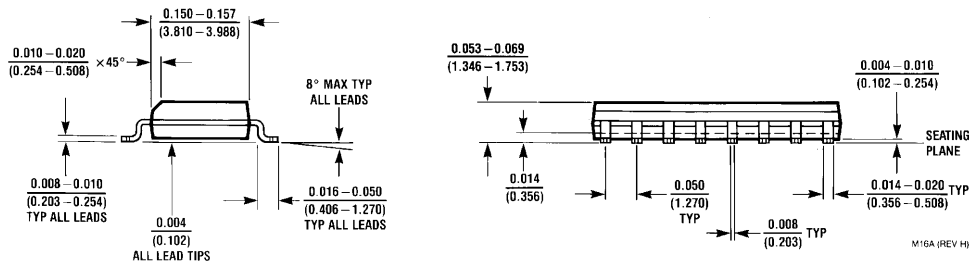
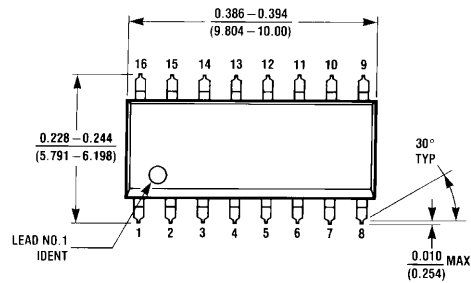
**20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A**

E20A (REV D)

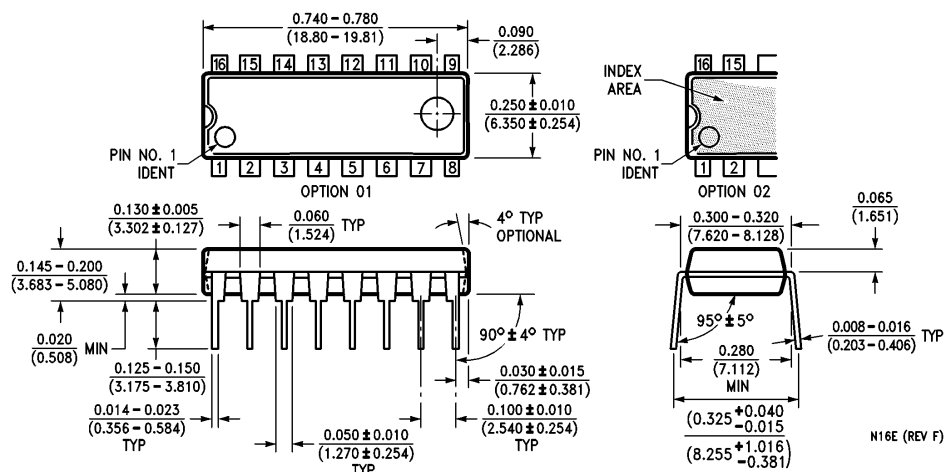
Physical Dimensions inches (millimeters) (Continued)



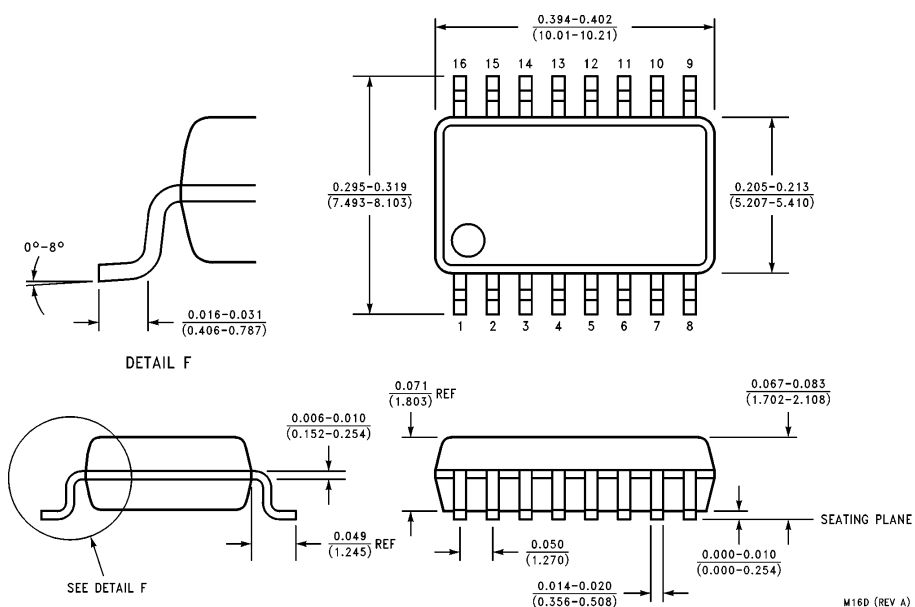
16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A



16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)

**16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E**



16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D

